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Radiation-hard miniature optical engine with high bandwidth

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ABSTRACT

Future silicon trackers will be operated in an intense radiation environment and require large volumes of data to be transmitted off detector. In addition, the optical modules must be of low mass in order to limit multiple scattering and nuclear interactions that would degrade the overall performance of the detector. We present a miniature optical engine that satisfies these constraints. The optical engine consists of an ASIC driving a VCSEL (Vertical Cavity Surface Emitting Laser) array in an optical package. Two ASICs are designed to operate a 12-channel VCSEL array at 1.28 or 5.12 Gb/s per channel, which yields a total data rate of up to 60 Gb/s. The core transistors are fabricated in a 65 nm CMOS process which enhance the radiation-hardness. Each channel contains equalizer (CTLE) and clock-data recovery circuits (CDR) so that the ASIC can restore the highly distorted electrical signal after propagating through several meters of cables of small diameter. The equalizer, CDR, and VCSEL driver are configured via a digital I^2C chip interface with triple redundant memory to mitigate single event upset (SEU) effects. The bias and modulation currents are controlled by a digital-to-analog converter (DAC). We present the design of the circuit together with the results of the simulations and preliminary measurements.

1. Introduction

The use of VCSEL arrays allows the fabrication of a compact optical module for high-speed data transmission. The compact design is enabled by readily available commercial high-speed VCSEL arrays. Modern VCSELs are humidity tolerant and hence no hermitic packaging is needed. With the use of a 12-channel array operating at 5.12 Gb/s per channel, an array based optical module can deliver an aggregate data rate of 60 Gb/s. With a standard spacing of 250 μm between two adjacent VCSELs, the width of a 12-channel array is only slightly over 3 mm. This allows the fabrication of a compact optical module for the installation in locations where space is at a premium. The use of a fiber ribbon also reduces the fiber handling. Moreover, a fiber ribbon is less fragile than a single-channel fiber. These advantages greatly simplify the production, testing, and installation of optical links.

VCSEL arrays are widely used in off-detector data transmission in high-energy physics [1]. The first implementation [2] of VCSEL arrays for on-detector application is in the optical links of the ATLAS pixel detector. The experience from the operation of this first generation of array-based links was satisfactory. The ATLAS experiment therefore continued to use VCSEL arrays in the second-generation optical links [3] for a new layer of the pixel detector, the insertable barrel layer (IBL), installed in early 2014 during the long shutdown (LS1) to prepare the Large Hadron Collider (LHC) for collisions at the center-of-mass energy of 13 TeV. In addition, ATLAS also decided to move the optical links of the original pixel detector to a more accessible location. The replacement optical links are also array based.

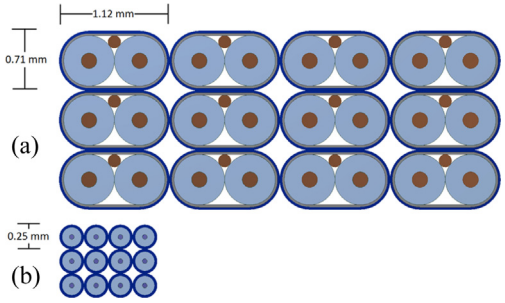

Fig. 1. Comparison of (a) twelve TwinAx cables and (b) twelve fibers in a ribbon.

The placement of the optical links at a distance from the front-end electronics is a necessity for the pixel tracking detectors at the high-luminosity LHC (HL-LHC) because of the intense radiation. This has the added advantage that the optical links would be serviceable. However, the high-speed data signal must be transmitted via low-mass cables ("skinny cables") to a remote location. Unfortunately, the cables

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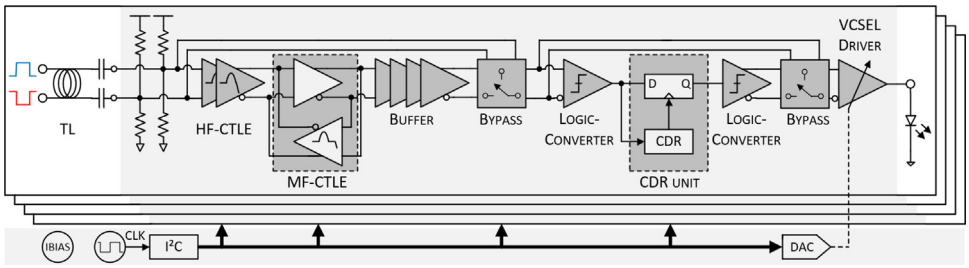

Fig. 2. Block diagram of 4-channel VCSEL driver ASIC. All components outside the shaded area are external.

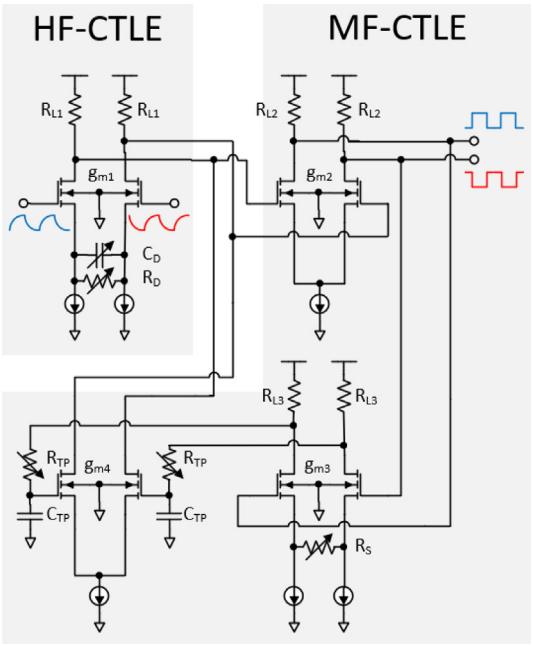

Fig. 3. Schematic diagram of the equalization circuit consisting of high-frequency (HF) and mid-frequency (MF) CTLE.

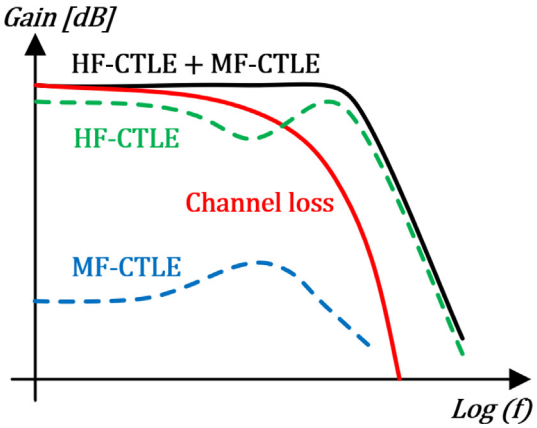

Fig. 4. Illustration how combination of mid-frequency CTLE (MF-CTLE) and high-frequency CTLE (HF-CTLE) could equalize the frequency response to produce a uniform response up to high frequency for a signal emerged from a skinny cable.

severely degrade the data signal, necessitating equalization and clock-data recovery (CDR) circuits in the VCSEL driver to restore the data signal. In this proceeding, we present the design of a 4-channel VCSEL array driver with these circuitries. The ASIC is laid out in such a way to allow three ASICs to be placed side-by-side to drive a 12-channel VCSEL array, resulting in a compact optical engine in order to satisfy the severe space constraint. The design of the VCSEL array driver together with the preliminary result from the measurement will be presented.

2. Electrical vs. optical transmission cables

It is instructive to compare the service requirement of electrical cables vs. optical fibers as this is a major motivation for developing the 12-channel VCSEL driver. We use the electrical cables in the baseline of new ATLAS pixel detector (ITK-Pixel) for the comparison [4]. Fig. 1 shows a comparison of twelve pairs of co-axil electrical cables (TwinAx) vs. a standard 12-fiber ribbon. The cross section of the electrical cables is ten times larger, representing a major challenge in the routing of the electrical and cooling services for the pixel modules. Moreover, the electrical cables with two copper conductor and one copper drain wire and the aluminum outer shield introduce a significant amount of material in the path of the particles emerging from *pp* collision region. The interactions of these particles produce more hits in the downstream detectors, starting with the pixel modules and then the silicon strip modules, the proposed high-granularity timing detector (HGTD), and calorimeters. These extra hits require more data bandwidth in the readout which in turn requires more data links and hence adding more material. This vicious cycle is particularly acute in the high η (forward) region in which particles traverse the cables at high glancing angles, producing many interactions. This motivates us to develop a 12-channel VCSEL driver for a compact optical engine to be mounted at a few hundred centimeters from the interaction region. This also avoid the need to build hundreds of crates ("opto-boxes") to house the optical modules.

3. ASIC design

We have designed a 4-channel VCSEL driver that can be deployed at a few hundred centimeters from the interaction region to reduce the radiation exposure to the coupled VCSEL array. A compact optical engine can be fabricated with three ASICs in parallel to drive a 12-channel VCSEL array. The ASIC can also be fabricated in a 12-channel version to simplify the fabrication of a 12-channel optical engine.

The VCSEL array driver ASIC was designed using the core transistors of the 65 nm CMOS process of TSMC.[1] The core transistors offer the thinnest oxide available and thus the design benefits from the known improvement in total ionizing dose radiation tolerance provided by thinner oxides [5].

The ASICs are designed for two different speeds, 1.28 and 5.12 Gb/s, for possible future applications. At these speeds, the signal from the front-end electronics will be severely degraded after propagating through the skinny cables. The ASIC therefore includes equalizer and clock-data recovery (CDR) circuits to restore the signal after propagating through up to 5 m of 30 AWG TwinAx cables.

A block diagram of the 4-channel VCSEL driver ASIC is shown in Fig. 2. The ASIC is designed to connect to the long skinny cables via

[1] Taiwan Semiconductor Manufacturing Company, Limited.

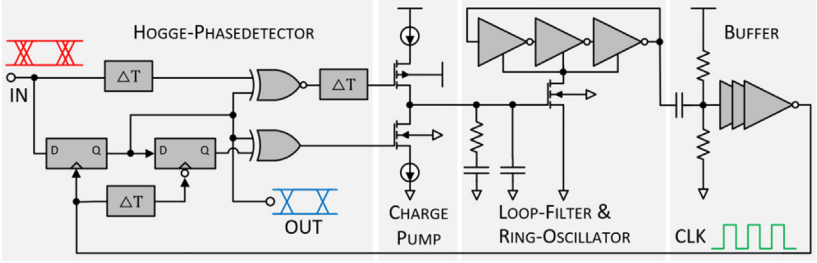

Fig. 5. Clock-data recovery circuit for the recovery of the clock to retime the data stream in order to reduce the clock jitter.

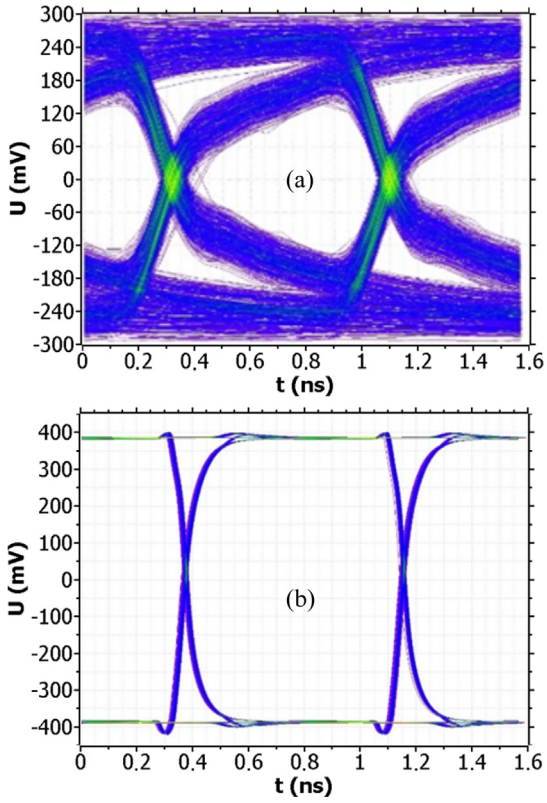

Fig. 6. Eye diagram of a 1.28 Gb/s signal after (a) 5 m of skinny cable and (b) the CDR.

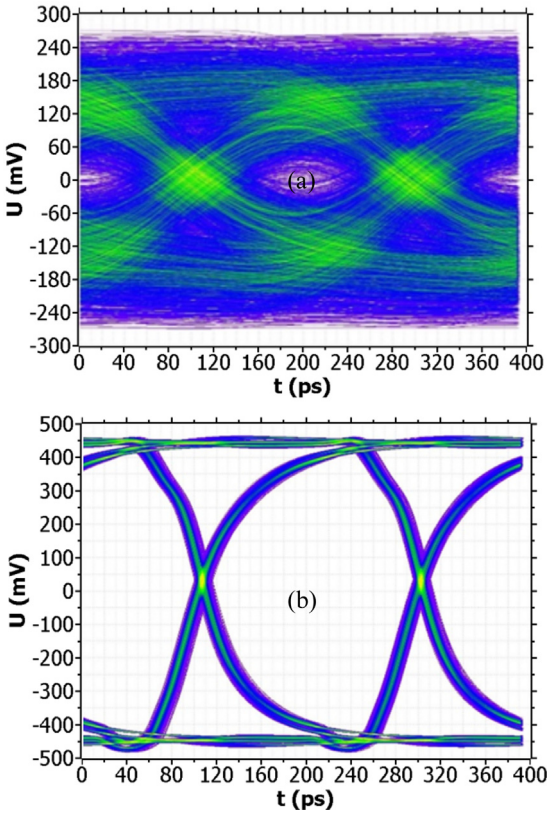

Fig. 7. Eye diagram of a 5.12 Gb/s signal after (a) 5 m of skinny cable (b) and the CDR.

external high broadband capacitors to prevent low frequency jitter. The degradation of the signals due to the frequency dependent power losses in the cables are compensated with two high-frequency (HF) and one mid-frequency (MF) equalizers, using continuous time linear equalization (CTLE) for balancing and increasing the signal bandwidth [6]. The four-stage buffers consist of current amplifiers designed to decrease the amplitude jitter. The logic converter switches the signal from CML to CMOS-levels to control digital logic gates. The CDR recovers the clock to retime the data stream to reduce timing jitter. There are two bypass circuits, allowing verification of the functionality of the equalizers and CDR separately. The bias and modulation currents of the individual channels in the VCSEL array is controlled via a DAC. An I^2C interface with triple redundant memory is used for controlling and adjusting frequency parameter of equalizers and CDR, programming the DACs, and selecting the bypass routes.

The design of the equalization circuit is shown in Fig. 3. A conventional HF-CTLE as shown in Fig. 4 produces a non-uniform response in the mid-frequency range, resulting in higher output jitter. A mid-frequency CTLE is therefore added to compensate for the mid-frequency attenuation.

The architecture of the CDR circuit is shown in Fig. 5. The circuit can operate with data rates of 1.28 or 5.12 Gb/s [7]. The delay elements implemented in the phase detector compensate for the propagation delays of the D flip-flops to eliminate inherent phase distortion. Two loop filter capacitors are charged by a low gain charge pump. In addition, an external loop filter capacitor (not shown, in parallel to the existing one), can be used to further reduce the clock jitter. A voltage controlled low noise ring oscillator (VCO) generates a low jitter clock signal to retime the input data signal. The AC-coupled clock is amplified by three inverter-buffers to decrease signal rise- and fall times.

4. Results from simulation

The post-layout simulation of the ASIC driving a VCSEL incorporates effects of parasitic resistances, capacitances and inductances, including the wire bonds. Results from the AC simulation of the equalizer circuit predict an overall improvement of the signal bandwidth from 200 MHz after the skinny cable to 3 GHz after the equalizer. Fig. 6 shows the eye diagram after the skinny cable and the CDR for 1.28 Gb/s data of PRBS-31 (pseudorandom binary sequence 31) with a string of 2560

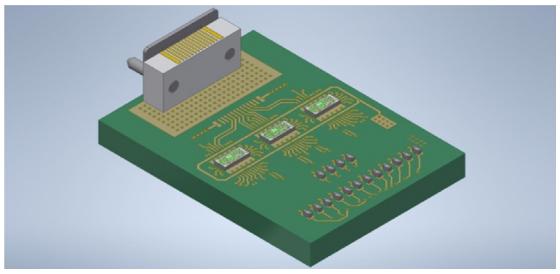

Fig. 8. Rendering of a miniature optical engine with three ASICs driving a 12-channel VCSEL array mounted in an optical package on the upper left-hand corner.

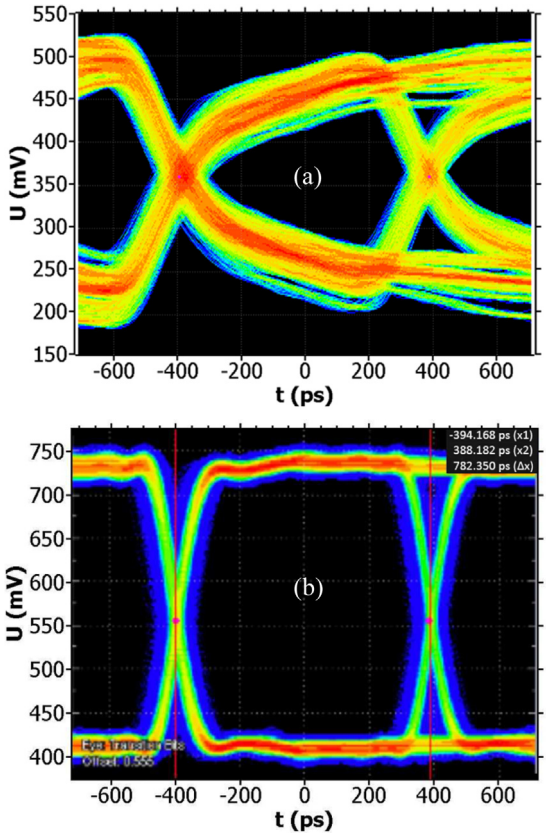

Fig. 9. Measured eye diagram of a 1.28 Gb/s signal (a) at the end of 5 m of skinny cable (b) and after it has been processed by a channel in a prototype ASIC.

bits. The eye after 5 m of skinny cable is somewhat closed with large jitter (total), ± 161 ps for a bit error rate (BER) of 10^{-12}. The jitter is reduced to ± 37 ps after the CDR.

The corresponding eye diagrams for a 5.12 Gb/s signal of PRBS-31 with a string of 10,240 bits transmitted is shown in Fig. 7. The eye after 5 m of skinny cable is completely closed. The eye is opened up after the CDR circuit with a jitter of ± 32 ps.

5. Miniature optical engine

A design of the miniature optical engine is shown in Fig. 8. The board contains three ASICs for driving a 12-channel VCSEL array mounted inside an optical package. The design takes advantage of the experience in fabricating 400 optical modules (opto-boards) [3] for the ATLAS pixel detector. The same optical package is used, based on the experience in fabricating 1700 packages for ATLAS. The fiber ribbon coupled to the optical package is detachable, a major convenience in the testing and installation of the optical modules. The physical dimension of the printed circuit board (PCB) is 1.5 cm x 1.8 cm which can be reduced further when the three ASICs are merged into a 12-channel ASIC.

6. Results from preliminary measurements

We present a preliminary measurement of the ASIC. The ASIC has been tested with an input signal of 1.28 Gb/s generated by a FPGA using Aurora protocol with 64b/66b bit encoding. The signal is sent to the ASIC via 5 m of TwinAx cable. Each channel in the ASIC is measured using an oscilloscope with 50 Ω load and all channels are active during the measurement. Fig. 9 shows the eye diagram of one channel for 1,600,467 transmitted bits. The eye diagram is open with a small jitter, ± 32 ps for a BER of 10^{-12}, somewhat smaller than the expectation from simulation. The ASIC is therefore functional and detailed characterization is in progress.

7. Summary

We have designed a 4-channel VCSEL driver ASIC that can be used in the fabrication of a 12-channel optical engine operating either at 1.28 or 5.12 Gb/s. The ASIC contains equalization and clock-data recovery circuits to restore the highly distorted electrical signal after propagating through several meters of wires of small diameter. The miniature optical engine offers the possibility to greatly reduce detector material in the sensitive region of a silicon tracker. The preliminary measurement indicates that the ASIC is functional and detailed characterization is in progress.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

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