High-Speed/Radiation-Hard Optical Engine for HL-LHC

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Abstract. We have designed and fabricated a compact array-based optical engine for transmitting data at 10 Gb/s. The device consists of a 4-channel ASIC driving a VCSEL (Vertical Cavity Surface Emitting Laser) array in an optical package. The ASIC is designed using only core transistors in a 65 nm CMOS process to enhance the radiation-hardness. The ASIC contains an 8-bit DAC to control the bias and modulation currents of the individual channels in the VCSEL array. The DAC settings are stored in SEU (single event upset) tolerant registers. Several devices were irradiated with 24 GeV/c protons and the performance of the devices is satisfactory after the irradiation.

Keywords: Radiation-hard optical link · High-speed optical link
VCSEL array driver ASIC

1 Introduction

A parallel optical engine is a compact device for high-speed data transmission. The compact design is enabled by readily available commercial high-speed VCSEL arrays. These modern VCSELs are humidity tolerant and hence no hermitic packaging is needed[1]. With the use of a 12-channel array operating at 10 Gb/s per channel, a parallel optical engine can deliver an aggregate bandwidth of 120 Gb/s. With a standard spacing of 250 μm between two adjacent VCSELs, the width of a 12-channel array is only slightly over 3 mm. This allows the fabrication of a rather compact parallel optical engine for installation in locations where space is at a premium. The use of a fiber ribbon also reduces the number of fibers to handle and moreover a fiber ribbon is less fragile than a single-channel fiber. These advantages greatly simplify the production, testing, and installation of optical links.

VCSEL arrays are widely used in off-detector data transmission in high-energy physics [1]. The first implementation [2] of VCSEL arrays for on-detector application is in the optical links of the ATLAS pixel detector. The experience from the operation of this first generation of array-based links has been quite positive. The ATLAS experiment therefore continued to use VCSEL arrays in the second-generation optical

[1] See for example, http://www.photonics.philips.com/.

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links [3] for a new layer of the pixel detector, the insertable barrel layer (IBL), installed in early 2014 during the long shutdown (LS1) to prepare the Large Hadron Collider (LHC) for collisions at the center-of-mass energy of 13 TeV. In addition, ATLAS also decided to move the optical links of the original pixel detector to a more accessible location. The replacement optical links are also array based.

Based on this extensive and positive experience, it is logical for the ATLAS pixel detector of the high-luminosity LHC (HL-LHC) to continue to use optical links based on the opto-board (optical engine) concept. In these proceedings, we report the result of an R&D project on the next generation optical engine operating at high speed.

2 Design of the Opto-Board

The opto-board is a miniature printed circuit board (PCB) as shown Fig. 1. A VCSEL array driver ASIC is mounted on the opto-board next to an opto-pack that houses a VCSEL array. This keeps the length of the wire bonds between the ASIC and the VCSEL array to a minimum to diminish the parasitic capacitance and inductance of the wire bonds. This allows the ASIC to drive the VCSELs at high speed. The PCB has a thick copper back plane (1.0 mm) for thermal management. An MTP[2] barrel attached to an aluminum brace is secured to the opto-board via a screw. A fiber ribbon terminated with a MTP connector can be inserted into the MTP barrel to receive the optical signal from the VCSEL array. An electrical connector[3] is attached to the PCB to transmit high-speed data from a pixel module to the VCSEL array driver ASIC. The high-speed electrical signals from the connector to the ASIC are transmitted using controlled impedance differential pair transmission lines on the PCB.

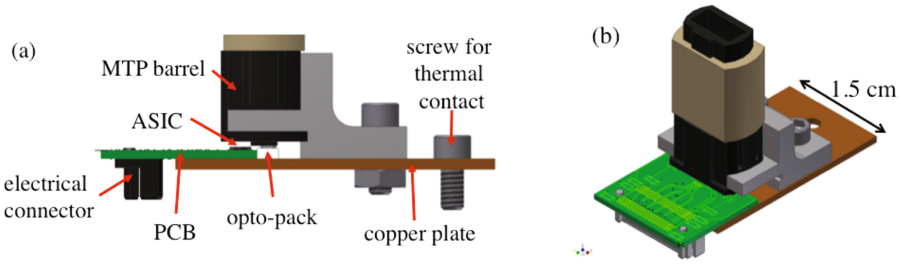

Fig. 1. (**a**) Schematic drawing of an opto-board together with a MTP barrel fastened to the opto-board for the insertion of a fiber ribbon terminated with MTP connector to receive the optical signal from the VCSEL array. (**b**) A three-dimensional rendition of the setup.

[2] MTP connector, US Conec Ltd.

[3] LSHM connector, Samtec Inc.

3 VCSEL Array Driver ASIC

The VCSEL array driver ASIC was developed under the US Collider Detector R&D (CDRD) program of DOE. We have prototyped the ASIC in two runs, both in 4-channel versions, using the 65 nm CMOS process of TSMC[4]. We only use the core transistors of the process in order to achieve maximum radiation tolerance. Both ASICs include an 8-bit DAC to set the VCSEL modulation and bias currents. The DAC settings are stored in SEU (single event upset) tolerant registers. Several improvements were implemented in the second prototype ASIC:

- Eliminated all external biases. All biases are now programmable via DACs. The bias that is distributed across the ASIC is set via a current and then is converted into a voltage at the point of use. This allows faster recovery from the signal switching as there is no large RC constant between the generator of the bias voltage and the point of use as in the previous scheme.
- Added more on-chip decoupling capacitance of $\sim$200 pF for the whole ASIC.
- Eliminated output feedback amplifier to set output level. One of the modes in the circuit of the first prototype ASIC had large impedance and was virtually an open circuit, causing large jitter, instead of driving the bias voltage.
- Added pre-emphasis to the signal at the output of the receiver that received the electrical input signals. The location of the added pre-emphasis is programmable via a delay line.
- Added pre-emphasis and feed through capacitors on the driver block of the ASIC to increase the speed, thereby improving the timing/amplitude control.
- All power lines are tied together with a better power plane. In the first prototype ASIC, each channel has two power pads. In the new ASIC, there are a total of 13 power pads, including some large pads for multiple wire bonds.

4 Results from the First Prototype ASIC

In the first prototype ASIC [4], all four channels are operational and the bit error rate is less than 1.3×10^{-15} with all channels active using pseudo random bit strings (PRBS) as input. Figure 3a shows the optical eye diagram at 10 Gb/s. The eye is open but improvements are needed to reduce the jitter.

The expected radiation level for the optical links depends on the location. For example, if the opto-boards are installed near the outer radius of the endcaps of the silicon tracker ("ID endplates"), the ionizing dose is 10.2 Mrads and the non-ionizing dose is 5.2×10^{14} 1-MeV n_{eq}/cm^2. In October 2015, we irradiated eight opto-boards with prototype ASICs using 24 GeV/c protons at the CERN PS irradiation facility. In four opto-boards, each ASIC drove a resistive load while in the other four opto-boards, each ASIC drove a VCSEL array[5]. The opto-boards with VCSEL arrays attached were

[4] Taiwan Semiconductor Manufacturing Company, Limited.

[5] The VCSEL array used is V850-2174-002, fabricated by Finisar Corporation.

exposed to a dose of 4.58×10^{14} protons/cm^2, corresponding to an ionizing dose of 12.2 Mrads and a non-ionizing dose of 2.69×10^{14} 1-MeV n_{eq}/cm^2, assuming that the radiation damage in the VCSEL scales with the non-ionizing energy loss (NIEL) in the GaAs [5, 6]. The opto-boards containing no VCSELs were exposed to a dose of 2.78×10^{15} protons/cm^2, corresponding to an ionizing dose of 74.0 Mrads.

All ASICs were powered and monitored during the irradiation but at reduced speeds because it was not practical to install high-speed cables at the irradiation facility. The opto-boards with VCSEL arrays were periodically removed from the proton beam to allow the annealing of the VCSELs that occurred naturally when powered. All channels were operational at the end of the irradiation. The optical eye diagram of one channel after irradiation is compared to that before irradiation in Fig. 2 for 10 Gb/s operation. The optical amplitude decreases from 2.07 to 1.19 mW. The opening of optical eye diagram is smaller but the device still operates error free for more than 30 min, corresponding to a bit error rate, BER $<5 \times 10^{-14}$, with all channels active. Figure 3 shows a comparison of the corresponding optical eye diagrams for 5 Gb/s operation, the expected data transmission speed of the ATLAS pixel detector at HL-LHC. The eyes are open both before and after irradiation. This is the first demonstration of the radiation hardness of an array driver/VCSEL combination operating at 10 Gb/s with a dose of greater than 10 Mrads.

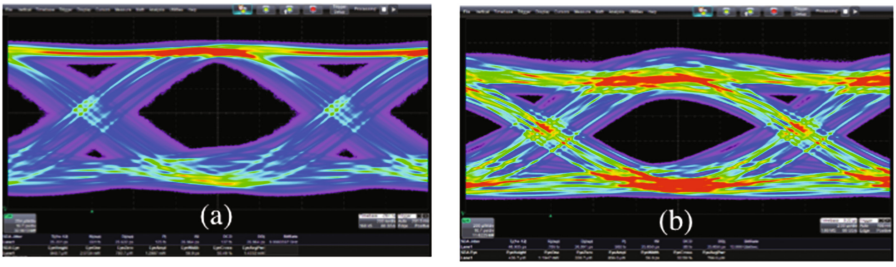

Fig. 2. Optical eye diagram of a VCSEL operating at 10 Gb/s before (**a**) and after (**b**) irradiation.

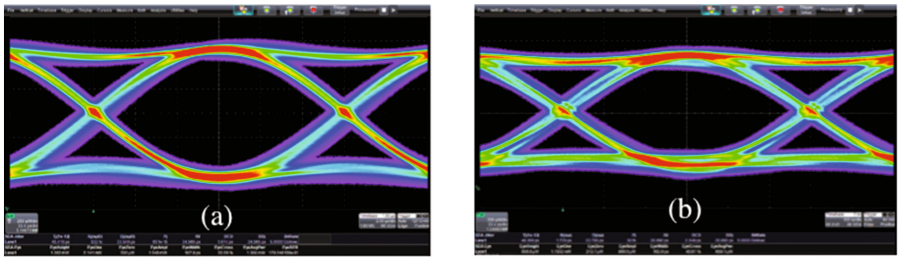

Fig. 3. Optical eye diagram of a VCSEL operating at 5 Gb/s before (**a**) and after (**b**) irradiation.

5 Results from the Second Prototype ASIC

The second prototype ASIC is much easier to tune for operation at 10 Gb/s because of the various improvements listed in Sect. 4. The supply voltage of the ASIC is 1.2 V and the current consumption is 150 mA with all four channels operating at 10 Gb/s. The common cathode voltage is set at −1.3 V in order to provide enough headroom to drive the VCSEL. The current consumption of the common cathode voltage is 25 mA. All channels have excellent coupled optical power, higher than 2 mW. The optical eye diagram is shown in Fig. 4a for 10 Gb/s operation. In comparison with Fig. 2a, the eye is more open but there is significant jitter and this is being investigated. The BER is $<5 \times 10^{-14}$ on all channels with every channel active. Figure 4b shows the optical eye diagram operating at 5 Gb/s, the target data transmission speed of the ATLAS pixel detector at HL-LHC. The eye is wide open, indicating satisfactory performance.

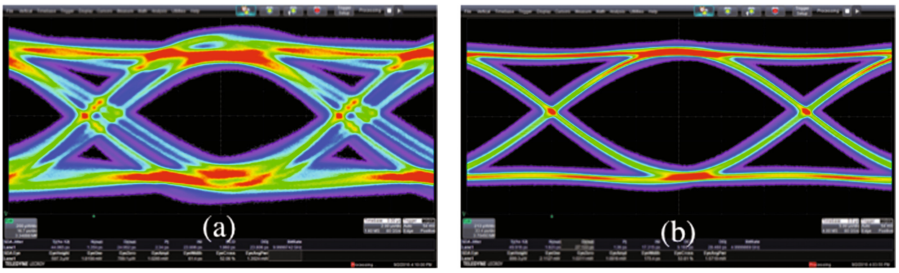

Fig. 4. Optical eye diagram of a VCSEL in the second prototype ASIC operating at 10 (**a**) and 5 (**b**) Gb/s.

6 Conclusions

We have designed and fabricated a new opto-board including an array driver ASIC and optical packaging to allow 10 Gb/s optical data transmission. The ASIC can operated at 10 Gb/s after irradiation (> 10 Mrads). The plan is to further improve the design of the ASIC for application in the ATLAS pixel detector at HL-LHC.

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