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Optical link ASICs for LHC upgrades

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We have designed several ASICs for possible applications in a new ATLAS pixel layer for the first phase of the LHC luminosity upgrade. The ASICs include a high-speed driver for the VCSEL, a receiver/decoder to decode the signal received at the PIN diode to extract the data and clock, and a clock multiplier to produce a higher frequency clock to serialize the data for transmission. These chips were designed using a 130 nm CMOS process to enhance the radiation-hardness. We have characterized the fabricated chips and the submission has been mostly successful. We irradiated the chips with 24 GeV/c protons at CERN to a dosage of 70 Mrad. We observed no significant degradation except the driver circuit in the VCSEL driver fabricated using the thick oxide process in order to provide sufficient voltage to drive a VCSEL. The degradation is due to the large threshold shifts in the PMOS transistors used.

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[1] Speaker

1.Introduction

The Large Hadron Collider (LHC) at CERN will be upgraded in two phases, resulting in ten time higher luminosity. The detectors are expected to be exposed to a similar increase in radiation. We have designed several ASICs for possible applications in a new pixel layer for the ATLAS experiment in the first phase of the luminosity upgrade. The ASICs were fabricated using a 130 nm CMOS 8RF process [1] and include two VCSEL drivers (640 Mb/s and 3.2 Gb/s), a PIN receiver with a clock and data recovery circuit capable of operation at 40, 160, or 320 Mb/s, and two clock multipliers designed to operate at 640 Mb/s. The clock multiplier is needed to produce a higher frequency clock to serialize the data for transmission. All circuitry within the test chip was designed following test results and guidelines from CERN on radiation tolerant design for the process used [2]. We summarize below the results from the characterization, including the irradiation with 24 GeV protons at CERN. All chips tested were packaged for the irradiation and therefore we experienced some speed degradation due to the added stray capacitance of the packaging.

2.VCSEL driver chip

The two VCSEL driver chips have similar architecture, one optimized for 640 Mb/s with higher drive current and the other for 3.2 Gb/s with lower current. Each consists of a 1.5 V LVDS receiver circuit, a 1.5 to 2.5 V logic converter circuit, and a 2.5 V VCSEL driver circuit. Both VCSEL drivers allow for adjustable bias and modulation currents and contain circuitry to reduce switching noise on the power supply lines. We used a 2.5 V supply for the driver circuitry because most commercially available VCSELs require bias voltages greater than 2 V to produce suitable output optical power. The driver portion of the chips was therefore designed using the thick oxide transistors instead of thin oxide transistors for all other circuits. Previous results from CERN have shown that thin oxide transistors designed using conventional layout techniques exhibit radiation tolerance suitable for SLHC applications. However, conventionally designed thick oxide transistors are not suitably radiation tolerant. All of the thick oxide transistors were therefore designed using an enclosed structure.

The performance of the four packaged chips was satisfactory up to 1 Gb/s. The performance at higher speeds could not be sufficiently evaluated due to the packaging parasitics. In the irradiation, each chip was connected to a 25 Ω resistor instead of a VCSEL to allow testing of the degradation of the chip alone. The duty cycle of the output signal and the current consumption of the LVDS receiver remained constant during the irradiation. However, we observed significant decrease in the current consumption of the VCSEL driver circuit and the output drive current. Post-irradiation analysis of the IV characteristic of a PMOS transistor fabricated in the thick oxide technology indicates a significant threshold shift and the effect can be emulated in a simulation. The shift is significantly smaller in the NMOS transistors. The present current mirror in the driver circuit uses both types of transistors and thus is sensitive to the different threshold shifts. The plan is to use PMOS transistors only in the future design.

3.PIN receiver and decoder chip

The PIN receiver/decoder contains a trans-impedance amplifier, limiting amplifier, bi-phase mark (BPM) decoder with clock recovery, and LVDS drivers to send the decoded data and recovered clock off chip. The clock and data are recovered using a delay locked loop with networks of switchable capacitors in the delay stages allow for the three operating frequencies, 40, 160, and 320 Mb/s. However, due to insufficient time to optimize the design, the chips operate at somewhat lower speed and require higher threshold currents to achieve a low bit error rate (BER). Other than these two limitations, the performance of the chips is satisfactory, including clock jitter, duty cycle, rise/fall time, and high/low levels of the LVDS drivers.

For the irradiation, four chips were tested in each of the two setups, one was purely electrical and the other involved a PIN diode so that we could decouple the electrical and optical degradations. The decoded data were transmitted to the control room using 20 m of coax. In the first setup, 40 Mb/s BPM signals were transmitted over 20 m of coax to the chips. In the second setup, we sent 40 Mb/s BPM signal via a fiber to a PIN diode coupled to a chip. We observed single event upset during the spill but observed no degradation in the threshold for ~1 error/s. The BER decreased with larger PIN current and was higher for a chip coupled to a PIN diode as expected. The current consumption was constant during the irradiation.

4.Clock multiplier

The clock multiplier circuits on the test chip consist of charge pump/ring oscillator phase locked loops (PLL) with dividers in the feedback loop. One circuit performs a frequency multiplication of 16 and the other a multiplication by 4, both yielding a 640 MHz clock. All four multipliers packaged for the irradiation functioned well with clock jitter of < 8 ps or 0.5%. During the irradiation, we observed that the clocks of two chips lost lock and power cycling was needed to resume operation at 640 MHz. This problem is not yet understood.

5.Summary

We have designed prototype ASICs using the 130 nm process to enhance the radiation-hardness. We observed no significant performance degradation up to a dose of 70 Mrad except in the VCSEL driver. This is due a large threshold shift in the PMOS transistors fabricated in the thick oxide technology for the operation at 2.5 V to drive the VCSEL.

6.Acknowledgement

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References

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