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Radiation-Hard/High-Speed Parallel Optical Links

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Abstract

We have designed and fabricated a compact parallel optical engine for transmitting data at 5 Gb/s. The device consists of a 4-channel ASIC driving a VCSEL (Vertical Cavity Surface Emitting Laser) array in an optical package. The ASIC is designed using only core transistors in a 65 nm CMOS process to enhance the radiation-hardness. The ASIC contains an 8-bit DAC to control the bias and modulation currents of the individual channels in the VCSEL array. The performance of the optical engine up at 5 Gb/s is satisfactory.

Keywords: HL-LHC; optical-link; VCSEL array driver; radiation-hard;

1. Introduction

A parallel optical engine is a compact device for high-speed data transmission. The compact design is enabled by readily available commercial high-speed VCSEL arrays. These modern VCSELs are humidity tolerant and hence no hermitic packaging is needed [1]. With the use of a 12-channel array operating at 10 Gb/s per channel, a parallel optical engine can deliver an aggregate bandwidth of 120 Gb/s. With a standard spacing of 250 μm between VCSELs, the width of a 12-channel array is only slightly over 3 mm. This allows the fabrication of a rather compact parallel optical engine for installation in locations where space is at a premium. The use of a fiber ribbon also reduces the number of fibers to handle and moreover a fiber ribbon is less fragile than a single-channel fiber. These advantages greatly simplify the production, testing, and installation of optical links.

VCSEL arrays are widely used in off-detector data transmission in high-energy physics [2]. The first implementation [3] of VCSEL arrays for on-detector application is in the optical links of the ATLAS pixel

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detector. The experience from the operation of this first generation of array-based links has been quite positive. In particular, the failure rate of the optical links fabricated by The Ohio State University is ~0.1% [4]. The ATLAS experiment therefore continues to use VCSEL arrays in the second-generation optical links [5] for a new layer of the pixel detector, the insertable barrel layer (IBL), installed in early 2014 during the long shutdown (LS1) to prepare the LHC for collisions at the center-of-mass energy of 13 TeV. In addition, ATLAS also decided to move the optical links of the original pixel detector to a more accessible location. The replacement optical links are also array based.

The optical modules (optical engines or opto-boards) for the two generations of optical links for the ATLAS pixel detector are similar in design. However, there are several improvements in the second-generation opto-boards [5] to increase the reliability of the opto-board and simplify the fabrication procedure. In particular, the optical package (opto-pack) has a much more robust design [6]. About 400 opto-boards were fabricated, corresponding to about 6,000 uplinks (from the pixel detector up to the counting room) and 3,000 downlinks (from the counting room down to the pixel detector). The links are operated at 40-160 Mb/s.

Based on this extensive and positive experience, it is logical for the ATLAS pixel detector of the HL-LHC to continue to use optical links based the opto-board concept. In these proceedings, we report the result of an R&D project on the next generation optical engine operating at high speed.

2. Design of the Opto-Board

The opto-board is a miniature printed circuit board (PCB). Figure 1 shows a drawing of the opto-board. A VCSEL array driver ASIC is mounted on the opto-board next to an opto-pack. This keeps the length of the wire bonds between the ASIC and the VCSEL array to a minimum to minimize the parasitic capacitance and inductance of the wire bonds. This allows the ASIC to drive the VCSELs at high speed. The PCB has a thick copper back plane (1.0 mm) that can be fastened with a screw to a heat sink to remove the heat generated by the ASIC and VCSEL array. The heat sink can be a copper rail with tube in the center for the passage of coolant. An MTP barrel attached to an aluminum brace is fixed to the opto-board via a screw. A fiber ribbon terminated with a MTP connector can be inserted into the MTP barrel to receive the optical signal from the VCSEL array. The spring-loaded MTP connector is widely used in the optical communication industry due to its ease of use. An electrical connector [7] is attached to the PCB to transmit high-speed data to the VCSEL array driver ASIC. Due to their high speeds, the electrical signals from the connector to the ASIC are transmitted using controlled impedance differential pair transmission lines.

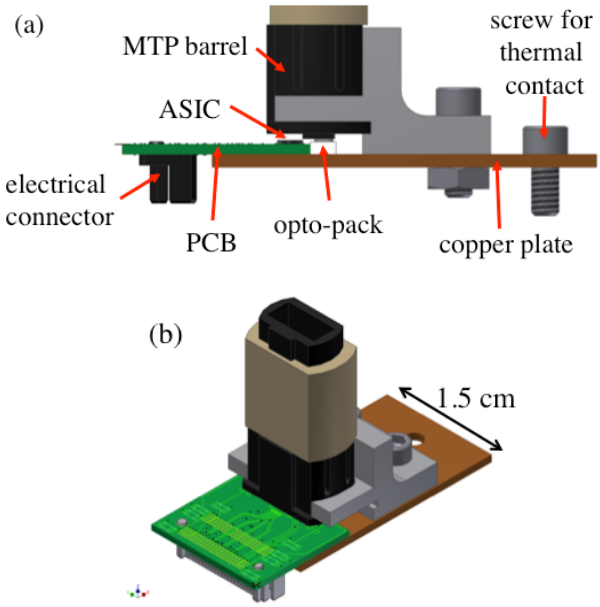

Figure 1: (a) Schematic drawing of an opto-board together with a MTP barrel fastened to the opto-board for the insertion of a fiber ribbon terminated with MTP connector to receive the optical signal from the VCSEL array. (b) A three-dimensional rendition of above setup.

3. Design of the Opto-Pack

We have designed an opto-pack that is similar to that used in the second-generation opto-boards for two reasons [6]. First the opto-pack has a simple design and is easy to handle. Second we have extensive experience in fabricating the opto-packs, 1,200 pieces for the second-generation opto-boards. In addition, we have also fabricated 280 opto-packs for the off-detector opto-receivers (RXs). In total, our production volume is equivalent to 18,000 channels.

The opto-pack consists of a small BeO block mounted with one optical array and two guide pins as shown in Fig. 2. The design is similar to the opto-pack used in the second-generation opto-boards but with a simplification. The traces for connecting to the common cathode of a VCSEL array are replaced by a plane of solid metal. The BeO substrate is also shorter to minimize the length of the wire bonds between the VCSEL array and the driver ASIC, critical for high-speed data transmission. The two guide pins have their relative position defined by a MT ferrule and fixed with epoxy. The VCSEL array is aligned with respect to the two guide pins to a precision of a few microns. Details of the assembly procedure are given in Ref. [6].

4. VCSEL Array Driver ASIC

The VCSEL array driver ASIC is a product of the US Collider Detector R&D (CDRD) program of DOE. This is an R&D program to design a 12-channel VCSEL array driver ASIC for operation at 10 Gb/s. The ASIC used in this opto-board prototype is a 4-channel version from the first prototype run. The test chip was fabricated in October 2014 using the 65 nm CMOS process of TSMC [8]. The ASIC has a dimension of 2 mm x 2 mm. Each channel of the ASIC has a slightly different design in order to explore different design choices. We only use the core transistors of the process in order to achieve maximum radiation tolerance. The ASIC includes an 8-bit DAC to set the VCSEL modulation and bias currents. The DAC settings are stored in SEU (single event upset) tolerant registers. All four channels are operational and the bit error rate is less than 1.3 x 10^{-15} with all channels active using pseudo random bit strings (PRBS) as input. Figure 3 shows the optical eye diagram at 10 Gb/s. The eye is open but improvements are needed to reduce the jitter. However, the ASIC is quite adequate for operation at 5 Gb/s as required for the pixel detector of the ATLAS experiment at HL-LHC.

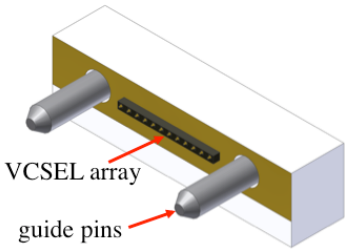

Figure 2: Schematic drawing of an opto-pack. The distance between the two guide pins is 4.6 mm.

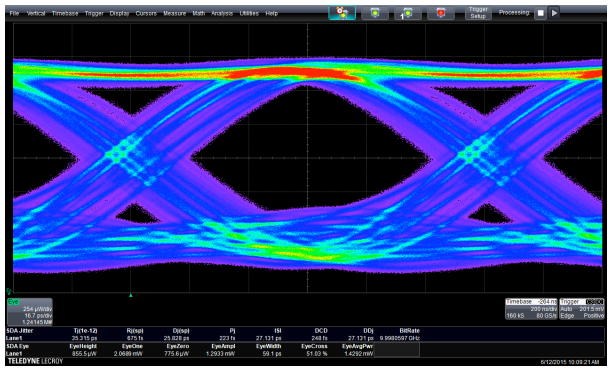

Figure 3: Optical eye diagram of a VCSEL channel coupled to a driver ASIC operating at 10 Gb/s.

5. Results from the Prototype

The miniature opto-board has been prototyped. Figure 4 shows a picture of the opto-board with an MTP connector attached. A top view of the opto-board is shown in Fig. 5(a). A zoom-in view focusing on the ASIC and the VCSEL array on an opto-pack is shown in Fig. 5(b). The VCSEL array contains 12 channels [9]. It is evident that the opto-board design is readily scalable to 12 channels by replacing the ASIC.

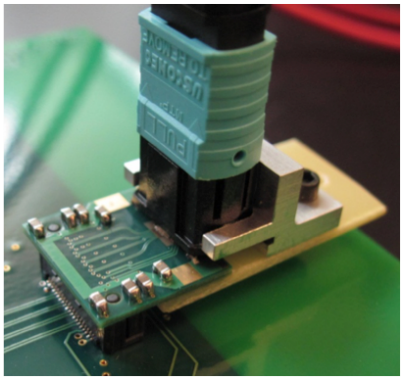

Figure 4: Opto-board with an MTP connector attached.

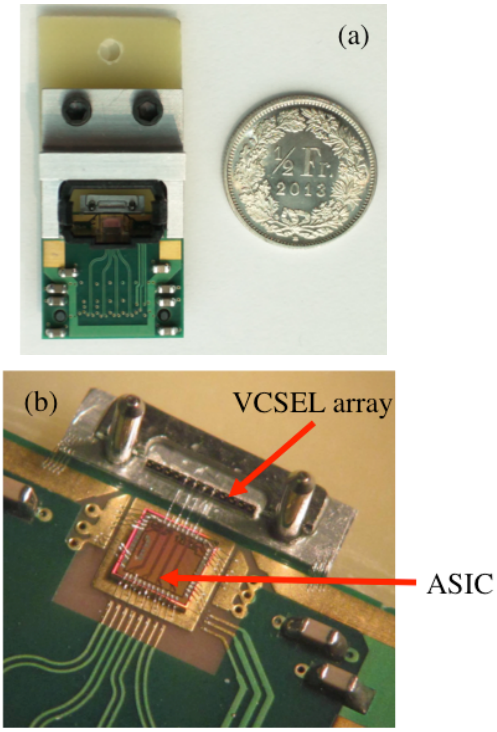

Figure 5: (a) Top view of an opto-board. (b) A zoom-in view showing the placement of the ASIC with respect to the VCSEL array between the two guide pins on an opto-pack.

High-speed electrical signals (data) will be transmitted via a back plane in the opto-box and then through the mating connector on the opto-board to the ASIC. Figure 6

shows a prototype version of the back plane. Each pair of SMA connectors receives CML (Current-Mode Logic) signals and these signals then propagate along the controlled impedance differential pair transmission lines to the connector that mates with the connector on the opto-board. On the back plane, the differential pairs have 175 μm trace widths and spacing. On the opto-board, the pairs have smaller feature size, 125 μm width and space, in order to match the separation of 250 μm between two VCSELs. In an actual experiment, the back plane will be kept as small as possible and more compact multi-channel connectors will be used instead of the SMA connectors.

The supply voltage of the ASIC is 1.2 V and the current consumption is 150 mA with all four channels operating at 5 Gb/s. The common cathode voltage is set at -1.3 V in order to provide enough headroom to drive the VCSEL. The current consumption of the common cathode voltage is ~20 mA.

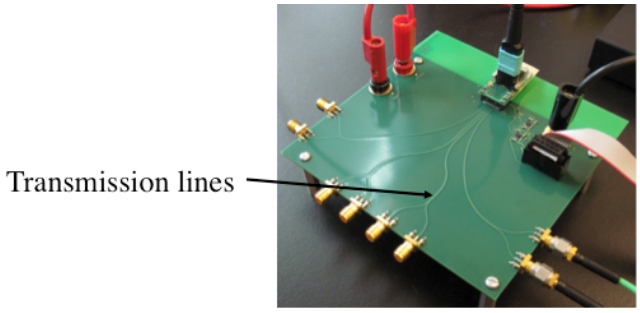

Figure 6: An emulator of the back plane of the opto-box for sending high-speed electrical signals to the opto-board.

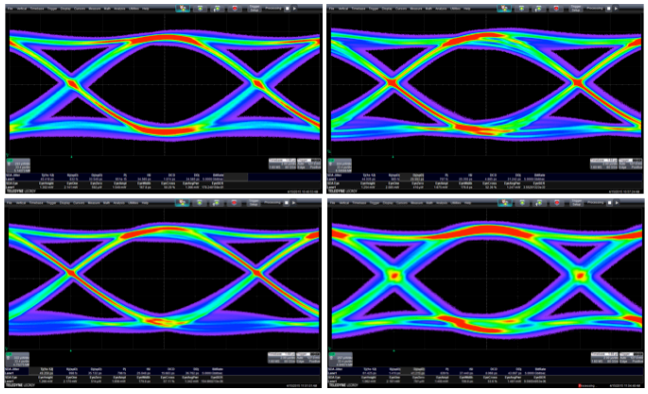

Figure 7: Optical eye diagrams of all four channels on the opto-boards operating at 5 Gb/s.

All channels have excellent coupled optical power, better than 2 mW. Figure 7 shows the optical eye diagrams of the four channels with all channels active at 5 Gb/s. The eye diagram is quite open. The bit error rate is less than 1 x 10^{-13} with all channels active. This prototype study demonstrates that it is possible to send high-speed electrical signals via a connector to the opto-board, avoiding the need to connect the high-speed cables directly to the opto-board. This greatly simplifies the logistics of testing and installation. The opto-board therefore satisfies the need of the pixel detector of the ATLAS experiment at HL-LHC.

We expect the optical engine to be radiation hard but this remains to be verified. We plan to irradiate the circuitry with 24 GeV protons at CERN in October 2015.

6. Conclusions

A high-speed parallel optical engine has been successfully designed and prototyped for the pixel detector of the ATLAS experiment at HL-LHC. The components tested include the VCSEL array driver ASIC and the optical package. The performance for optical data transmission at 5 Gb/s is satisfactory. The optical engine is expected to be radiation hard and the radiation hardness will be verified.

Acknowledgement

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[7] LSHM connector, Samtec Inc.
[8] Taiwan Semiconductor Manufacturing Company, Limited.
[9] The VCSEL array used is V850-2174-002, fabricated by Finisar Corporation.