

# Radiation-hard ASICs for optical data transmission in the first phase of the LHC upgrade

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We have designed two ASICs for possible applications in the optical links of a new layer of the pixel detector to be install inside the ATLAS Pixel detector for the first phase of the LHC luminosity upgrade. The ASICs include a high-speed driver for a VCSEL and a receiver/decoder to decode the signal received at a PIN diode to extract the data and clock. Both ASICs contain 4 channels for operation with a VCSEL or PIN array. The ASICs were designed using a 130 nm CMOS process to enhance the radiation-hardness. We have characterized the fabricated ASICs and the performance of the ASICs is satisfactory. The receiver/decoder properly decodes the bi-phase marked input stream with low PIN current and the driver can operate a VCSEL up to  $\sim 5$  Gb/s. The added functionalities are also successful, including redundancy to bypass a broken VCSEL or PIN channel, individual control of VCSEL current, and power-on reset circuit to set all VCSEL currents to a nominal value.

## 1. Introduction

The Large Hadron Collider (LHC) at CERN, Geneva, Switzerland, will be upgraded in two phases to increase the luminosity. The ATLAS experiment plans to add a new pixel layer inside the current pixel detector during the first phase of the upgrade. The optical data transmission will also be upgraded to handle the high data transmission speed. The upgrade for the on-detector optical links will be based on VCSEL and PIN arrays operating at 850 nm as in the current system. Two ASICs have been designed for this new generation of optical links to incorporate the experience gained from the current system.

The ASICs [1] have been designed using 130 nm 8RF-DM CMOS process. The driver couples to a VCSEL array with one channel designated as a spare. Similarly for a receiver/decoder couples to a PIN array. With the inclusion of a remote control interface, this allows redundancy in both directions by enabling a signal to be re-routed from a bad VCSEL or PIN channel. The submitted chip contains four VCSEL drivers (VDC), four PIN diode receivers/decoders (Digital Opto-Receiver Integrated Circuit or DORIC), and the associated circuitry to control the re-routing of the signals to the designated spare channels. All circuitry within the test chip was designed following test results and guidelines from

CERN on radiation tolerant design in the 130 nm process used [2]. We have characterized the fabricated ASICs and the results will be presented below.

## 2. DORIC

Each of the DORIC contains a PIN diode receiver, a bi-phase marked (BPM) clock/data recovery circuit, and has low voltage differential signal (LVDS) outputs for both the clock and data. All four DORICs are designed to operate with a 1.5 V power supply and a 40 Mb/s BPM input stream. One of the DORICs includes circuitry to extend its operational speed to 80, 160, or 320 Mb/s. Two-channel multiplexers have been inserted in the post amplification paths of the non-spare DORIC channels. With these multiplexers, the signal from the spare amplifier channel may be routed to the channel of choice. A block diagram of the DORIC section of the chip is shown in Figure 1.

In order to allow remote control over channel steering and other functionality within the chip, a command decoder has been included in three of the DORICs. The command decoder was designed for the front-end chips of the new pixel layer. Because the chips will be resided in a high radiation environment, special care was taken to improve the single event upset tolerance of the command decoder. The command word for configuring the

chip is formed by a majority vote of the three command decoders. To further improve our chip's tolerance to single event upsets, all latches in our design are based on a dual interlocked storage cell (DICE) latch designed for use in the configuration memory of the front-end chips of the pixel detector.

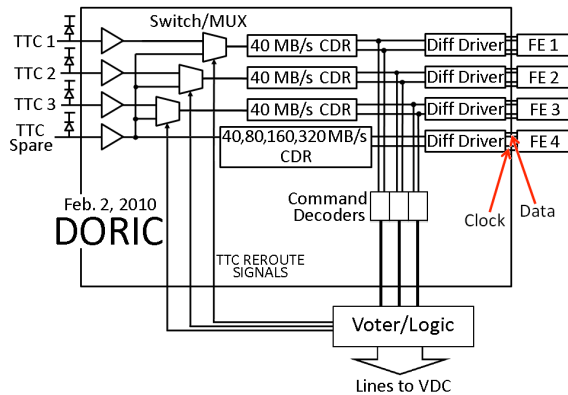


Figure 1. DORIC block diagram. In the final design, there will be one less output than input, i.e. if one the PIN diode malfunctions, the optical signal will be transmitted via the spare PIN to the original FE channel.

To simplify some of the testing and to allow verification of the command decoder's operation, we have included a serially interfaced test port to the command word. Figure 2 shows a block diagram of the interface.

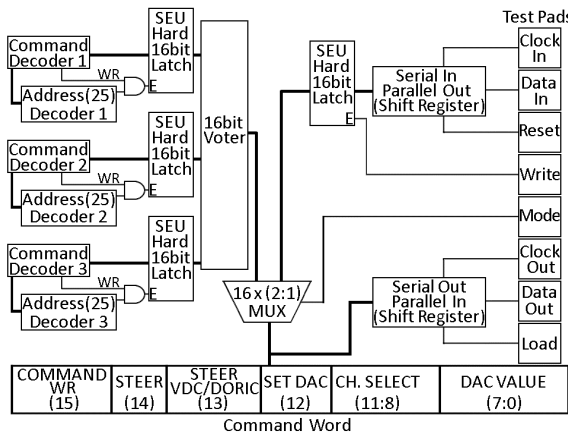


Figure 2. There are two interfaces for loading the 16-bit word needed for the ASIC operation: the command decoder interface on the left or the test port on the right.

All four DORIC channels can properly decode the data at 40 Mb/s with no bit errors for low input PIN currents,  $\sim 20 \mu\text{A}$  for the three single-speed channels and  $\sim 40 \mu\text{A}$  for the multi-speed channel. For the multi-speed channel, the threshold is higher at faster speed, from  $\sim 60 \mu\text{A}$  at 80 Mb/s to  $\sim 100 \mu\text{A}$  at 320 Mb/s. The cause for the higher thresholds is currently under investigation. The clock jitter (peak-to-peak) at 40 Mb/s is  $\sim 1.4 \text{ ns}$  for both single-speed and multi-speed channels. For the multi-speed channel, the jitter is smaller at higher operating speed, as little as  $\sim 100 \text{ ps}$  at 320 Mb/s. It should be noted that the multi-speed channel requires external bias tuning for proper operation at 160 and 320 Mb/s due to the limited dynamic range of the clock duty cycle control circuitry and further improvement is needed in the next submission. The steering circuit functions properly, i.e. signal received at the spare DORIC channel can be rerouted through the other DORIC channels. However, this can only be excised via the test port because the scan chain enable of the command decoder was left floating due to a miscommunication with the designer of the command decoder.

### 3. VDC

The four VDC channels are designed to operate at speeds up to 5 Gb/s. Each channel has an LVDS receiver, an 8-bit DAC, and a driver stage for converting the received LVDS signal into a current sufficient to drive a VCSEL. Two of the four VDC channels provide the capability to add a pre-emphasis current to the VCSEL modulation current. The duration of the pre-emphasis current pulse and its amplitude are adjustable via wire-bond pads. One of the VDC channels is designated as the spare channel and contains a 16:1 multiplexer. The multiplexer allows routing of the received LVDS signal from any of the other three channels to the spare channel output. A block diagram of the VDC portion of the test chip is shown in Figure 3.

The 8-bit DAC and LVDS receiver are designed to operate with a 1.5 V supply and the driver stage is designed to operate with a 2.5 V power supply. A higher supply voltage is required by the output stage to allow enough headroom to drive VCSELs which normally have threshold voltages of  $\sim 2 \text{ V}$ . The output driver is capable of delivering 12 mA modulation current and up to 4 mA bias current if driving a VCSEL with a 2 V threshold voltage.

The 8-bit DAC is used to set the VCSEL modulation current. The setting of each DAC is accomplished by sending appropriate commands to the command decoders in the DORIC. To enable operation in case of a failure in the communication link to the command decoder, we have included a power-on reset circuit that will set the VCSEL modulation current to 10 mA upon power up. Furthermore, we have included a test mode that allows bypassing of the DAC to directly set the modulation current via a wire bond pad. This functionality will not be implemented in final design.

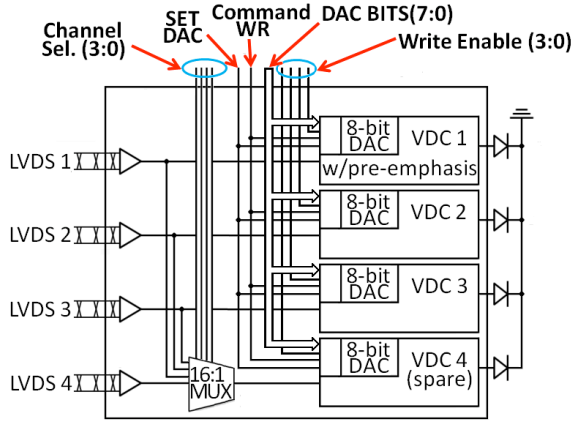


Figure 3. VDC block diagram. In the final design, there will be one less input than output, i.e. if one of the VCSELs malfunctions, the LVDS signal will be transmitted via the spare VDC/VCSEL.

In the prototype VDC, the power-on reset circuit functions properly, supplying a VCSEL modulation current of  $\sim 10$  mA upon power up. We can steer the signal received via the test port to the spare VDC/VCSEL. In addition, we can set the DAC to control individual VCSEL currents. All four channels run error free at 5 Gb/s with bit error rate of  $< 5 \times 10^{-13}$ , including the spare channel with the signal routed from the other LVDS inputs. Figure 4 shows the eye diagrams of the optical signal in one channel and the signal routed from a spare channel. It is evident that the eye is “open” although more improvement is desirable to expend the operation margin.

#### 4. Summary

We have successfully fabricated 4-channel driver and receiver ASIC arrays in the 130 nm process for

use in the optical link upgrade. The receiver can properly decode the bi-phase marked input stream with low PIN current and the driver can operate a VCSEL up to  $\sim 5$  Gb/s. The added functionalities are also successful, including redundancy to bypass a broken VCSEL or PIN channel, individual control of VCSEL current, and power-on reset circuit to set all VCSEL currents to a nominal value.

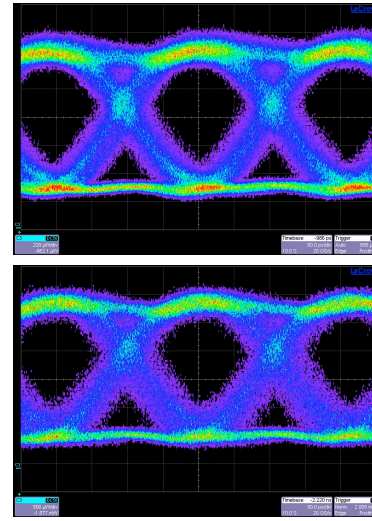


Figure 4. Eye diagram of the optical signal in a VDC channel (top) and the signal routed via a spare channel (bottom). The signal is measured with a 4.5 GHz optical probe.

#### ACKNOWLEDGEMENTS

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