

10 Gb/s Radiation-Hard VCSEL Array Driver

K.K. Gan, P. Buchholz, S. Heidbrink, H. Kagan, R. Kass, J. Moore, D.S. Smith, M. Vogt, M. Ziolkowski

Abstract—We present an R&D program to develop an ASIC that contains a 12-channel VCSEL (Vertical Cavity Surface Emitting Laser) array driver operating at 10 Gb/s per channel, yielding an aggregated bandwidth of 120 Gb/s. The design of the 10 Gb/s array driver ASIC is based on a prototype ASIC for driving a VCSEL array at 5 Gb/s. We will briefly describe the design of the 5 Gb/s ASIC that was fabricated in a 130 nm CMOS process. Two ASICs were irradiated with 800 MeV protons to a dose of 0.92×10^{15} 1-MeV n_{eq}/cm^2 and remain operational. For the 10 Gb/s VCSEL array driver ASIC, we have submitted for fabrication a four-channel test chip using a 65 nm CMOS process. The circuit design together with the result from a simulation of the extracted layout with parasitic capacitance and inductance will be presented.

I. INTRODUCTION

The Large Hadron Collider (LHC) at CERN (Geneva) is now the highest energy and luminosity collider in the world. To further enhance the physics potential, the LHC will be upgraded to even higher luminosity. The detectors will be upgraded in tandem to fully exploit the new physics potential. The optical data transmission system will thus need to be upgraded to handle the higher data transmission speed.

Commercial VCSEL arrays capable of operation at 10 Gb/s are now readily available. A 12-channel VCSEL array offers a compact and robust solution for data transmission. With individual VCSELs operating at 10 Gb/s, the total aggregated bandwidth is 120 Gb/s per fiber ribbon. In previous studies, these commercial VCSEL arrays have been proven to be sufficiently radiation-hard [1]. Therefore, we will design a VCSEL array driver ASIC with sufficient radiation hardness to survive in challenging HEP deployments.

We will present results from an R&D project to produce a radiation-hard VCSEL driver ASIC capable of 10 Gb/s operation per channel. As a first step in this direction, we have designed a VCSEL array driver ASIC for operation at 5 Gb/s. The prototype ASIC was fabricated in a 130 nm CMOS process. We will briefly describe the design and present the result after an irradiation with 800 MeV protons to a dose of 0.92×10^{15} 1-MeV n_{eq}/cm^2 . This will be followed by a description of the

design for a 10 Gb/s VCSEL array ASIC. A 4-channel version of the ASIC will first be fabricated in a 65 nm CMOS process before expanding to 12 channels. We will present the circuit designs together with results from a simulation of the extracted layout with parasitics included.

II. RESULTS FROM A 5 GB/S VCSEL ARRAY DRIVER

We have successfully designed a VCSEL array driver ASIC to operate at speeds up to 5 Gb/s [2]. The ASIC was fabricated in a 130 nm CMOS process to enhance the radiation-hardness. Each ASIC contains eight low voltage differential signal (LVDS) receivers to receive the data from the front-end electronics [3]. The received LVDS signal is converted in the driver stage into a current sufficient to drive a VCSEL. The amplitude of the modulation current in each driver is controlled via an 8-bit DAC. There is also a single 8-bit DAC to set the bias currents of all channels simultaneously. In addition, there are four spare drivers with associated 8-bit DACs that can receive the LVDS signal from any of the eight LVDS receivers via a switching network. This allows the received LVDS signal to be transmitted via one of the four spare VCSEL channels should a VCSEL in one of inner eight channels become non-operational. To enable operation in case of a failure in the communication link to the receiver array ASIC, we have included a power on reset circuit that sets the modulation current in the VCSEL to 9 mA on top of a bias current of 1 mA upon power up with no signal steering.

The 8-bit DAC and LVDS receiver are designed to operate with a 1.5 V supply and the driver stage is designed to operate with a 2.5 V power supply. A higher supply voltage is required by the output stage to allow sufficient headroom to drive VCSELs which normally have threshold voltages of 2 V or higher.

We have characterized several ASICs. Each ASIC is coupled to a VCSEL array fabricated by ULM with a bandwidth of 10 Gb/s [4]. The performance of the ASIC at 5 Gb/s is satisfactory with a bit error rate (BER) of $< 5 \times 10^{-13}$ with all other channels in the ASIC active. We have irradiated two ASICs with 800 MeV protons to a dose of 0.92×10^{15} 1-MeV n_{eq}/cm^2 . Both ASICs were powered during the irradiation. Fig. 1 shows a comparison of the optical eye diagrams obtained before and after the irradiation for one of the ASICs. It is evident that there is more jitter after the irradiation but the ASIC is still operational with a low BER.

III. DESIGN OF A 10 GB/S VCSEL ARRAY DRIVER

We have migrated the design of the 5 Gb/s VCSEL array driver for operation at 10 Gb/s. As a first step, a four-channel

Manuscript received December 4, 2014. This material is based upon work supported by the U.S. Department of Energy Office of Science, Office of Basic Energy Sciences, under Award No. DE-SC0011726 and by the German Federal Minister for Research and Technology (BMBF) under Award No. 056Si74.

K. K. Gan, H. Kagan, R. D. Kass, J. Moore, D. S. Smith are with Department of Physics, The Ohio State University, Columbus, OH 43210, USA (telephone: 614-292-4124, e-mail: gan@mps.ohio-state.edu).

P. Buchholz, S. Heidbrink, M. Vogt, and M. Ziolkowski are with Fachbereich Physik, Universität Siegen, Siegen, Germany (telephone: 271-740-3780, e-mail: Michael.Ziolkowski@uni-siegen.de).

test chip has been designed for fabrication in a 65 nm CMOS process. To achieve the maximum possible radiation-hardness, all transistors used will be core transistors. The core transistors have the thinnest gate oxide available in this process. Given this, the supply voltage of the test chip will be 1.2 V. The block diagram of the VCSEL driver is shown in Fig. 2. The VCSEL modulation and bias currents are controlled via 8-bit DACs. Single event upset (SEU) tolerant registers are used to store the DAC settings (more details below).

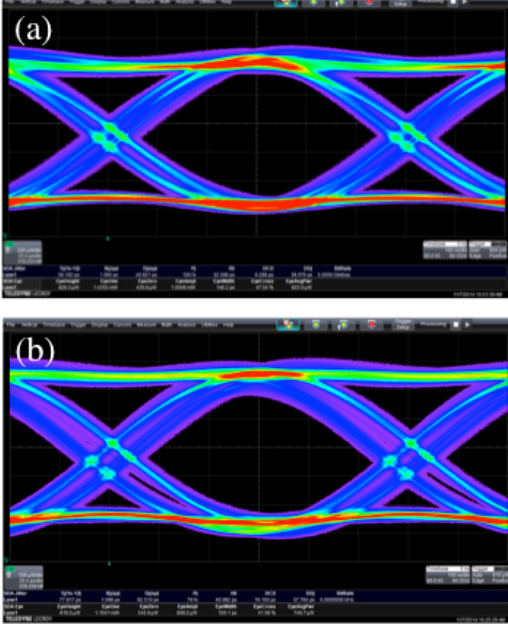


Fig. 1. Comparison of the optical eye diagrams (a) before and (b) after irradiation for a VCSEL channel coupled to a driver ASIC.

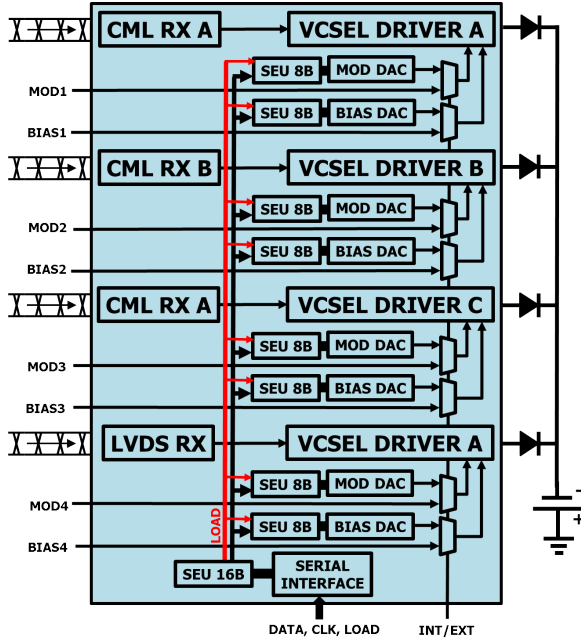


Fig. 2. Block diagram of the 4-channel VCSEL array driver for 10 Gb/s operation.

The ASIC is designed to operate with a supply voltage of 1.2 V. However, commercial VCSEL arrays have a common cathode and require a higher operating voltage. Therefore we

apply a negative bias to the VCSEL cathode in order to provide enough voltage headroom for modulating the VCSEL.

The four channels in the ASIC have different differential receiver and VCSEL driver topologies. These different topologies will be used to qualify the performance and radiation hardness of the different topologies. There are two versions of CML (current mode logic) receivers along with an LVDS like receiver. For the VCSEL driver, there are three different versions with modified driver architectures. The fourth channel, containing the LVDS like receiver, will use a copy of the driver (Driver A) from one of the channels containing a CML receiver. The motivation to include an LVDS like receiver is that, while it has more limited bandwidth, LVDS requires less power to operate than CML. If we can achieve suitable performance at 10 Gb/s with a lower power design this will of course be beneficial.

A. Receiver

The CML receiver is a four-stage limiting amplifier as shown in Fig. 3. Each stage is a common mode feedback amplifier with feed forward capacitors on the input differential pair to enhance the higher frequency signal components. The third channel includes an inductor at the last stage to enhance the bandwidth by inductive peaking. The current consumption of each receiver is 36 mA at 1.2 V, corresponding to a power dissipation of 43 mW. Fig. 4 shows the eye diagram of the extracted layout with and without the inductor. Both eye diagrams are wide open and look similar.

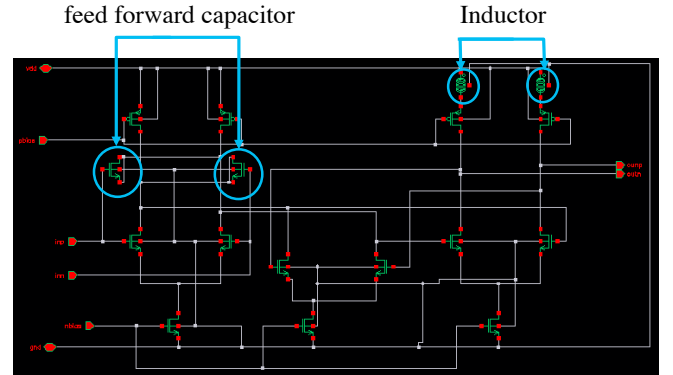


Fig. 3. Schematic diagram of the CML receiver.

As noted above, an LVDS receiver is implemented in channel 4 to reduce the link power consumption. The circuit consumes somewhat lower power, 36 mW, for a current of 30 mA at 1.2 V. The eye diagram as simulated from the extracted layout is slightly worse as shown in Fig. 5, but is still wide open.

B. VCSEL Driver

In the VCSEL driver, the current in the VCSEL is set by two transistors. One transistor has a constant bias current and the other is biased by a capacitive feed forward of the negative half of the differential input signal as shown in Fig. 6. This produces a pre-emphasis and improves the rise and fall times of the VCSEL current. The driver consumes 15 mA of current or 18 mW of power. The eye diagram from a simulation of the

extracted layout including pad, wire-bond, and VCSEL parasitics is shown in Fig. 7. The eye is acceptable.

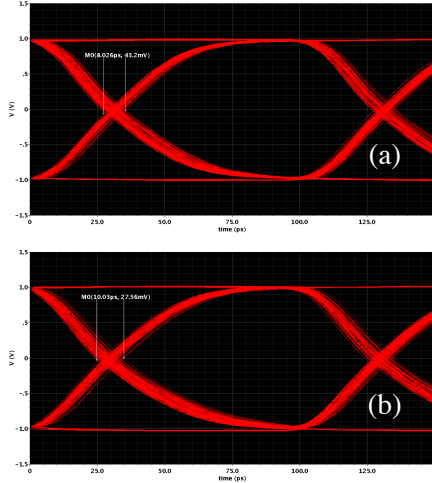


Fig. 4. Eye diagrams of the CML receiver with (a) and without (b) inductive peaking at the last stage.

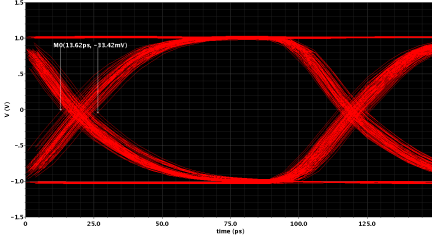


Fig. 5. Eye diagram of the LVDS receiver.

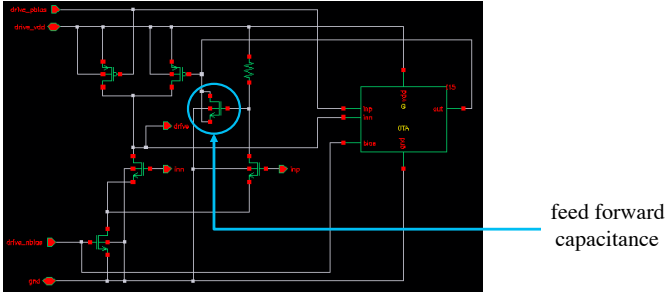


Fig. 6. Circuit of the driver of a VCSEL.

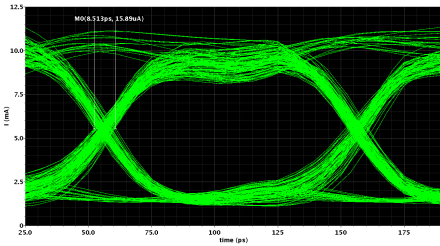


Fig. 7. Eye diagram from a simulation of the extracted layout of the VCSEL driver circuit including parasitic capacitance and inductance.

C. 8-bit DAC and SEU Tolerant Registers

Two 8-bit DACs are used for remotely controlling the VCSEL bias and modulation currents. The DACs are a scaled version of the existing design from the 5 Gb/s VCSEL array driver ASIC fabricated in a 130 nm CMOS process. We plan to use an external reference voltage for this prototype while

waiting for the release of a bandgap reference IP (intellectual property) circuit from CERN. The circuit consumes 270 μ A of current. Fig. 8 shows a sweep of the DAC current vs time (DAC value). The DAC is not quite linear. However, the performance is quite adequate for our application.

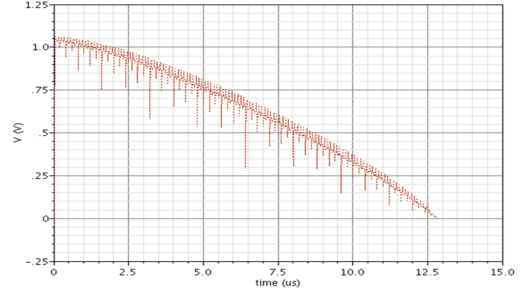


Fig. 8. Output voltage of the 8-bit DAC vs time (DAC value).

The registers for the DACs are based on triply redundant dual interlocked storage cell (DICE) latches [5] to improve their SEU tolerance. The design of an individual DICE latch is shown in Fig. 9. Nodes X1 to X4 store data as complementary values. Consequently, two sensitive nodes storing the same logic state X1/X3 or X2/X4 must change state at the same time to upset the DICE latch. The upset probability is further reduced by separating the drain area corresponding to the sensitive nodes as shown in Fig. 10. The SEU tolerance of the register design will be tested in an irradiation.

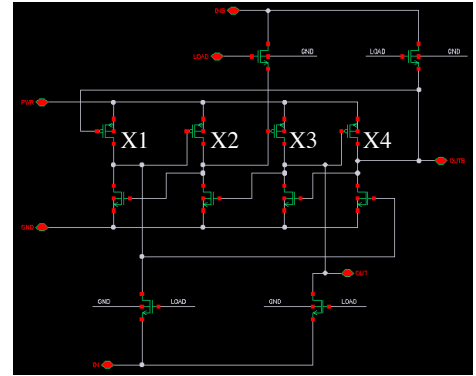


Fig. 9. Circuit of a DICE latch.

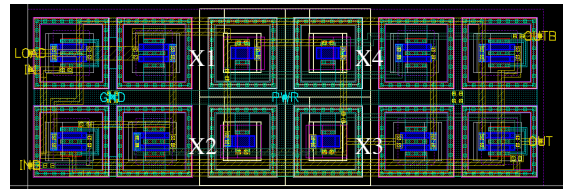


Fig. 10. Layout of a DICE latch.

The 4-channel VCSEL array driver has been submitted for fabrication in early October 2014. The fabricated ASICs will be characterized and then irradiated to verify the radiation hardness. Test results from the four different VCSEL driver channels will guide us in tuning and selecting a preferred topology for the design of a 12-channel ASIC.

IV. CONCLUSIONS

We present an R&D program to develop an ASIC in a 65 nm CMOS process to operate a 12-channel VCSEL array at 10 Gb/s per channel. The design is an upgraded version of a similar ASIC operating at 5 Gb/s, fabricated in a 130 nm CMOS process. We present the result of the 5 Gb/s VCSEL array driver after irradiation. The ASIC is still operational at 5 Gb/s but with more jitter. We present the design of a 10 Gb/s VCSEL array driver together with results from simulations of the extracted layout including parasitics. The ASIC has been submitted for fabrication in October 2014. An evaluation of the performance of the prototype ASIC both before and after irradiation will guide us in the design and fabrication of a 12-channel VCSEL array driver.

REFERENCES

- [1] A. Nagarkar et al., Study of the Radiation-Hardness of VCSEL & PIN Diodes, PoS (RD11) 036 (2012).
- [2] K.K. Gan et al., "Radiation Hard/High-Speed Parallel Optical Links", Nucl. Instrum. Methods. A 765, pp. 64-68 (2014).
- [3] Due to the requirement of another project, the input has only eight receivers even though the output couples to a 12-channel VCSEL array.
- [4] The VCSEL array used is ULM850-10-TN-N0112U, fabricated by ULM Photonics.
- [5] M. Menouni et al., "Design and Measurements of SEU Tolerant Latches", in Proceedings of Topical Workshop on Electronics for Particle Physics (TWEPP08), Naxos, Greece (2008), pp. 402-405.