ELSEVIER SCIENCE

Radiation-Hard/High-Speed Parallel Optical Links

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Elsevier use only: Received date here; revised date here; accepted date here

Abstract

We have designed an ASIC for use in a parallel optical engine for a new layer of the ATLAS pixel detector in the initial phase of the LHC luminosity upgrade. The ASIC is a 12-channel VCSEL (Vertical Cavity Surface Emitting Laser) array driver capable of operating up to 5 Gb/s per channel. The ASIC is designed using a 130 nm CMOS process to enhance the radiation-hardness. A scheme for redundancy has also been implemented to allow bypassing of a broken VCSEL. The ASIC also contains a power-on reset circuit that sets the ASIC to a default configuration with no signal steering. In addition, the bias and modulation currents of the individual channels are programmable. We have tested the ASIC and the performance up to 5 Gb/s is satisfactory. Furthermore, we are able to program the bias and modulation currents and to bypass a broken VCSEL channel. We are currently upgrading our design to allow operation at 10 Gb/s per channel yielding an aggregated bandwidth of 120 Gb/s. Preliminary results of the design will be presented.

Keywords: HL-LHC; optical-link; VCSEL array driver; radiation-hard;

1. Introduction

A parallel optical engine allows a compact design for high-speed data transmission. The design is enabled by readily available high-speed VCSEL arrays. With the use of a 12-channel array operating at 10 Gb/s per channel, a parallel optical engine can deliver an aggregate bandwidth of 120 Gb/s. With a standard spacing of 250 μm between VCSELs, the width of a 12-channel array is only slightly over 3 mm. This allows the fabrication of a rather compact parallel optical engine for installation in locations where space is at a premium. Besides the reduced physical size, there are other advantages in using an array solution. For example, one can reserve 1 in 12 channels for redundancy instead of doubling the number of channels if using a single-channel VCSEL. This is therefore a much more efficient scheme to implement redundancy for bypassing a dead channel. The array scheme also reduces the service

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requirements by using one power supply to bias each array instead of a single power supply for each VCSEL channel. Additionally, the use of a fiber ribbon reduces the number of fibers to handle and moreover a fiber ribbon is less fragile than a single-channel fiber. These multiple advantages greatly simplify the production, testing, and installation of optical links.

VCSEL arrays are widely used in off-detector data transmission. The first implementation of VCSEL arrays for on-detector application is in the optical links of the ATLAS pixel detector. The experience from the operation has been quite positive despite failures in the optical readout system [1]. Modern VCSELs are humidity tolerant and hence no special precautions are needed. The ATLAS experiment plans to continue the use of VCSEL arrays in a new layer of the pixel detector, the insertable barrel layer (IBL), to be installed in the initial phase of the LHC luminosity upgrade.

In response, we have designed an ASIC for possible use in the IBL project. The ASIC is a 12-channel VCSEL array driver capable of operating up to 5 Gb/s per channel. We will present some measurements of the characteristics of the ASIC below. We have also modified the design for operation at 10 Gb/s per channel and the preliminary design will be presented.

2. Results from a 5 Gb/s VCSEL Array Driver

The VCSEL array driver ASIC is designed to operate at speed up to 5 Gb/s. The planned operating speed for the IBL optical link is 160 Mb/s but we designed the ASIC to operate at much higher speed to gain experience in the design of a high-speed array driver. The ASIC was fabricated in a commercial 130 nm CMOS process to enhance the radiation-hardness. All circuitry was designed following test results and guidelines from CERN on radiation tolerant design in the 130 nm process used [2]. The ASIC is an improved version of the driver designed with a 250 nm CMOS process for use in the optical links [3] of the installed pixel detector of the ATLAS experiment. Several improvements were incorporated into the new ASIC taking advantage of experience gained from building and operating the first array-based optical links and will be detailed below.

Each ASIC contains eight low voltage differential signal (LVDS) receivers to receive the data from the front-end electronics. A block diagram of the ASIC is shown in Figure 1. The received LVDS signal is converted in the driver stage into a current sufficient to drive a VCSEL. The amplitude of the modulation current in each driver is controlled via an 8-bit DAC. There is also a single 8-bit DAC to set the bias currents of all of the channels simultaneously. When connected to a commercial VCSEL array fabricated by ULM Photonics [4], the ASIC delivers up to 13.5 mA of modulation current and up to 4 mA of bias current. We have included four spare drivers with associated 8-bit DACs that can receive the LVDS signal from any of the eight LVDS receivers via a switching network. This allows the received LVDS signal to be transmitted via one of the four spare VCSEL channels should a VCSEL in one of eight inner channels become non-operational. To enable operation in case of a failure in the communication link to the receiver array ASIC, we have included a power on reset circuit that will set the modulation current in the VCSEL to 9 mA on top of a bias current of 1 mA upon power up with no signal steering.

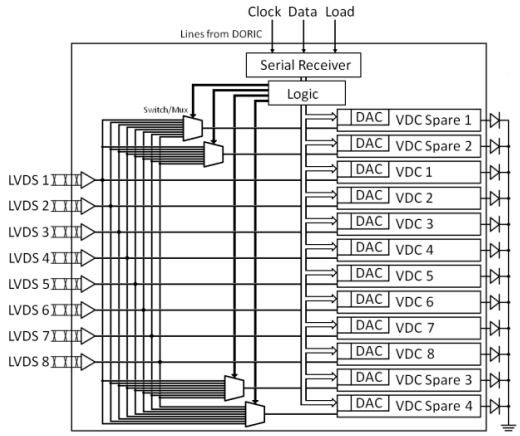

Figure 1: A 12-channel VCSEL array driver ASIC.

The 8-bit DAC and LVDS receiver are designed to operate with a 1.5 V supply and the driver stage is designed to operate with a 2.5 V power supply. The higher supply voltage is used by the output stage to allow enough headroom to drive VCSELs which normally have threshold voltages of ~2 V.

We have characterized several ASICs. Each ASIC is coupled to a VCSEL array with a bandwidth of 10 Gb/s [4]. The current consumption for the 2.5 V supply is measured to be 250 mA with all channels active at 5 Gb/s and with 12 mA of modulation and 4 mA of bias current in each VCSEL. Under this condition, the VCSEL produces an optical power in excess of 1 mW. The power consumption for the 1.5 V supply under these conditions is 30 mA. A reduced power consumption on the 2.5 V supply is possible by lowering the VCSEL bias and modulation currents however this introduces a penalty on the output optical power.

The optical eye diagram of a channel in the driver ASIC with the bias settings described above is shown in Figure 2. All other channels in the ASIC were active with the same pseudo-random input signal but delays introduced by cabling and buffer chips distributing the signals effectively desynchronize the signals into each VCSEL driver channel. It is evident that the eye is open.

Due to the limited availability of a high-speed optical probe in our test, we also evaluate the performance of the

driver ASIC using a Finisar Small Form Factor (SFP+) transceiver. This SFP+ transceiver is specified to operate at 10 Gb/s and thus we can use it to probe of the quality of the received the optical signal from the VCSEL. This is accomplished by feeding the SFP+ electrical output to a 13 GHz oscilloscope. It should be noted that the use of the SFP+ transceiver improves the vertical eye opening. The transceiver discriminates the optical signal and thus removes amplitude noise by re-shaping the wave fronts. Figure 3 shows the eye diagram obtained with the SFP+ transceiver. It is evident that the received electrical signals are well separated from the reference mask [5]. We used simulations on the extracted layout to find the cause of the bi-modal jitter in the optical and received electrical eye diagrams. The simulations indicate that the bi-modal jitter originated in the LVDS receiver which then propagated through the rest of the circuit. In simulation we found 19 ps of peak to peak bi-modal jitter in the VCSEL current. For comparison, we measured 20 ps jitter in the observed eye diagrams. Thus, our simulations agree well with our measurements and we will focus further efforts on improving the design of the LVDS receiver.

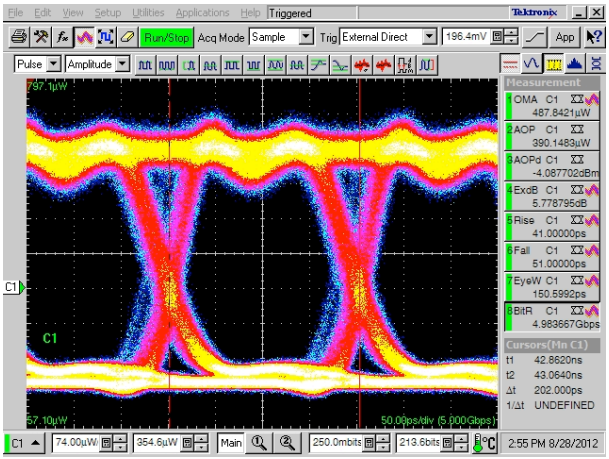

Figure 2: Optical eye diagram of a VCSEL channel coupled to a driver ASIC.

The eye diagram in Fig. 3 is for the case in which only one VCSEL driver channel is active. Figure 4 shows the eye diagram with all channels active, a more realistic operating condition. It is evident that the jitter is somewhat larger, 53 ps peak to peak, but that the signal is well separated from the reference mask. The bit error rate is less than $5x10^{-13}$ with all channels active at 5 Gb/s.

As noted above, the ASIC also contains several functionalities to make the optical links more reliable and easier to operate, motivated by the experience in operating the first on-detector optical links based on VCSEL arrays. This includes a power-on reset circuit that sets the ASIC to a default configuration with no signal steering in case of a failure in the communication link to the ASIC. This feature has been successfully implemented. We also verified that the bias and modulation currents of the individual channels are programmable. The power-on reset circuit sets the ASIC to produce 9 mA of modulation current and 1 mA of bias current. This has also been verified.

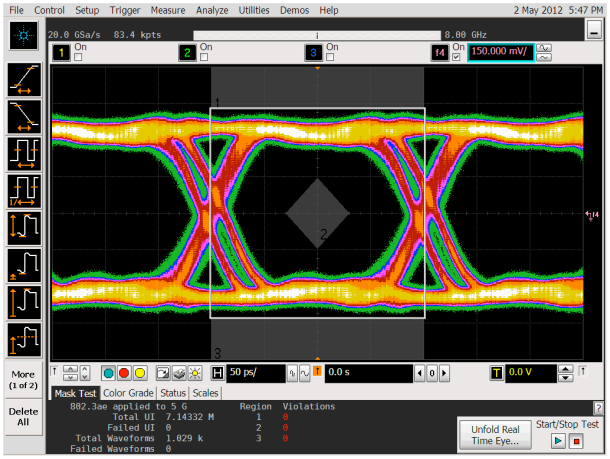

Figure 3: Eye diagram of a VCSEL channel coupled to a driver ASIC as viewed with a SFP+ transceiver. Only one driver channel is active.

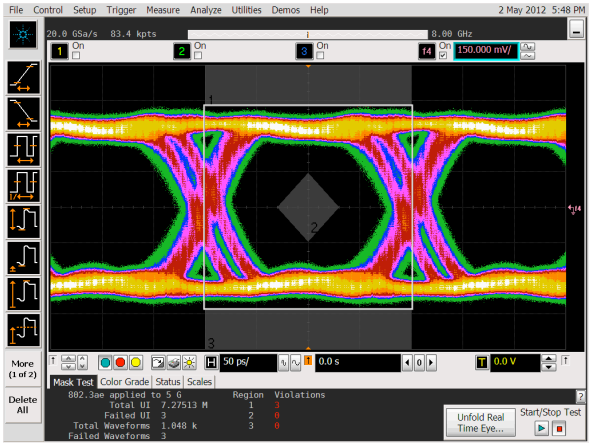

Figure 4: Eye diagram of a VCSEL channel coupled to a driver ASIC as viewed via a SFP+ transceiver. All driver channels are active.

The redundancy circuit is an important feature implemented for the bypassing of a broken VCSEL. The integrity of the steered signal in the spare channel has been tested by steering the signal through the maximum distance from a channel on one side of the ASIC to the spare channel on the other side. Figure 5 shows the eye diagram of this signal. The steered signal has more jitter as expected but is well separated from the reference mask.

3. Preliminary Design of a 10 Gb/s VCSEL Array Driver

We are currently designing a 10 Gb/s VCSEL driver to yield an aggregated bandwidth of 120 Gb/s when coupled

to a 12-channel VCSEL array. A central question of the design is which semiconductor process to use. We expect both 130 nm SiGe BiCMOS and 65 nm CMOS to have the sufficient bandwidth. However, due to cost consideration, we will first attempt to design the driver using the 130 nm CMOS process to see if this is practical.

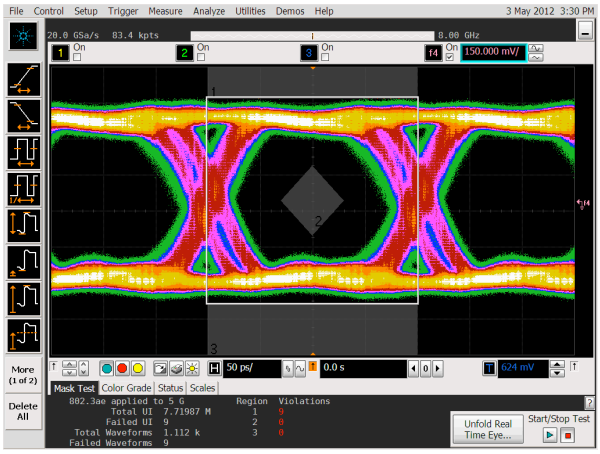

Figure 5: Eye diagram of the steered signal in a spare channel as viewed via a SFP+ transceiver. All driver channels are active.

The 130 nm process provides three FET types with different oxide thicknesses to be compatible with various power and signal schemes. The 5 Gb/s VCSEL driver uses transistors with the medium oxide thickness in order to drive the VCSEL with a supply voltage of 2.5 V. This is not practical for the high speed operation due to the increased parasitic capacitance / inductance. We therefore modify the architecture to use thin oxide transistors and add a negative VCSEL bias voltage.

We have a preliminary design for the driver stage of the ASIC. The design has been laid out. We have simulated the extracted layout with parasitic capacitance, inductance, and resistance from the VCSEL itself and the wire bonds and pads used for connecting the VCSEL to the ASIC. The parasitics used for the ASIC and bond pads are provided by our ASIC design extraction software. For the bonds themselves we use a lumped model provided in [6]. The custom VCSEL model used includes a diode with parameters adjusted to match the IV characteristics of the VCSEL under test and a capacitance provided by the vendor. The simulated eye diagram of the driver stage is shown in Figure 6. It is evident that the eye diagram is open but obviously much work remains.

4. Conclusions

We present the result of a 5 Gb/s VCSEL array driver ASIC for use in a parallel optical engine. The ASIC is designed using a 130 nm CMOS process to enhance the radiation-hardness. The eye diagram is open and the added functionalities to make the optical engine more reliable and easier to operate are also successful. This includes the ability to set modulation current for each VCSEL individually and the bias current for the whole array. Also included is a redundancy circuit to bypass a broken channel and a power-on reset circuit to set the ASIC to a default configuration with no signal steering and a default bias and modulation currents in a VCSEL. In addition, we present a preliminary design for a 10 Gb/s VCSEL array driver for use in a parallel optical engine to produce an aggregated bandwidth of 120 Gb/s.

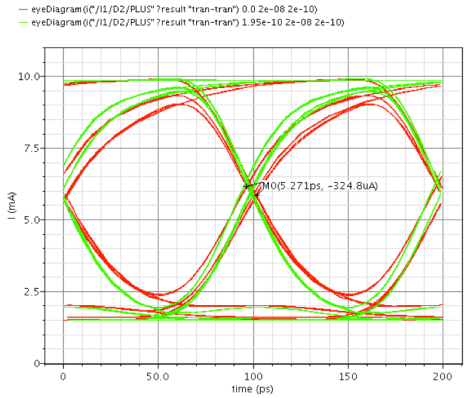

Figure 6: Simulated eye diagram for the VCSEL driver stage operating at 10 Gb/s.

Acknowledgement

This work was supported in part by the U.S. Department of Energy under contract No. DE-FG-02-91ER-40690 and by the German Federal Minister for Research and Technology (BMBF) under contract No. 056Si74.

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