Radiation-hard/high-speed data transmission using optical links

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The silicon trackers of the ATLAS experiment at the Large Hadron Collider (LHC) at CERN (Geneva) use optical links for data transmission. An upgrade of the trackers is planned for the Super LHC (SLHC), an upgraded LHC with ten times higher luminosity. We investigate the radiation-hardness of various components for possible application in the data transmission upgrade. We study the radiation-hardness of VCSELs (Vertical-Cavity Surface-Emitting Laser) and GaAs and silicon PINs from various sources using 24 GeV/c protons at CERN. The optical power of VCSEL arrays decreases significantly after the irradiation but can be partially annealed with high drive currents. The responsivities of the PIN diodes also decrease significantly after irradiation, especially for the GaAs devices. We have designed the ASICs for the opto-link applications and find that the degradation with radiation is acceptable.

1. INTRODUCTION

The SLHC is designed to increase the luminosity of the LHC by a factor of ten to 10^{35} $cm^{-2}s^{-1}$. Accordingly, the radiation level at the detector is expected to increase by a similar factor. The increased data rate and radiation level will pose new challenges for a tracker situated close to the interaction region. The silicon trackers of the ATLAS experiment at the LHC use VCSELs to generate the optical signals at 850 nm and PIN diodes to convert the signals back into electrical signals for further processing. The devices have been proven to be radiation-hard for operation at the LHC.

In this paper, we present a study of the radiation hardness of PINs and VCSELs. In addition, we present the results on three ASICs, a high-speed driver for a VCSEL, a receiver/decoder to decode the signal received at a PIN diode to extract the data and clock, and a clock multiplier to produce a higher frequency clock needed to serialize the data for transmission.

2. RADIATION HARDNESS OF PINS AND VCSELS

The main radiation effect in a VCSEL is expected to be bulk damage and in a PIN diode the displacement of atoms. We use the Non Ionizing Energy Loss (NIEL) scaling hypothesis to estimate the SLHC fluences [1-3] at the present pixel optical link location (PP0). After five years of operation at the SLHC, we expect the silicon component (PIN) to be exposed to a maximum total fluence of 2.5 x 10^{15} 1-MeV n_{eq}/cm^2 [4]. The corresponding fluence for a GaAs component (VCSEL or PIN) is 1.4 x 10^{16} 1-MeV n_{eq}/cm^2. We study the response of the optical link to a high dose of 24 GeV/c protons. The expected equivalent fluences at LHC are 4.3 and 2.7 x 10^{15} p/cm^2, respectively.

We packaged the PINs and VCSELs at OSU for the irradiation. For the PIN diodes, we irradiated two GaAs arrays from Advanced Optical Components (AOC), Optowell, ULM Photonics, and Hamamatsu. In addition, we also irradiated silicon PINs, two Taiwan arrays and eleven single-channel silicon diodes from Hamamatsu (five S5973 and six S9055). The VCSEL arrays irradiated include two from Optowell and one 5 and one 10 Gb/s array from AOC.

We monitored the PIN responsivities during the irradiation by illuminating the devices with light from VCSELs and measuring the PIN currents.

Figures 1 and 2 show the PIN currents for the GaAs and silicon devices as a function of time. The responsivities decreased during the irradiation as expected. Table 1 summarizes the responsivities before and after irradiation. Due to a technical problem, the devices received about half the dosage expected at SLHC and the responsivities after the SLHC dose are estimated by extrapolation. For the GaAs arrays, Optowell and Hamamatsu have the highest responsivities after the irradiation. As expected, the silicon devices are more radiation hard, with Hamamatsu S5973 having the highest responsivities. However, it should be noted that the bandwidth of the silicon PIN diodes is somewhat smaller. We await the return of the devices to OSU for further characterization.

Table 1: Responsivities (R) of PIN diodes from various sources before and after irradiation. The bandwidth (BW) of each device is also indicated.

	BW (Gb/s)	R (A/W)	
GaAs		Pre	Post
ULM	4.25	0.50	0.03
AOC	2.5	0.60	0.04
Optowell	3.125	0.60	0.10
Hamamatsu G8921	2.5	0.50	0.20
Si			
Taiwan	1.0	0.55	0.19
Hamamatsu S5973	1.0	0.47	0.29
Hamamatsu S9055	1.5	0.25	0.18

The VCSEL arrays were mounted on a shuttle to allow the arrays to be moved out of the beam for periodic annealing. The optical power vs. dosage is shown in Fig. 3. The optical power decreased during the irradiation as expected. We annealed the arrays by moving the arrays out of the beam and passing the maximum allowable current (~10 mA per channel) through the arrays for ~12-16 hours each day. The optical power increased during the annealing. Unfortunately, there was insufficient time for a complete annealing but the AOC arrays still have good optical power at the SLHC dosage. However, the situation is less clear with the Optowell device because of an intermittent connectivity problem. We believe the Optowell arrays will have good optical power when we characterize them in the lab after the radiation cool down.

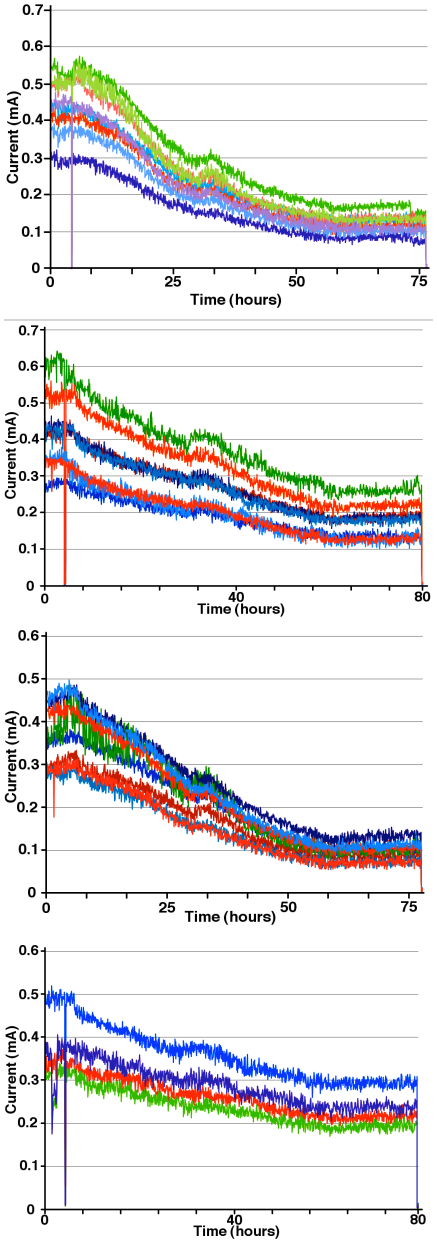

Figure 1: PIN current as a function of time (dosage) for the GaAs PIN arrays from four vendors, AOC, Optowell, ULM, and Hamamatsu. The irradiation occurred between ~5 and 50 hours.

3. RESULTS ON ASICS

We have designed a prototype chip containing building blocks for future SLHC optical link applications using a 130 nm CMOS 8RF process.

The chip contains four main blocks; a VCSEL driver optimized for operation at 640 Mb/s, a VCSEL driver optimized for operation at 3.2 Gb/s, a PIN receiver with a clock and data recovery circuit capable of operation at 40, 160, or 320 Mb/s, and two clock multipliers designed to operate at 640 Mb/s. The clock multiplier is needed to produce a higher frequency clock needed to serialize the data for transmission. All circuitry within the test chip was designed following test results and guidelines from CERN on radiation tolerant design in the 130 nm process used.

We have received the prototype chips and the chips has been characterized in the lab followed by an irradiation with 24 GeV/c protons at CERN. The results are summarized below. All chips tested were packaged for the irradiation, resulting in some speed degradation due to the added stray capacitance of the packaging.

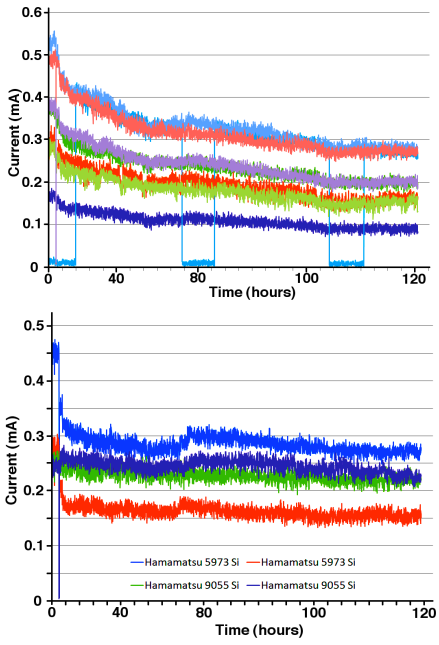

Figure 2: PIN current as a function of time (dosage) for the silicon PIN diodes from two sources, Taiwan (top) and Hamamatsu (bottom). The irradiation occurred between ~5 and 110 hours. The three sudden drops in the PIN current of a channel in the Taiwan array were due to an instrumental problem.

The two VCSEL driver circuits in the test chip have similar architecture, one optimized for 640 Mb/s with higher drive current and the other for 3.2 Gb/s with lower current. Each consists of a 1.5 V LVDS receiver circuit, a 1.5 to 2.5 V logic converter circuit, and a 2.5 V VCSEL driver circuit. Both VCSEL drivers allow for adjustable bias and modulation currents and contain circuitry to reduce switching noise on the power supply lines. We used a 2.5 V supply for the driver circuitry because most commercially available VCSELs require bias voltages greater than 2 V to produce suitable output optical power. To allow for 2.5 V operation, the driver portion of the chips were designed using the thick oxide transistors available in the 130 nm process. We chose to design the LVDS receiver using the standard thin oxide transistors that operate with a 1.5 V supply. The use of the thin oxide transistors allowed us to not only achieve higher bandwidth over the thick oxide transistors but also produce a circuit that could be used by other members of our community developing chips which operate with a single 1.5 V supply. Previous results from CERN have shown that thin oxide transistors designed using conventional layout techniques exhibit radiation tolerance suitable for SLHC applications. However, conventionally designed thick oxide transistors are not suitably radiation tolerant. Because of this, all of the thick oxide transistors were designed using an enclosed structure. Four prototype chips were packaged and the performance was satisfactory up to 1 Gb/s. The performance at higher speeds could not be sufficiently evaluated due to the packaging parasitics. These tests also verified the operation of the LVDS receiver up to 1 Gb/s. During the irradiation, each VDC was connected to a 25 Ω resistor instead of a VCSEL to allow testing of the degradation of the chip alone. The duty cycle of the output signal remained constant during the irradiation. The current consumption of the LVDS receiver also remained constant. However, we observed significant decreases in the VCSEL driver circuit current consumption and the output drive current. This indicates that the think oxide layout used in the VCSEL driver portion of the chip might not be as radiation-hard. However, it should be noted that the decrease in the drive currents could be compensated by adjusting the control current but this option was not used during the irradiation in order to study the degradation under the same condition.

The prototype PIN receiver circuit contains a trans-impedance amplifier, limiting amplifier, bi-phase mark (BPM) decoder with clock recovery, and

LVDS drivers to send the decoded data and recovered clock off chip. All transistors are of the thin oxide variety and thus the chip is designed to run with a single 1.5 V power supply. The clock and data recovery is accomplished using a delay locked loop that contains networks of switchable capacitors in the delay stages allow for the three operating frequencies, 40, 160, and 320 Mb/s. However, the eight chips packaged for the irradiation could only operate at 40, 80, and 160 Mb/s. This problem is not yet fully understood. Other than this mystery, the performance of the chips is satisfactory except for higher threshold currents required to have a low bit error rate (BER). The performance parameters measured include clock jitter, duty cycle, rise/fall time, and high/low levels of the LVDS drivers. The thresholds for no bit errors at 80 and 160 Mb/s are somewhat high and we plan to improve the noise immunity in the next submission using an improved layout topology. For the irradiation, the chips were tested in two different setups of four chips each. The first setup was purely electrical while the second setup involved a PIN diode so that we could decouple the electrical and optical degradations. In both setups, the decoded data were transmitted to the control room using 20 m of coax. In the first setup, 40 Mb/s BPM signals were transmitted over 20 m of coax to the chips. The long cable precluded testing at higher speed. In the second setup, we sent 40 Mb/s BPM signal via a fiber to a PIN diode coupled to a chip. For both setups, we observed single event setup during the spill and decided to monitor the threshold for ~1 error/s as a function of dosage and observed no degradation. The current consumption was constant during the irradiation. We also monitored the BER vs. PIN current during the irradiation. As expected, the BER decreased with larger PIN current and was higher for a chip coupled to a PIN diode.

The clock multiplier circuits on the test chip consist of charge pump/ring oscillator phase locked loops (PLL) with dividers in the feedback loop. One circuit performs a frequency multiplication of 16 and the other a multiplication by 4, both yielding a 640 MHz clock. The multipliers are designed using thin oxide transistors and are powered by a single 1.5 V supply. The multiplier circuits share a common 50 Ω driver and LVDS receiver enabling testing of only one multiplier at a time. An additional switching network allows the recovered clock from the PIN receiver prototype to be routed to either multiplier to allow for testing of how the received signal jitter is coupled to the multiplied clock. Four multipliers were packaged for the irradiation. All chips functioned well with clock jitter of < 8 ps or 0.5%. During the irradiation, we observed that the clocks of two chips lost lock and power cycling was needed to resume operation at 640 MHz. This problem needs to be investigated.

We are still characterizing the chip and awaiting the return of the irradiated chips to the lab for a post-irradiation comparison. An improved version of the chip will be submitted in March 2009 implementing what we learned from the study.

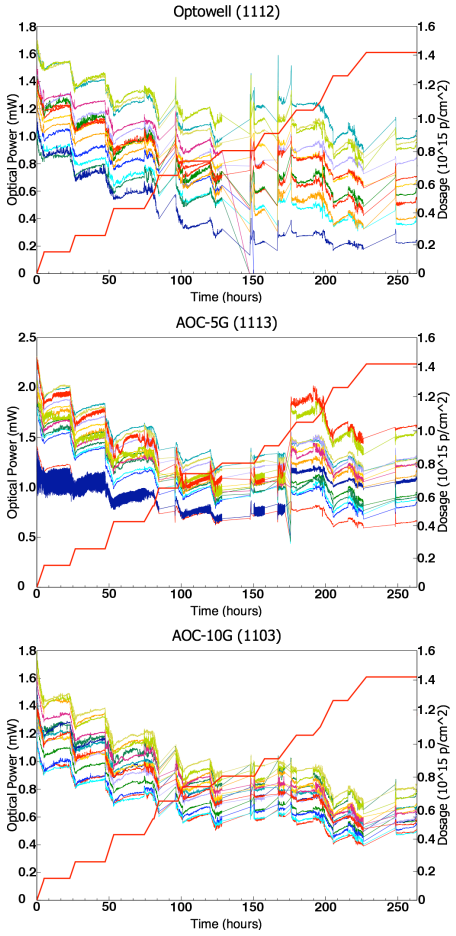

Figure 3: Optical power as a function of time (dosage) of three VCSEL arrays. The power decreased during the irradiation but increased during the annealing as expected. The sudden drop in power at ~150 hours for the Optowell array was due to a technical problem.

4. SUMMARY

We have studied the radiation hardness of PINs and VCSELs. The VCSEL arrays by AOC produce good optical power after the irradiation. Both GaAs and silicon PIN diodes by Hamamatsu have good responsivities after irradiation. We have designed the ASICs for the opto-link applications and find that the degradation with radiation is acceptable.

ACKNOWLEDGEMENTS

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REFERENCES

1. I. Gregor, "Optical Links for the ATLAS Pixel Detector," Ph.D. Thesis, University of Wuppertal (2001).
2. A. Van Ginneken, "Nonionzing Energy Deposition in Silicon for Radiation Damage Studies," FERMILAB-FN-0522, Oct. 1989.
3. A. Chilingarov, J.S. Meyer, T. Sloan, "Radiation Damage due to NIEL in GaAs Particle Detectors," Nucl. Instrum. Meth. A 395, 35 (1997).
4. The fluences include a 50% safety margin.