WBS 6.1.3
Pixel Communication & Services

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Level-3 Manager & CAM
The Ohio State University

U.S. ATLAS HL-LHC Upgrade Project DOE CD-1 Review
Brookhaven National Laboratory
Upton, NY
July 10-12, 2018

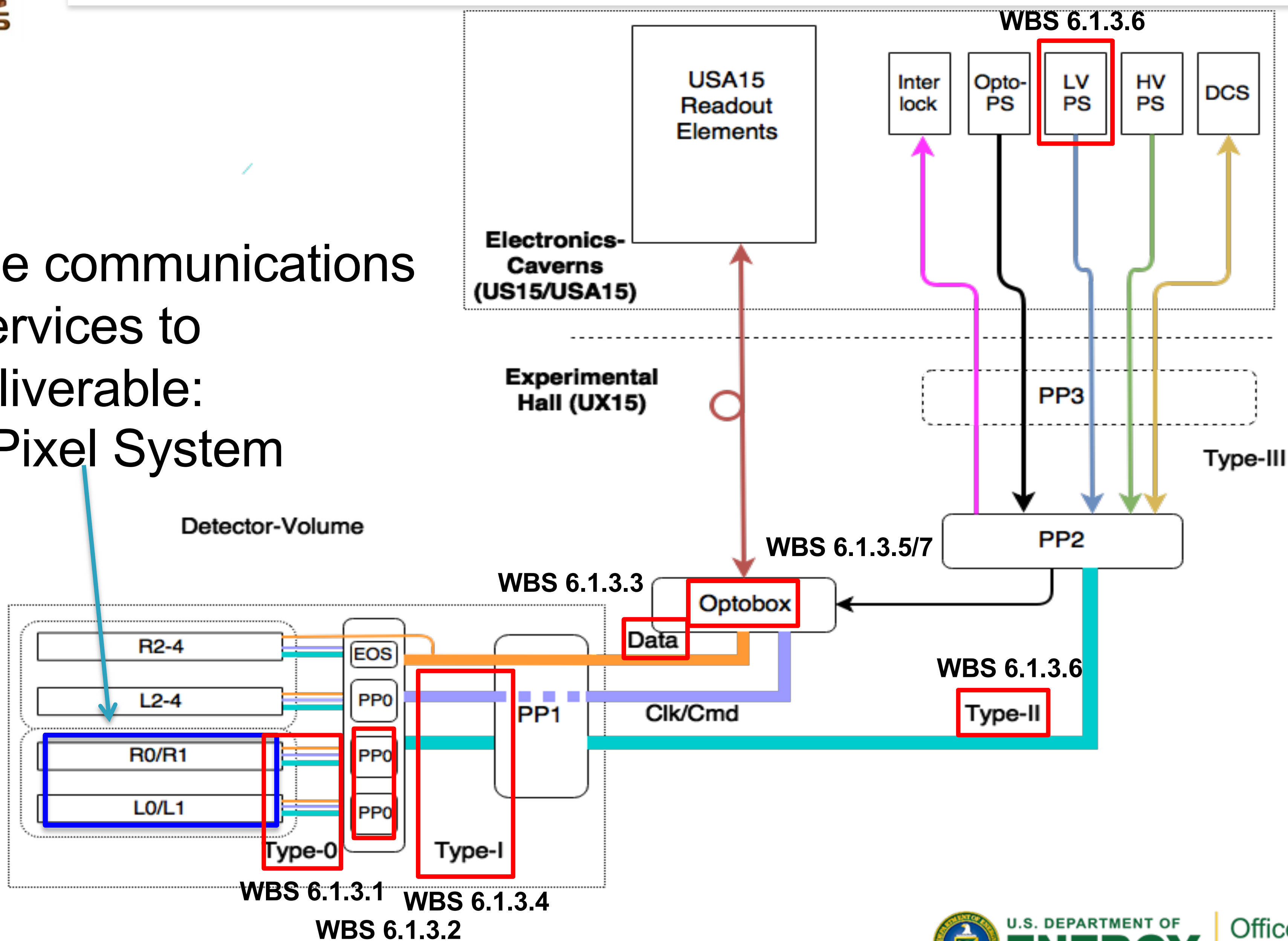
Outline

- Technical Details
  - Deliverable Overview
  - R&D Status and Plans
- Project Management
  - Management Structure: CAM and ICs
  - Cost and Schedule Estimating Methodology
  - ES&H
- Cost and Schedule
  - Budget and Schedule estimates
  - Risk and Uncertainty
- Closing Remarks

Technical Details

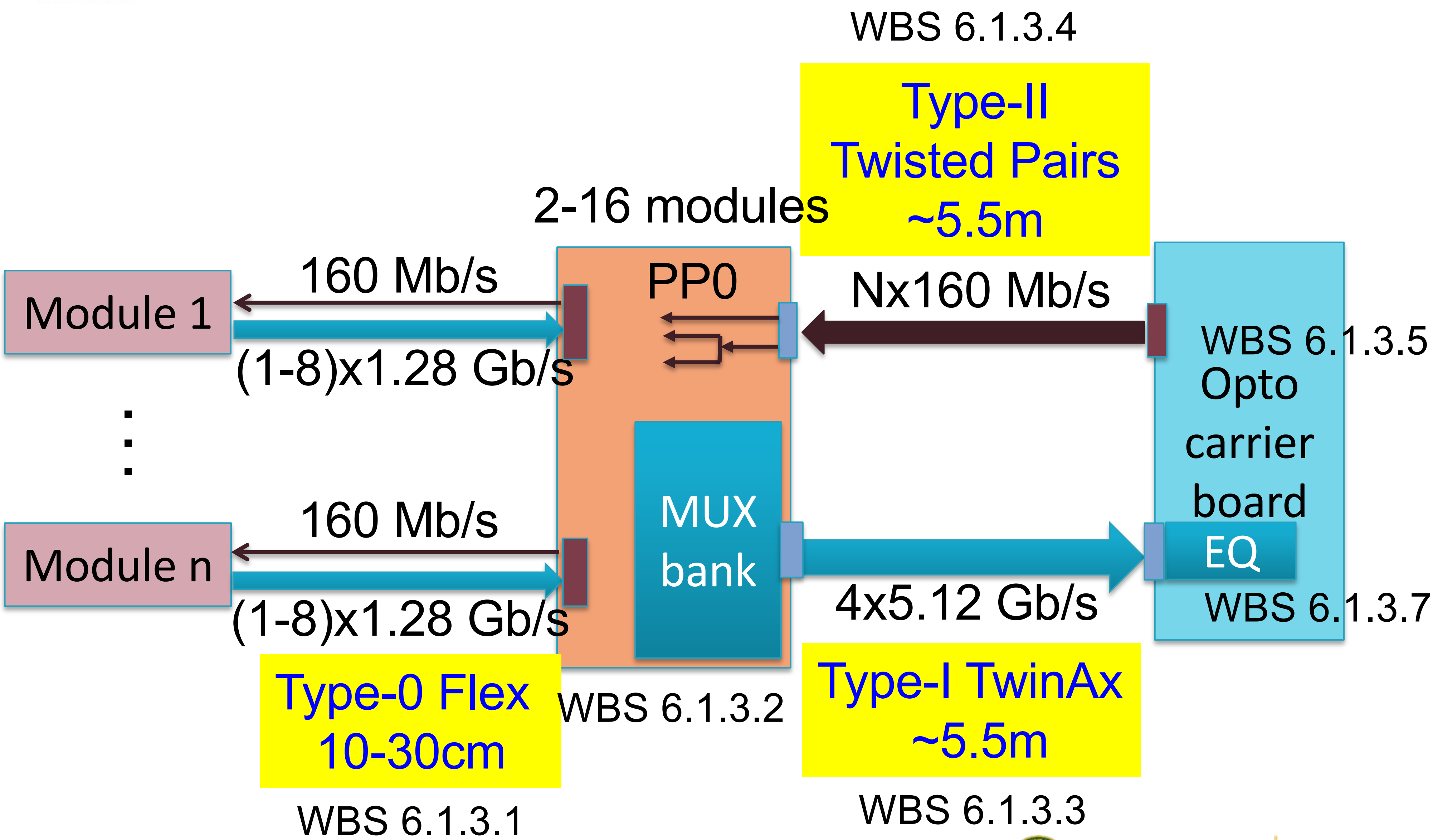
Deliverable Overview

Provide communications and services to US deliverable: Inner Pixel System



U.S. DEPARTMENT OF ENERGY Office of Science

Deliverable Overview



WBS 6.1.3.1

CQ.2

- Institution: Oklahoma State
- 6.1.3.1: Flex Circuit
  - design/prototype/production of radiation-hard flex circuits for transmission of command/clock, LV, HV, Detector Control System (DCS)
  - Challenge: high-speed transmission (1.28 Gb/s)/low signal loss or voltage drop with minimum material

	Quantity
Flexes needed for inner system	300
Yield	72%
Flexes to be produced	420

WBS 6.1.3.2

CQ.2

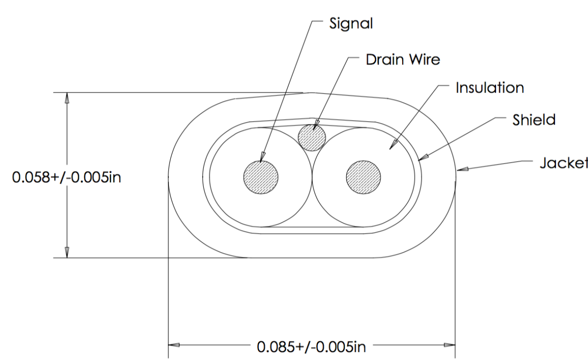
- Institution: SLAC
- 6.1.3.2: Patch Panel 0 (PP0)
  - Design/prototype/production of radiation-hard PP0 with connectors for data, command/ clock, LV, HV, Detector Control System (DCS)
  - challenge: minimum material and insertion loss in bandwidth/signal strength

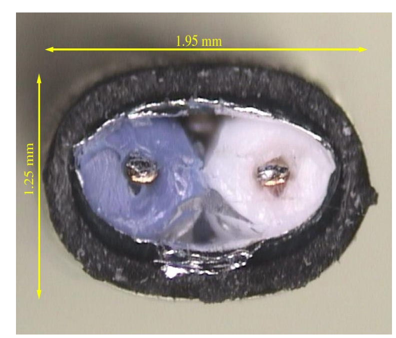
PP0 type	Quantity
Data Barrel L0	96
Data Barrel L1	120
Data Endcap	648
SP chains	264
Yield	85%

WBS 6.1.3.3

CQ.2

- Institution: SLAC
- 6.1.3.3: TwinAx
  - Radiation-hard co-axial cables for data transmission at 5.12 Gb/s from PP0 to opto carrier boards
  - Need 864 bundles of four TwinAx cables
    - Opto-box : soldering to mini-PCB with connector
    - PP0: soldering to PP0 for inner detector and to mini-PCB at outer detector
  - Challenge: high-speed data transmission up to 5.5 m of skinny cables with minimum attenuation and material





WBS 6.1.3.4

CQ.2

- Institution: UC Santa Cruz
- 6.1.3.4: Type-I bundle
  - design/prototype/production of radiation-hard cable bundles for command/clock, LV, HV, Detector Control System (DCS) from PP1 to PP0
  - Challenge:
    - compact bundles with minimum material and connectorization loss
    - complicated procedure to attach fine conductors to high-pin-count LEMO connectors

WBS 6.1.3.5

CQ.2

- Institution: Ohio State
- 6.1.3.5: Optical Carrier Board
  - QA of optical carry boards designed by Bern
  - Production of 280 boards, including 80% yield

WBS 6.1.3.6

CQ.2

- Institution: Oklahoma State
- 6.1.3.6: Serial Power Supply
  - design/prototype/production of power supplies, backplane, control system, chassis, Type-II cables
  - Challenge: supply constant current up to 16 FE ASICs in series
  - Technical Specs: supply constant current of 8 A per channel at 36 V to the front-end chips with a voltage range of 1.2-1.5 V per chip

Description	Quantity
Power supplies to be installed	307
Production yield	90%
Power supplies to be produced	341

Description	Quantity
Type-II cables needed in the pixel inner system	142
Production yield	90%
Type-II cables to be produced	158

WBS 6.1.3.7

CQ.2

- Institution: Southern Methodist U.
- 6.1.3.7: Equalizer ASIC
  - design/prototype/production of equalizer ASIC
  - Challenge:
    - correct for degradation of high frequency component of the data signal after propagation through TwinAx
    - need signal equalization circuit and clock data recovery (CDR) to retime the signal

Technical Specs

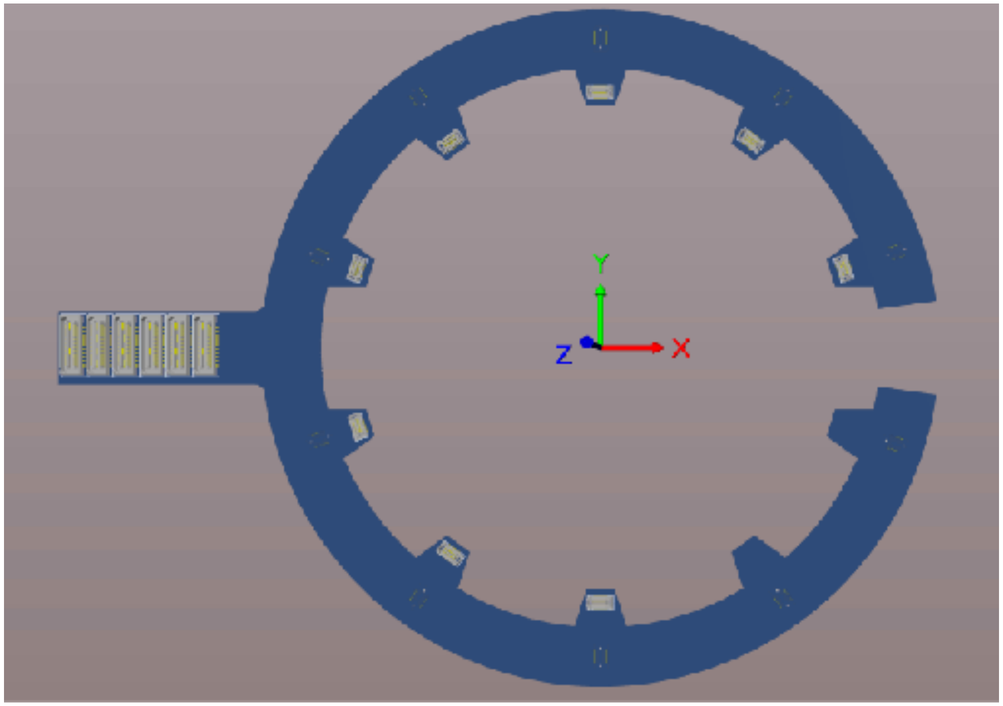
CQ.2

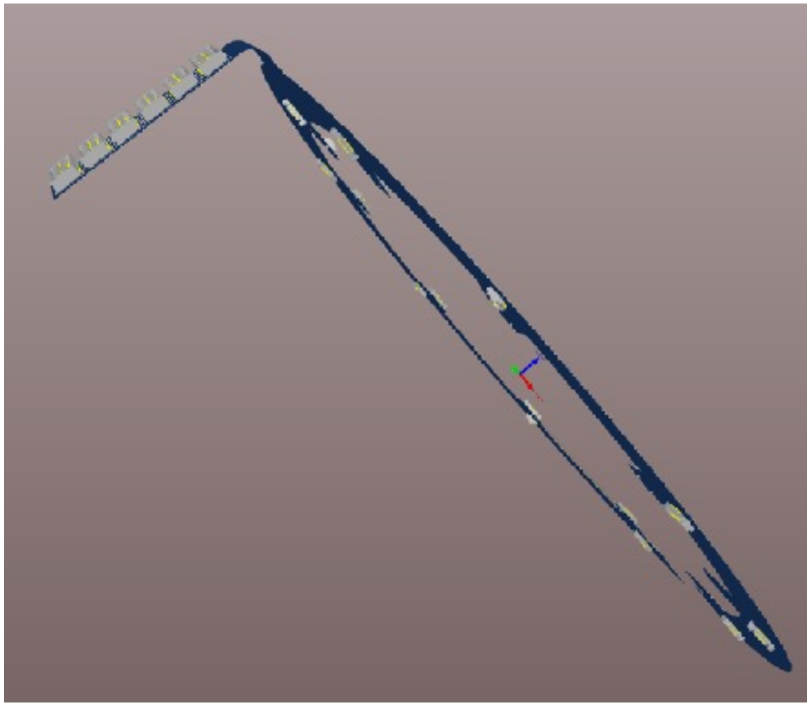
- 6.1.3.1 (Type-0 Flexes), 6.1.3.2 (Patch Panel 0), 6.1.3.3 (Twinax Cables), 6.1.3.4 (Type-I Cables) and 6.1.3.7 (Equalizer): radiation-hard data transmission from the modules to the optical converters at 5.12 Gb/s up to 5.5 meters with maximum attenuation of 20 dB.
- 6.1.3.5 (Opto-Links): optical converters for converting electrical data signals to optical signals for transmission to the DAQ system at 5.12 Gb/s per channel and vice verse for the clock/command signal at 160 Mb/s from the DAQ system.
- 6.1.3.6 (Serial Powering): Serial power supplies produce a constant current up to 8 A per serial power chain and provide a voltage of 1.5-2.0 V per module, with a maximum of 16 modules per chain.

R&D

CQ.2

- 6.1.3.1: Flex
  - Flex design is completed. Production in FY20.

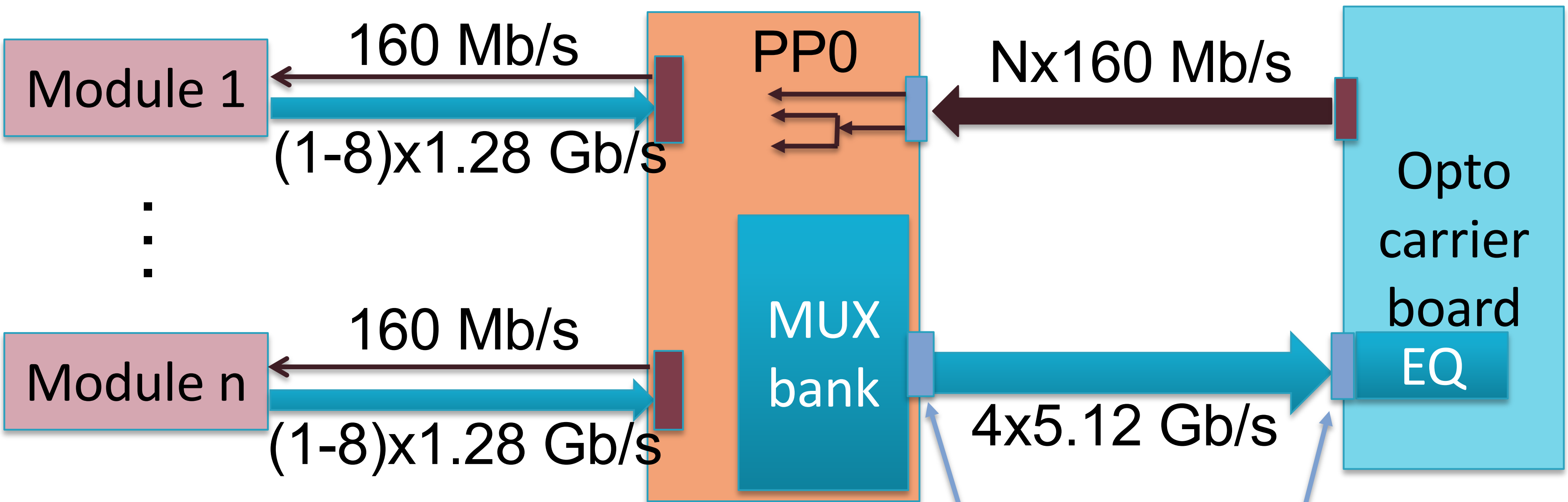




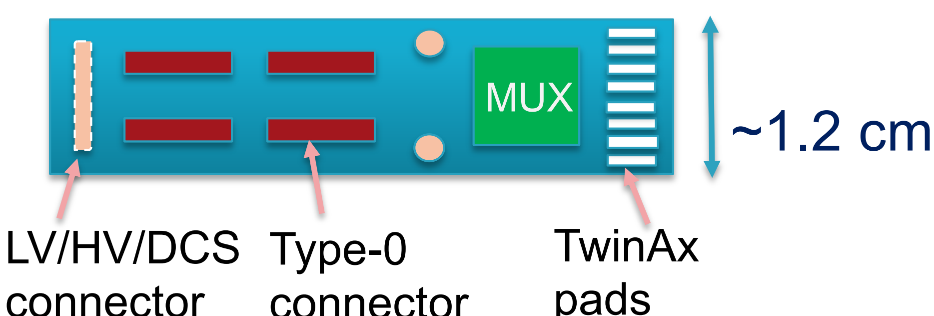
R&D

CQ.2

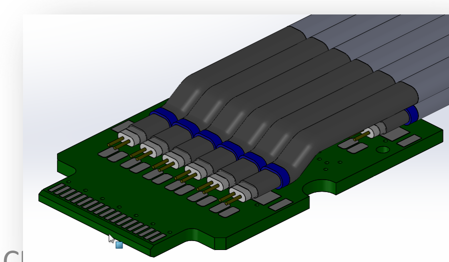
- 6.1.3.2: PP0
  - PP0: Initial conceptual design completed. Production in FY21.



PP0 model for barrel Layer 0



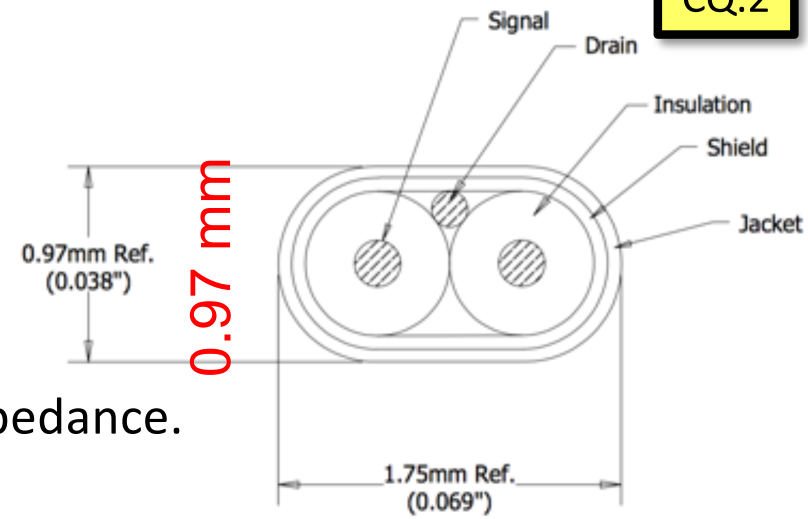
Soldering termination similar to ALICE SAMTEC/UEC5 custom solution



R&D

CQ.2

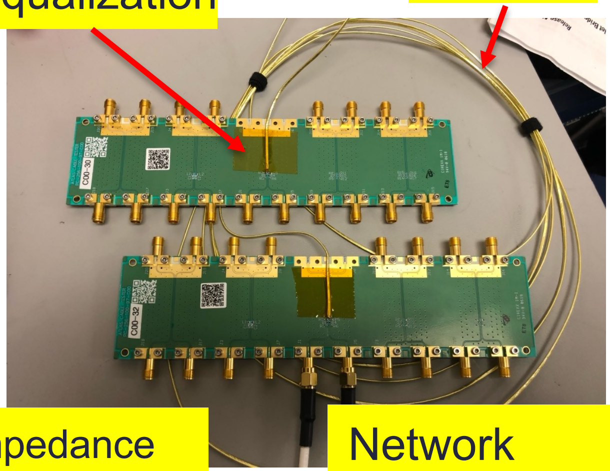
- 6.1.3.3: TwinAX
  - Custom development with TempFlex in 2009
  - Now Molex catalog item.
  - Negligible degradation after 10^{16} protons/cm^2
  - CC-Al wire and LDPE dielectric with 100 Ω impedance.
  - Production in FY20.



1.75 mm

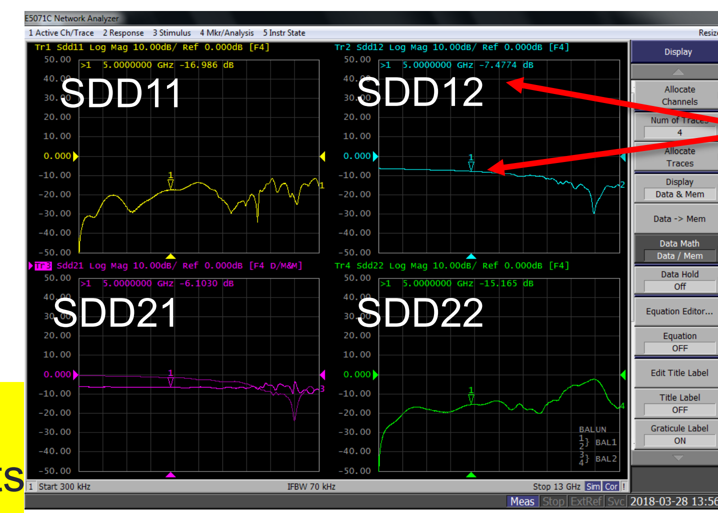
Equalization

TwinAx



Impedance matched test termination boards

Network Analyzer ports



S-parameter
-7.5 dB @ 5 GHz
for 6 m cable
vs. spec
-20 dB @ 3 GHz
with connections

R&D

CQ.2

- 6.1.3.4: Type-I Cable
  - Characterize S parameters of cables with various gauge and dielectric material.
  - Fabricated mechanical prototype of 32 shielded 36 AWG twisted pairs.
  - Production in FY20.

R&D

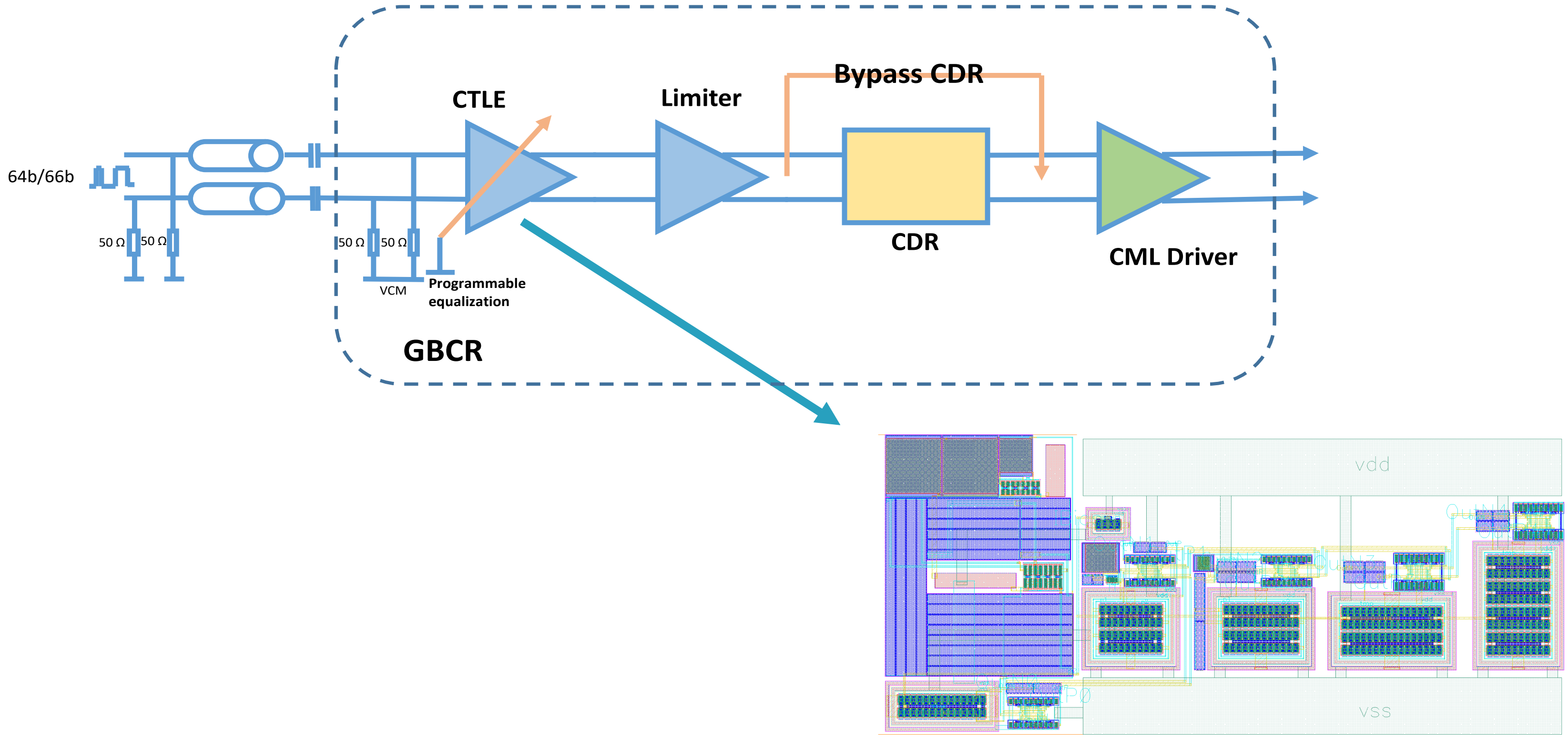
CQ.2

- 6.1.3.6: Serial Power Supply
  - Produced two prototype power supplies. Currently updating the design.
  - Fabricated automated test stand
  - Production in FY23.

R&D

CQ.2

- 6.1.3.7: Equalizer
  - Design of equalizer circuit and clock recovery circuit started. Layout of CTLE (continuous time linear equalization) completed in TSMC 65 nm CMOS technology. Production in FY20.



Project Management

L3 Project

CQ.5

- **6.01 ITk Pixels**
  L2M: P. Grenier (SLAC)
  Deputy: J. Metcalfe (ANL)
  - 6.01.01 Mechanics — L3M: J. Love (ANL)
    - 6.01.01.01 IST UW — IC: H. Lubati (U.Wash)
    - 6.01.01.02 IST LBNL — IC: E. Anderssen (LBNL)
    - 6.01.01.03 PP1 ANL — IC: J. Love (ANL)
    - 6.01.01.04 1/4 Shell — IC: N. Hartman (LBNL)
  - 6.01.02 Local Supports — L3M: M. Hance (UCSC)
    - 6.01.02.01 Cooling — IC: J. Proudfoot (ANL)
    - 6.01.02.02 Local Supp. — IC: E. Anderssen (LBNL)
    - 6.01.02.03 Tests — IC: R. Lopes de Sa (U.Mass)
  - 6.01.03 Comm/Power — L3M: K.K. Gan (Ohio)
    - 6.01.03.01 Typ-0 Serv — IC: S. Welch (OK State)
    - 6.01.03.02 PP0 — IC: Su Dong (SLAC)
    - 6.01.03.03 Twinax — IC: Su Dong (SLAC)
    - 6.01.03.04 Typ-1 Serv. — IC: J. Nielsen (UCSC)
    - 6.01.03.05 Optical Lnk — IC: K.K. Gan (Ohio)
    - 6.01.03.06 Serial Pwr — IC: S. Welch (OK State)
    - 6.01.03.07 Equalizer — IC: J. Ye (SMU)
  - 6.01.04 FE Chip — L3M: M. Garcia-Sciveres (LBNL)
    - 6.01.04.01 Chip LBNL — IC: M. Garcia-Sciveres (LBNL)
    - 6.01.04.02 Chip UW — IC: S-C. Hsu (U.Wash)
    - 6.01.04.03 Chip UCSC — IC: J. Nielsen (UCSC)
  - 6.01.05 Modules — L3M: J. Metcalfe (ANL)
    - 6.01.05.01 Mdl's ANL — IC: J. Metcalfe (ANL)
    - 6.01.05.02 Mdl's LBNL — IC: M. Garcia-Sciveres (LBNL)
    - 6.01.05.03 Test UCSC — IC: J. Nielsen (UCSC)
    - 6.01.05.04 Test OKU — IC: P. Gutierrez (OKU)
    - 6.01.05.05 Test Wisc — IC: C. Zhou (Wisconsin)
  - 6.01.06 Integration — L3M: M. Hance (UCSC)
    - 6.01.06.01 Loading — IC: C. Young (SLAC)

L3 Project

CQ.5

- 6.1.3.1+6.1.3.6: flex circuit and power supply
  - Oklahoma State: F. Rizatdinova leads the effort with S. Welch as the lead engineer at cost.
  - Cost estimate mostly based on quotes and data from previous hardware development projects
- 6.1.3.2+6.1.3.3: PP0/TwinAx
  - SLAC: Su Dong leads the effort with contributions from physicists plus engineers and technicians available at cost.
  - TwinAX cost estimate based on several years of R&D and PP0 based on fabricating similar objects for Insertable Barrel Layer (IBL) of ATLAS Pixel detector

L3 Project

CQ.5

- 6.1.3.4: Type-I bundle
  - UCSC: J. Nielson leads the effort with contributions from physicists plus engineers and technicians at cost.
  - Cost estimate based on similar objects for Insertable Barrel Layer (IBL) of ATLAS Pixel detector
- 6.1.3.5: Opto carrier board
  - Ohio State: K.K. Gan leads the effort with contributions from physicists plus engineers and technicians at cost.
  - Cost estimate based on building two generations of opto-boards for the Pixel detector of ATLAS
- 6.1.3.7: Equalizer
  - SMU: J. Ye leads the effort with contributions from engineers and technicians at cost.
  - Cost estimate based on design/prototyping of other ASICs

ES&H

CQ.6

- Safety is of the highest priority within the Project
  - Work at each institute adheres strictly to its ES&H policies

Institute	Institute ES&H Contact
Ohio State	M. St. Clair (https://ehs.osu.edu)
Oklahoma State	K. Southworth (https://ehs.okstate.edu)
SLAC	C. Fried (http://www-group.slac.stanford.edu/esh/)
SMU	B. Chance (https://www.smu.edu/BusinessFinance/RiskManagement/Health-Safety)
UC Santa Cruz	L. Wisser (https://ehs.ucsc.edu)

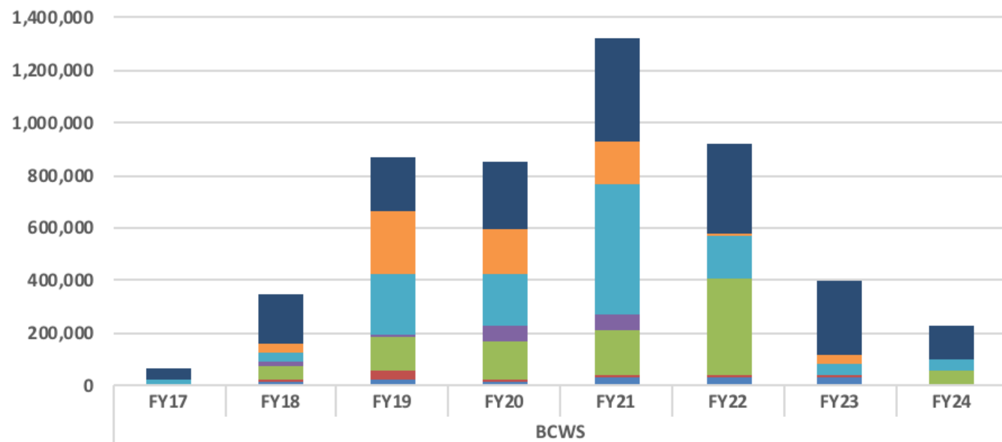
  - The BNL ES&H Liaison provides oversight and advice
  - US ATLAS HL-LHC Institute Contacts act as interfaces between their institute and BNL and CERN
- Main Hazards for this Deliverable
  - Radiation: test beams are in controlled areas
  - All work done in compliance with safety policies at the institute or CERN

Cost and Schedule

Budget & Effort

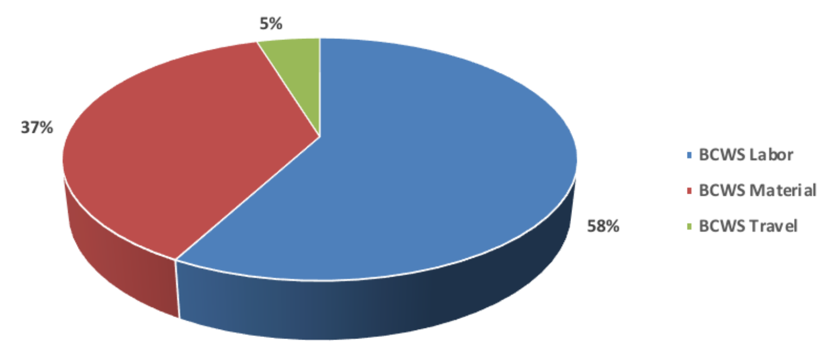
CQ.4

WBS 6.01.03 Chart - L3 Ttl Cost by Res Category



	FY17	FY18	FY19	FY20	FY21	FY22	FY23	FY24
ENG	43,397	188,731	204,352	257,507	394,849	338,299	282,241	127,123
EQUIP		38,110	239,703	166,090	157,570	13,912	29,912	
MAT	19,320	29,834	230,498	198,366	497,888	158,161	41,784	46,498
STU		16,157	7,204	57,762	57,901			
TECH	157	55,862	126,645	144,969	174,787	367,081		49,355
TRAVD		6,969	35,058	6,373	11,924	12,152	12,187	
TRAVF	4,374	13,516	22,646	19,118	28,443	28,734	29,872	5,380

WBS 6.01.03 Chart - L3 Lbr Mat and Trvl (%)



Schedule

CQ.3

- Items needed at SLAC integration in 2022:
  - 6.1.3.1: flex circuits
  - 6.1.3.2: PP0
  - 6.1.3.3: TwinAx
  - 6.1.3.4: Type-I bundles
- Items needed at CERN in 2024:
  - 6.1.3.5: opto carrier boards
  - 6.1.3.6: serial power supplies
  - 6.1.3.7: equalizer
- Main external dependencies:
  - System test: FE modules + cables + opto-links for operation at 5.12 Gb/s

Risk and Uncertainty

CQ.1

- RD-06-01-03-001: 5 Gb/s data transmission speed not achievable
  - Response: use slightly larger TwinAx cables or double the number of data cables to operate at 2.56 G/s, and/or operate at lower bandwidth and make use of data compression.
  - Mitigation: allocate more resource in connectorization
  - Cost: $9K-$12K
  - Delay: 2-4 months
- RD-06-01-03-002: Serial powering fails to meet specifications
  - Response: allocate more resource for prototyping and use new cables instead of the existing cables.
  - Mitigation: more prototyping of power supply and study of the cooling requirement
  - Cost: $70K-$120K
  - Delay: 2-4 months

Milestones

CQ.3

- FY19: Flex FDR
- FY19: TwinAx FDR
- FY19: Type-I bundle FDR
- FY20: Flex PRR
- FY20: TwinAx PRR
- FY20: Type-I bundle PRR
- FY21: PP0 FDR
- FY21: PP0 PRR
- FY22: Power supply PDR
- FY23: Power supply PRR

Closing Remarks

- Communication and Services WBS contains both active and passive deliverables
- Some R&D are well advanced and others just started
- Main technical challenge:
  - Achieve 5.12 Gb/s data transmission at up to 5.5 m of TwinAx + connectors from FE modules to equalizer ASIC to optical convertor with less then 20 dB of attenuation
    - Already achieve bandwidth of 5.12 Gb/s with up to 5.5 m of TwinAx + commercial components

BACKUP

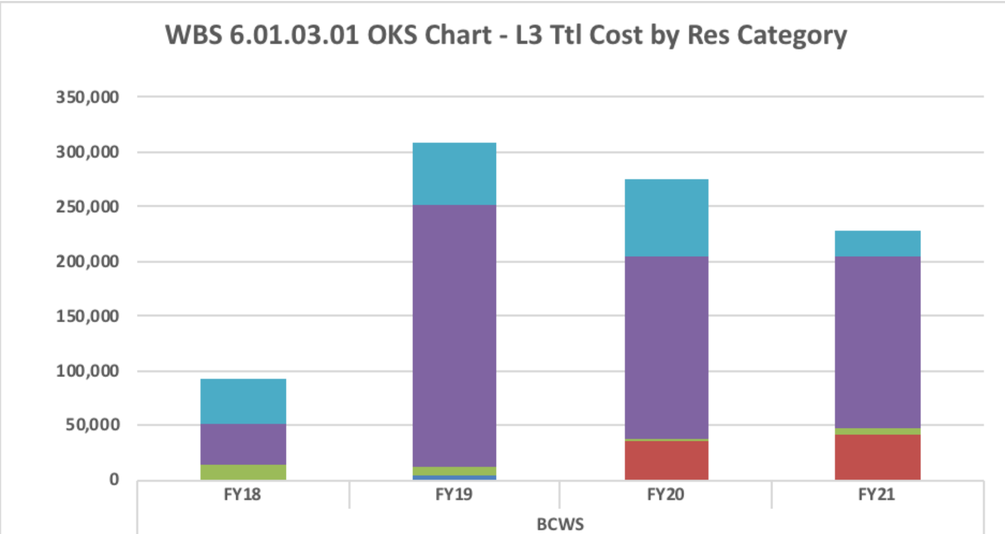
Bio Sketch of L3 Manager

- K.K. Gan, Professor of Physics, The Ohio State University
- Member of ATLAS since 1998
- Leading the design and fabrication of two generations of optical links for the ATLAS pixel detector

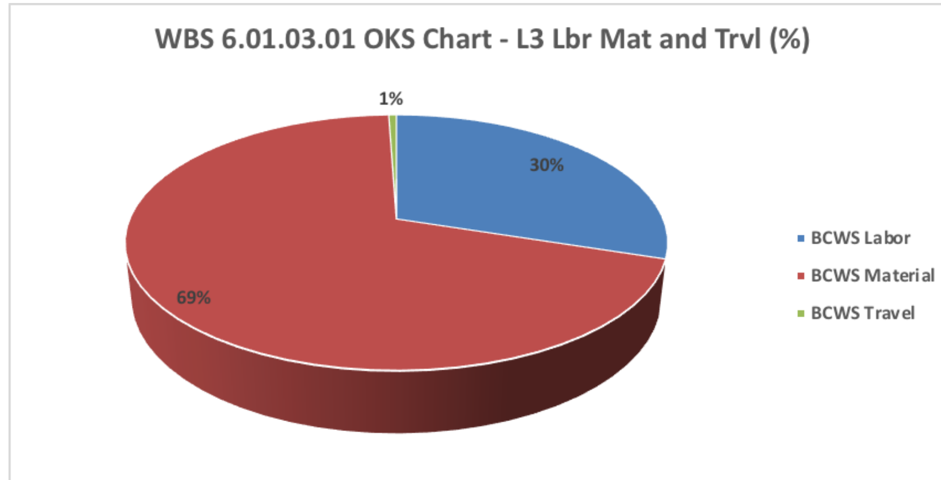
Institute Capabilities

- 6.1.3.1, 6.1.3.6, Oklahoma State:
  - Good facility for electronics development and fabrication
  - One engineer available at cost
  - Previously involved in the Insertable B-Layer pixel project
- 6.1.3.2, 6.1.3.3, SLAC:
  - Large facility for electronics development and fabrication
  - Large pool of engineers and technician available at cost
  - Previously involved in the Insertable B-Layer pixel project
- 6.1.3.4, UC Santa Cruz:
  - Good facility for electronics development and fabrication
  - Pool of engineers and technician available at cost
  - Previously involved in the Insertable B-Layer pixel project
- 6.1.3.5, Ohio State:
  - Clean room with automatic wire bonders and probe stations etc.
  - Engineers and technicians available at cost
  - Previously leading two ATLAS pixel opto-link projects
- 6.1.3.7, Southern Methodist:
  - Good facility for optical electronics development
  - Engineers available at cost
  - Previously leading ATLAS LAr opto-link projects

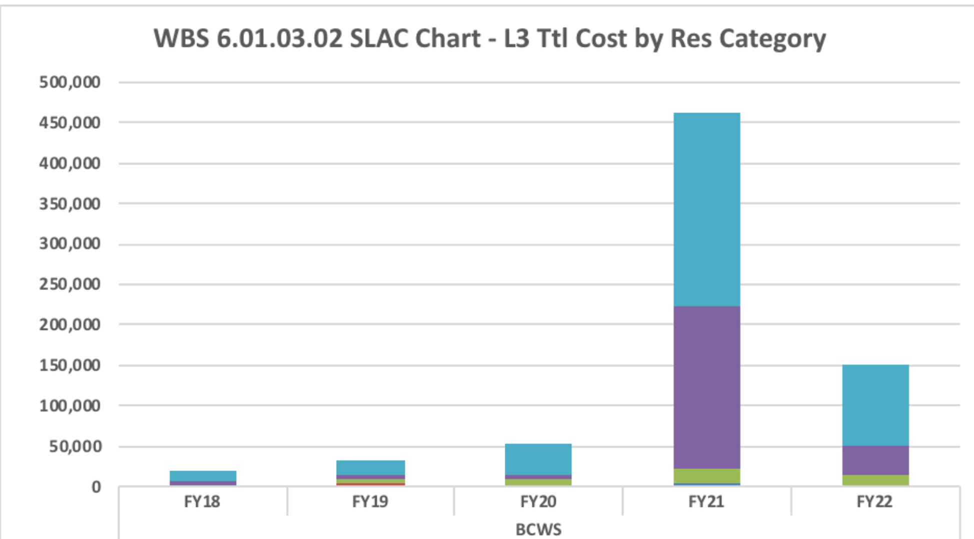
Budget & Effort



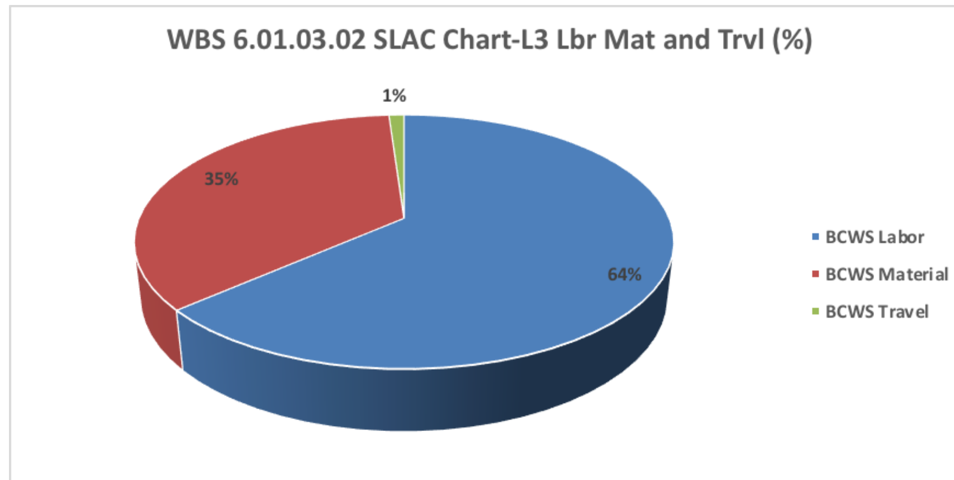
	FY18	FY19	FY20	FY21
ENG	40,330	58,354	72,327	23,084
EQUIP	38,110	239,703	166,090	157,570
MAT	13,516	6,187	2,868	4,102
STU			34,556	42,142
TRAVD		4,933		



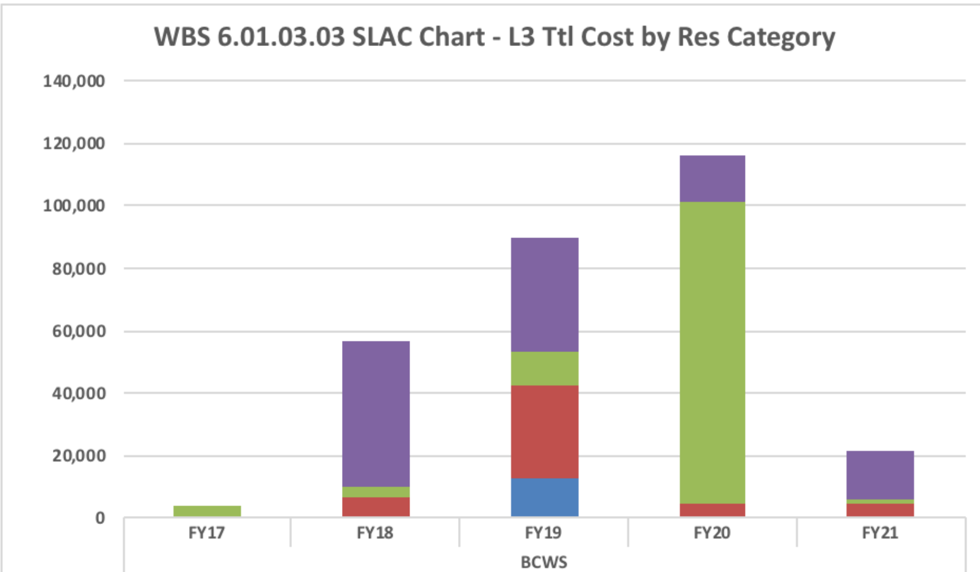
Budget & Effort



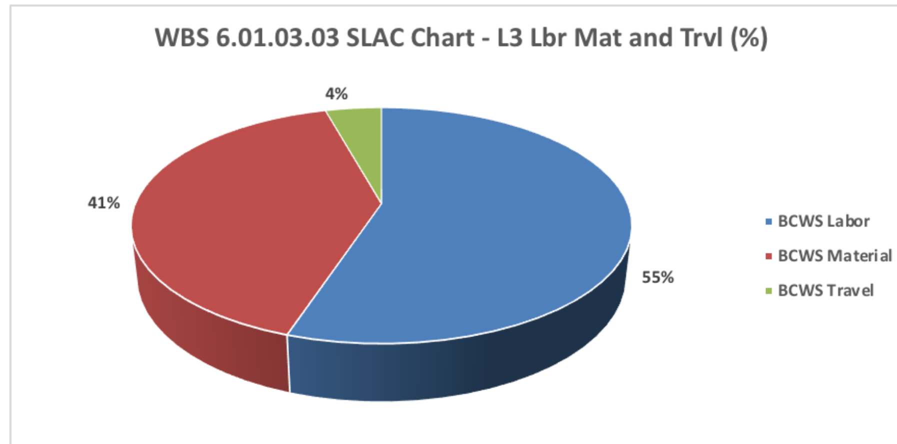
	FY18	FY19	FY20	FY21	FY22
ENG	11,659	18,764	37,106	238,279	99,445
MAT	5,241	5,932	6,110	201,346	35,617
TECH	2,980	5,430	9,484	18,034	15,480
TRAVD		3,324			
TRAVF				4,418	



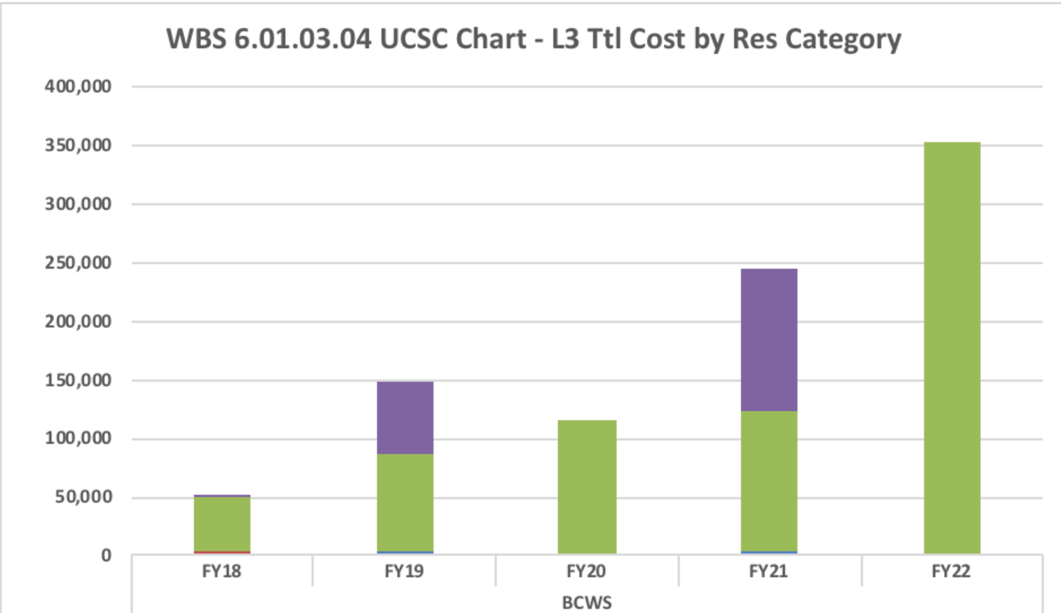
Budget & Effort



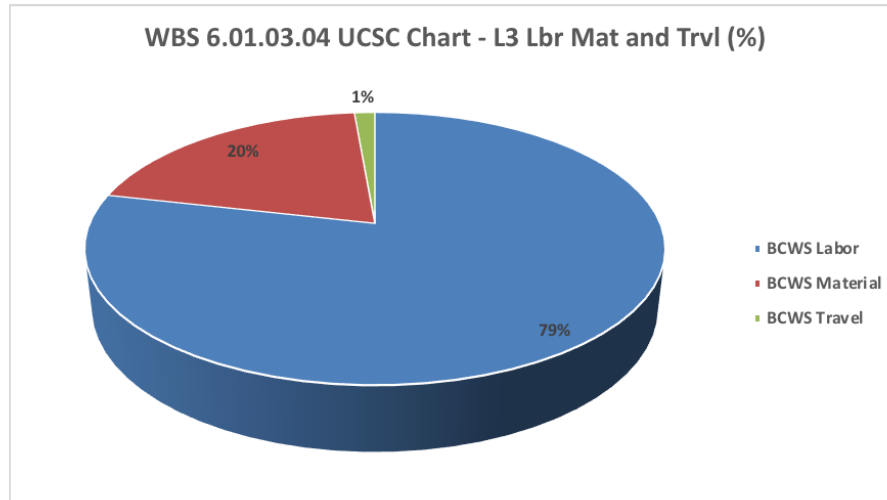
	FY17	FY18	FY19	FY20	FY21
ENG		46,640	36,030	14,844	15,926
MAT	3,947	3,998	11,034	96,753	1,259
TECH	157	6,371	30,102	4,377	4,508
TRAVD			12,467		



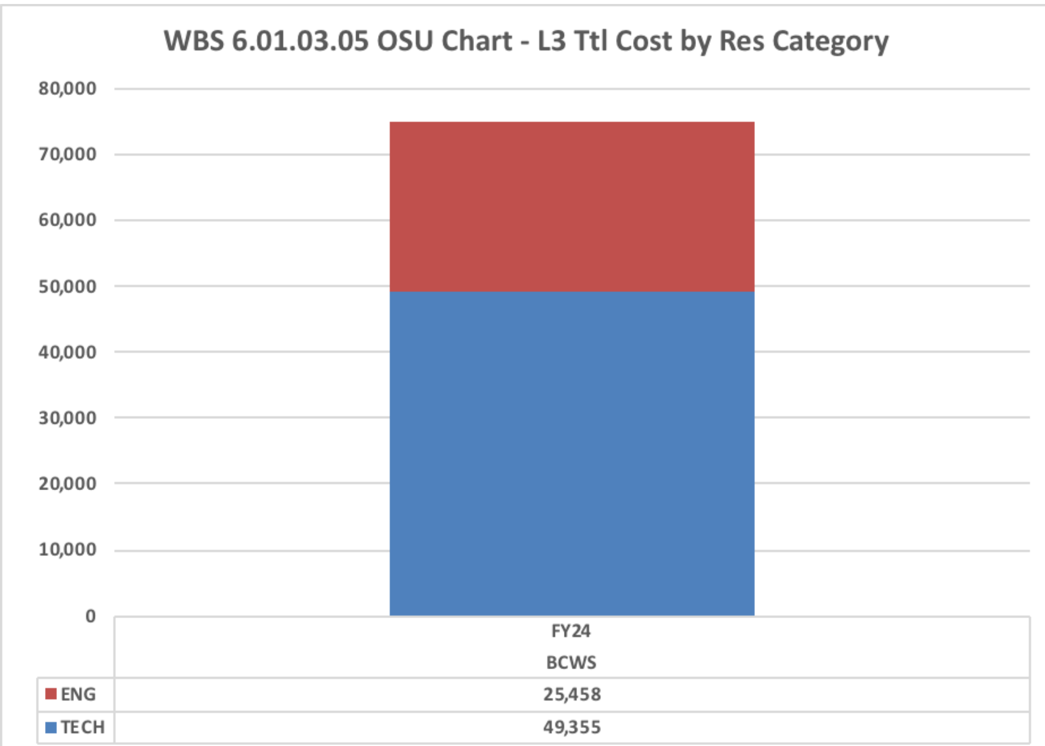
Budget & Effort

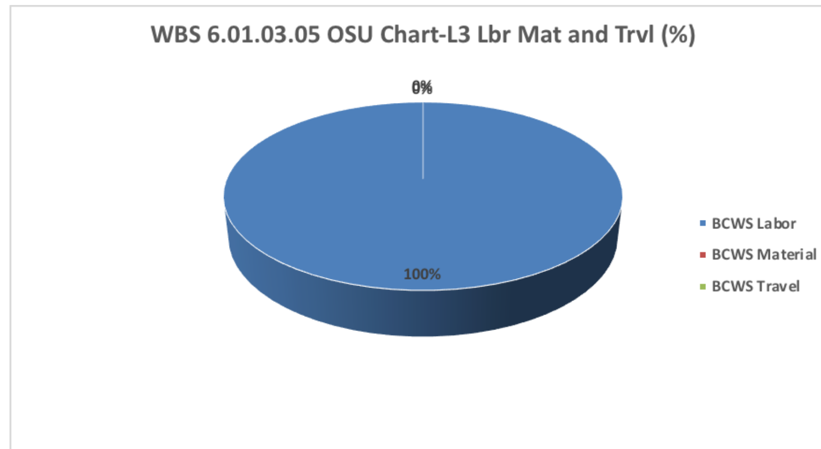


	FY18	FY19	FY20	FY21	FY22
MAT	238	61,001		121,329	
TECH	46,511	83,300	115,070	118,335	351,602
TRAVD	3,966				
TRAVF		4,084		4,333	

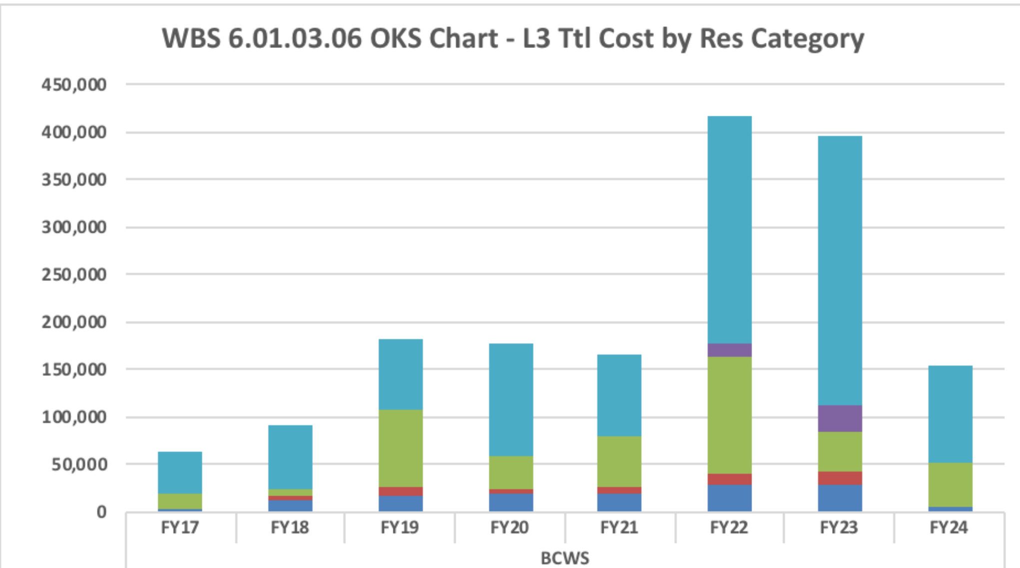


Budget & Effort

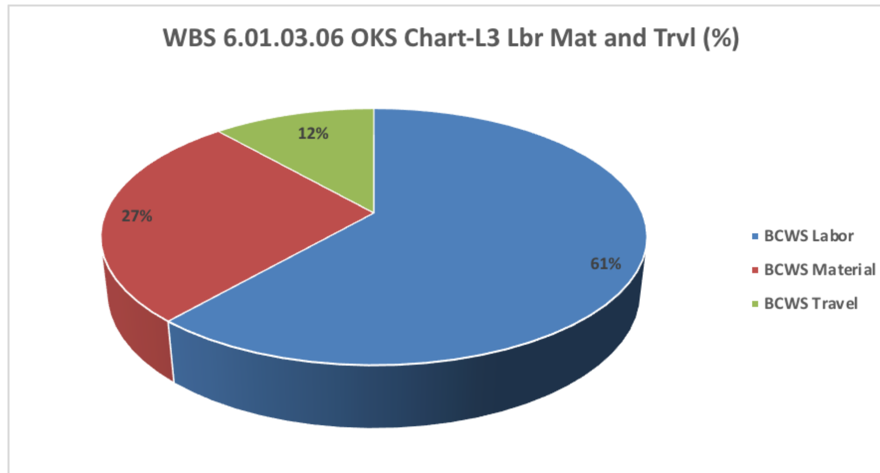




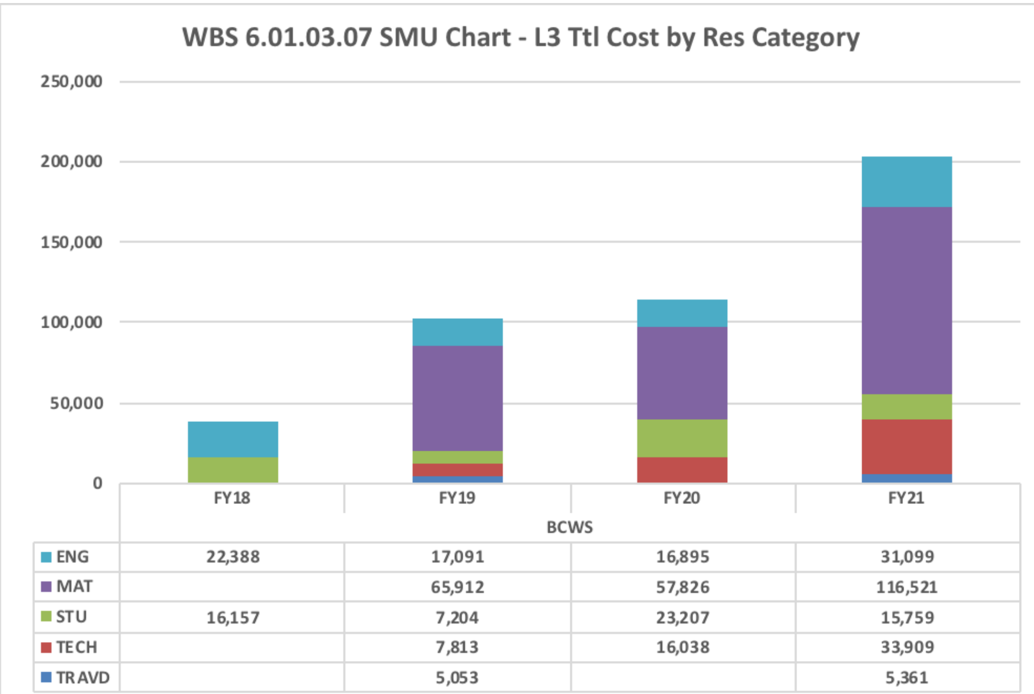
Budget & Effort



	FY17	FY18	FY19	FY20	FY21	FY22	FY23	FY24
ENG	43,397	67,713	74,113	116,335	86,460	238,854	282,241	101,666
EQUIP						13,912	29,912	
MAT	15,373	6,842	80,433	34,810	53,332	122,544	41,784	46,498
TRAVD		3,003	9,281	6,373	6,564	12,152	12,187	
TRAVF	4,374	13,516	18,562	19,118	19,692	28,734	29,872	5,380



Budget & Effort



	FY18	FY19	FY20	FY21
ENG	22,388	17,091	16,895	31,099
MAT		65,912	57,826	116,521
STU	16,157	7,204	23,207	15,759
TECH		7,813	16,038	33,909
TRAVD		5,053		5,361