Design and Fabrication of a Radiation-Hard 500-MHz Digitizer Using Deep Submicron Technology

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Outline

- NLC Requirements
- ADC Design
- Progress Report
- Plans

Beam Position Monitor Requirements at NLC

- NLC will collide 180-bunch trains of e^- and e^+:
  - bunch spacing: 1.4 ns
  - alignment of individual bunches in a train: < 1 □m
  - BPM determines bunch-to-bunch misalignment
  - ⇨ high bandwidth kickers bring the train into better alignment on next machine cycle
  - ⇨ multi-bunch BPM system with digitizers:
    - ★ 11-bit effective resolution
    - ★ 500 MHz bandwidth
    - ★ 2 G samples/s

Requirements of NLC Digitizers

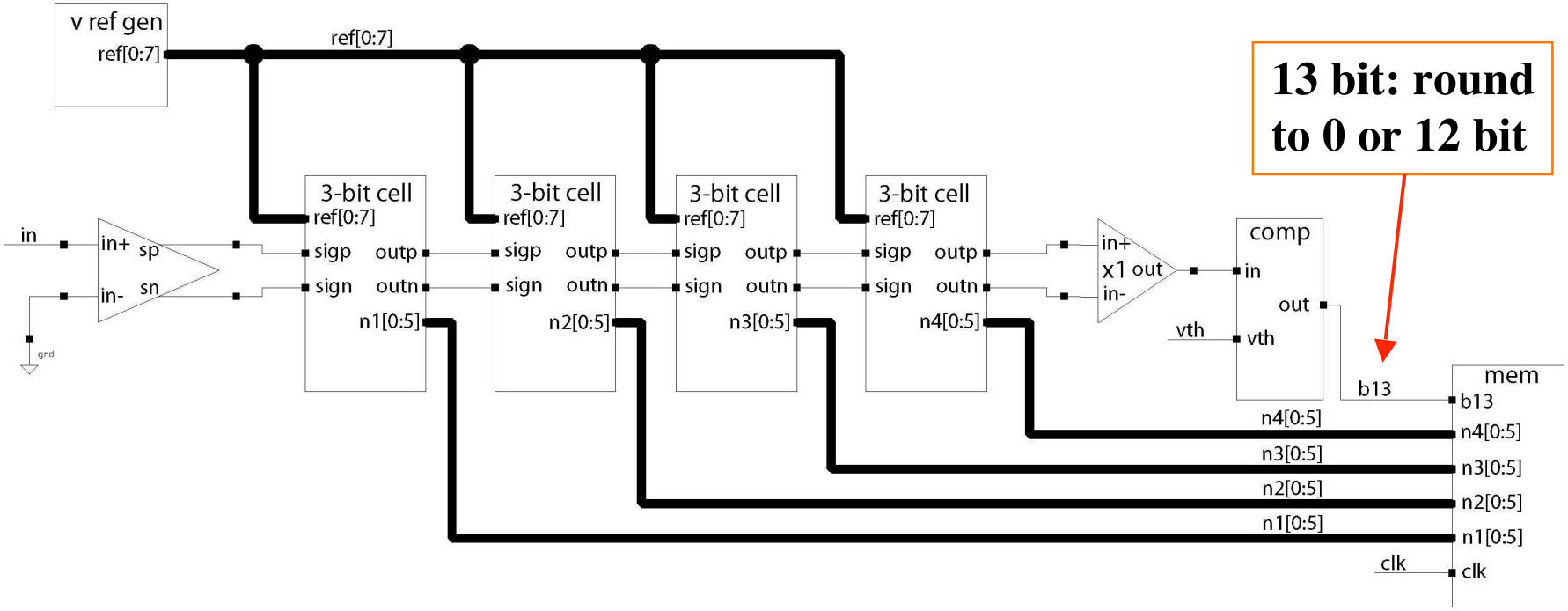
Function	Qty.	Resolution (eff. bits)	Bandwidth (MHz)	Comments
LLRF Control	13,000	11	100	Slightly beyond state-of-the-art
Structure BPM	22,000	8	5	Existing technology
"Qaud" BPM	10,000	11	12	Existing technology
Multi-bunch BPM	1,200	11	500	Well beyond state-of-the-art
Total	46,200			

- important to demonstrate feasibility of high speed/resolution digitizers
- ⇨ redesign of low level RF technology is needed without the digitizers

Proposal

- design a digitizer chip using deep-submicron technology (0.25 μm)
  - use enclosed layout transistors and guard rings
    - ⇨ radiation hard: > 60 Mrad
    - ⇨ no need for costly shielding and long cables
    - ⇨ readily access to electronics for testing and maintenance
- extensive experience in chip design using Cadence
  - designed radiation-hard chips for CLEO III, ATLAS, CMS
- why OSU is interested?
  - help to solve a challenging NLC problem
  - potential applications in HEP
- 2002 Holtkamp Committee ranking: 2 on scale of 1 to 4 (lowest)
  - ⇨ funded for 2003-4

12-bit Pipelined Digitizer



- input crudely digitized by 1st 3-bit cell
- ⇨ digitized value subtracted from input
- ⇨ difference is amplified by 8 and sent to 2nd 3-bit cell…

Digitizer for Multi-bunch BPM

- most challenging digitizer: 11 bit, 2 G samples/s, 500 MHz bandwidth
- input: sequence of doublets at 1.4 ns batch spacing
  - characterize with one parameter: pulse height
  - minimum sampling: 1/1.4 ns = 714 MHz
    - ⇨ interleaving 3 digitizers for redundancy
      - ⇨ 2 G samples/s

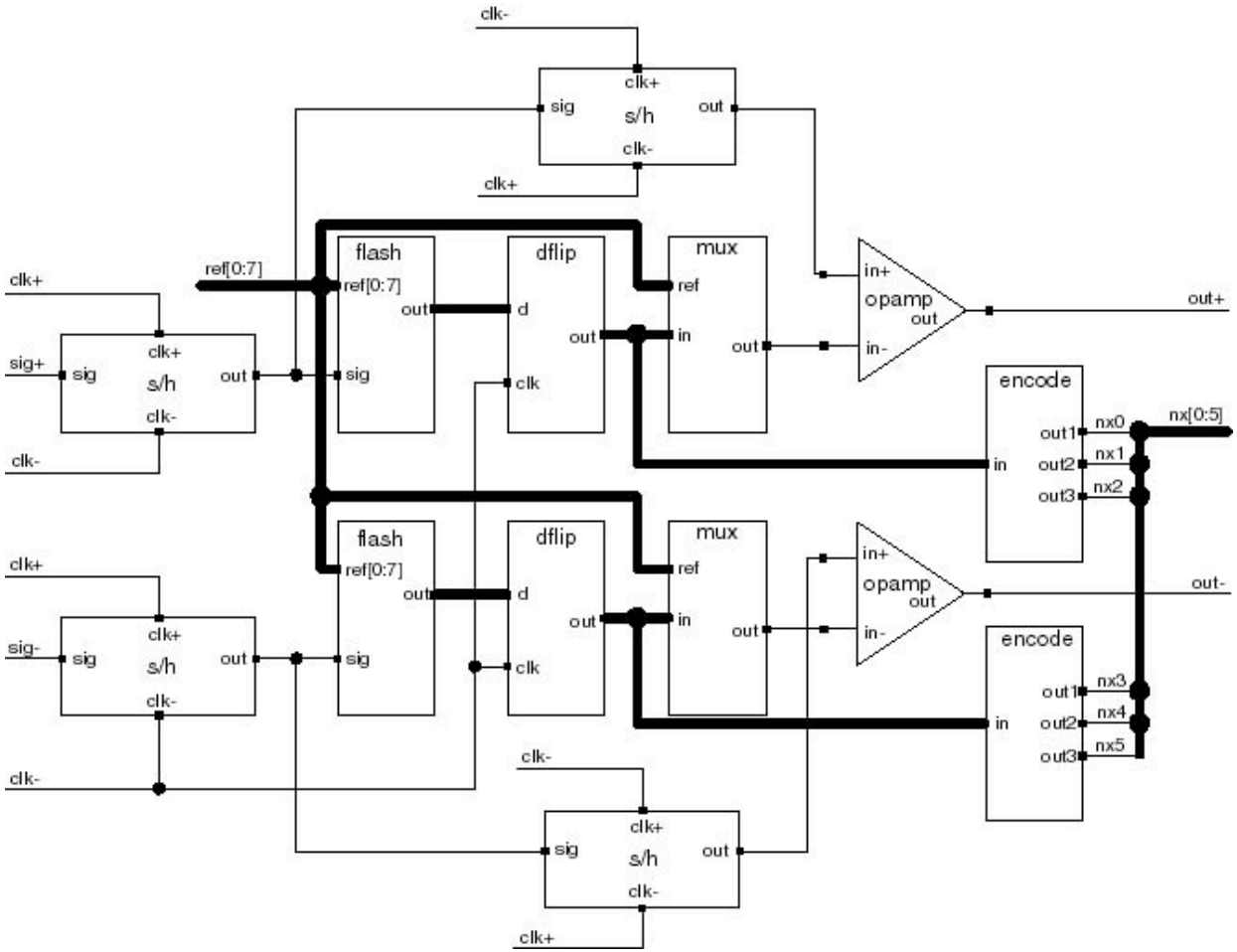
Precision

- submicron CMOS supply voltage: 2.5 V
  - ⇨ differential signal: ~ 1.6 V full swing
  - ⇨ LSB: 1.6 V/2^{12} = 390 □V
  - ⇨ stability/accuracy of comparator thresholds, amplifier & S/H gains, charge injection: 195 □V = 0.5 LSB = 0.5/2^{12} = 0.012%

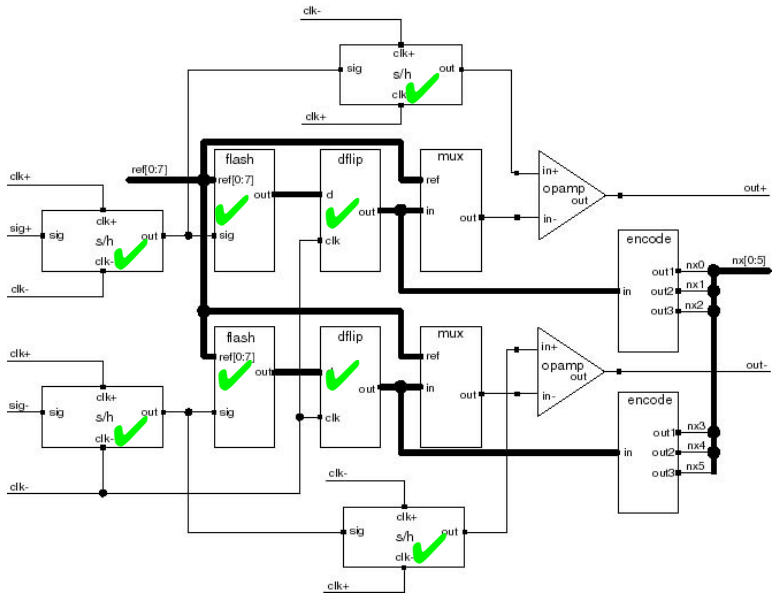
Fabrication Process

- gain-bandwidth requirement:
  - assume 0.7 ns for sample and 0.7 ns for hold
  - settling to 0.5 LSB for 12-bit digitizer requires 9□: $0.5/2^{12} \sim e^{-9}$
    - ⇨ □= 0.7 ns/9 = 78 ps
    - ⇨ rise time = 2.2 □= 171 ps
    - ⇨ gain x bandwidth = 8 x 1/2□□= 16.4 GHz
    - ⇨ IBM process SiGe BiCMOS 6HP/6DM via MOSIS: 40 GHz NPN bipolar transistors

3-Bit Cell

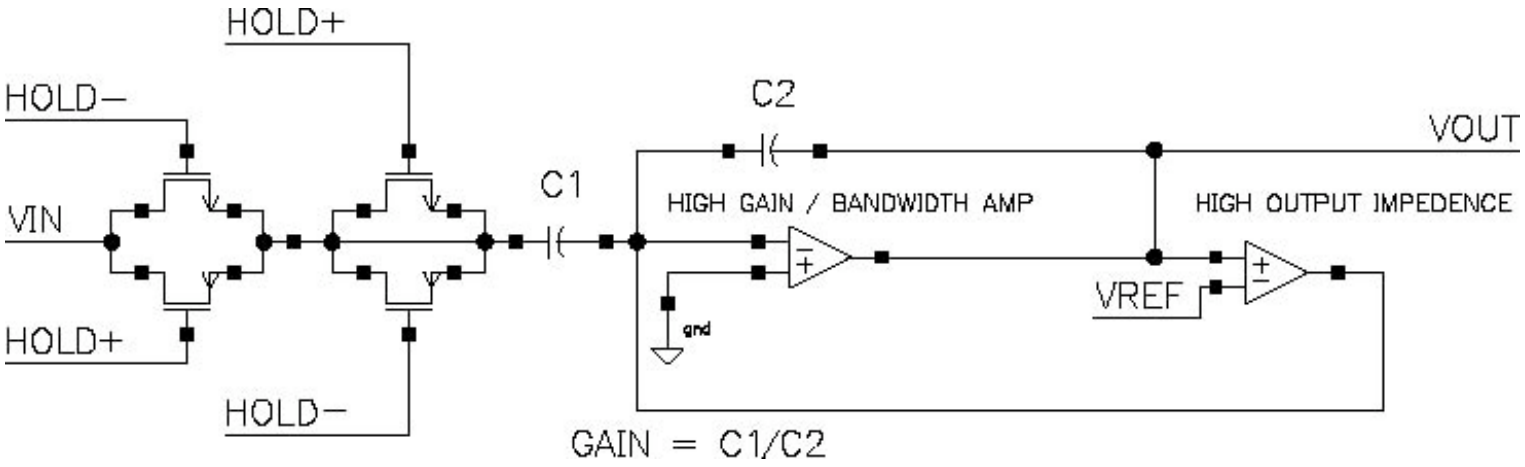

clk-
clk+
sig
s/h
out
clk-
clk+
ref[0:7]
flash
ref[0:7]
out
sig
dflip
d
out
clk
mux
ref
in
out
in+
opamp
out
in-
out+
clk+
sig+
sig
clk+
s/h
out
clk-
clk-
encode
out1
out2
out3
nx0
nx1
nx2
nx[0:5]
clk+
sig-
out-
clk-
nx3
nx4
nx5

3-Bit Cell Status



- simulated with Cadence
  - ✔ sample/hold + flash ADC/flip-flop: designed/simulated from schematic with parasitic capacitances
  - multiplexer: logic is fast but somewhat noisy
  - op-amp + encoder: still use ideal devices in simulation

Sample/Hold Status

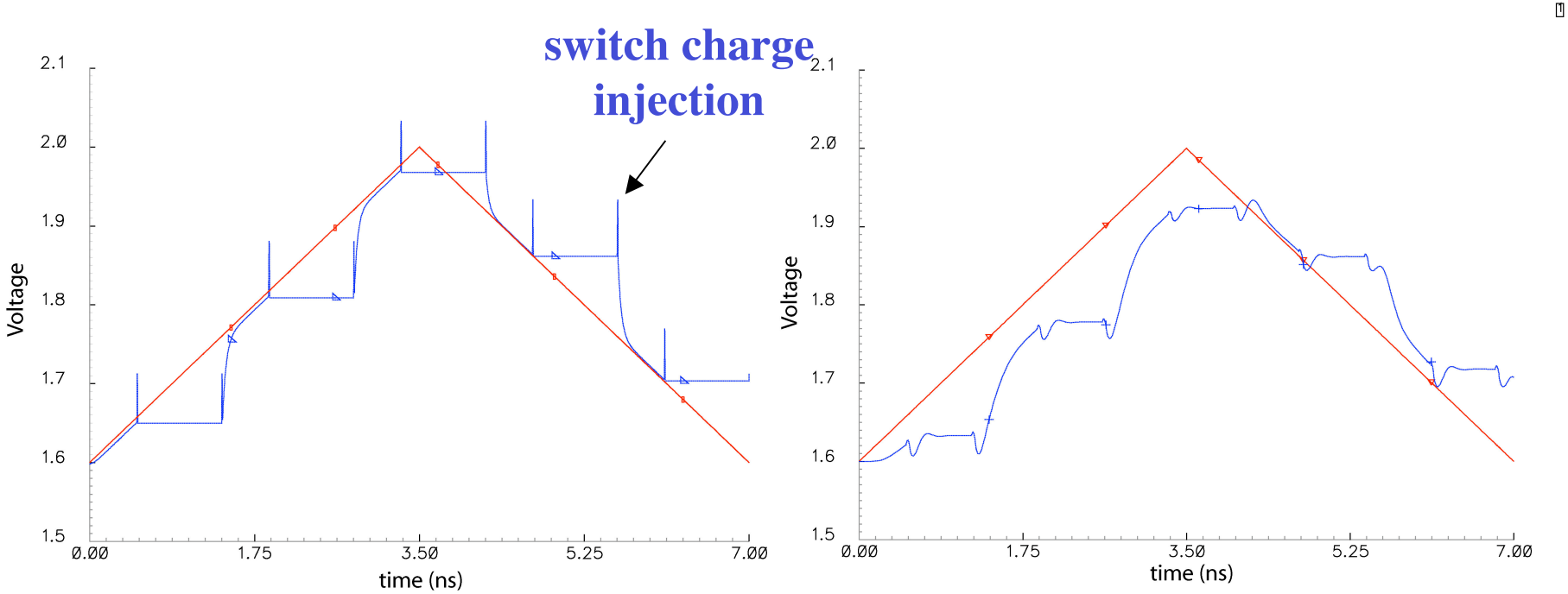


- design and simulated from schematic with parasitic capacitances
  - ✔ switch-on resistance small enough to allow 9□ in 700 ps
  - ✔ switching offset (noise) largely cancelled with dummy switch:
    - ■ 100 mV ⇨ 1 mV

Cadence Simulation of Sample/Hold

Amplifier: ideal

Amplifier: current design



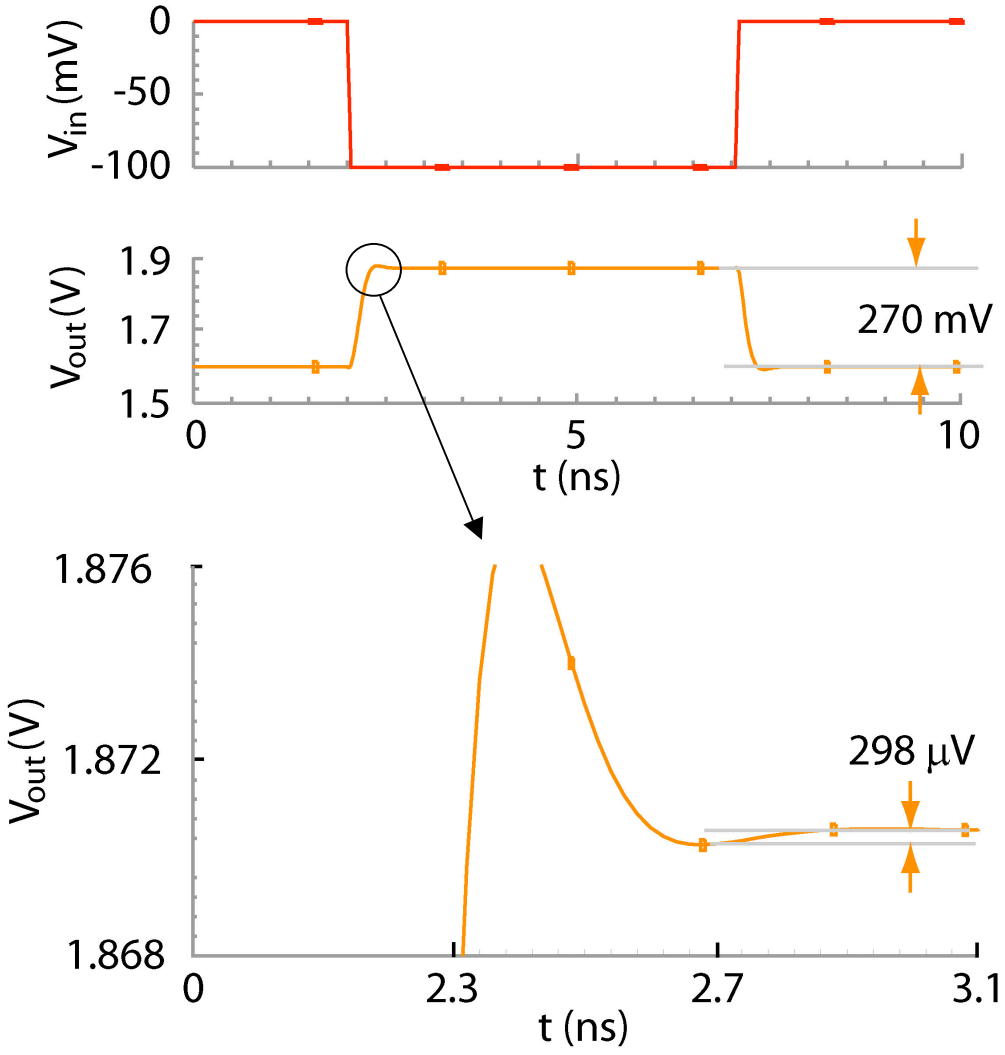
- amplifier signal not yet settle to 0.5 LSB in 0.7 ns

Simulation of Amplifier

- rise time: 186 ps
  - goal: 171 ps:
- precision at 0.7 ns:

$$\frac{298\ \mu V}{270\ mV} \times 2^{10}$$

⇨ need 4x improvement for 12-bit precision



Plans

- Year 2003-4:
  - complete design of amplifier + 3-bit cell
- Year 2004-5:
  - layout, submission, and testing of the building block circuits
  - radiation hardness tests
  - continued system design of a prototype 11-bit digitizer