10 Gb/s Radiation-Hard VCSEL Array Driver

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Outline

- Introduction to a compact solution
- Results with 5 Gb/s VCSEL array driver
- Design of 10 Gb/s VCSEL array driver
- Summary

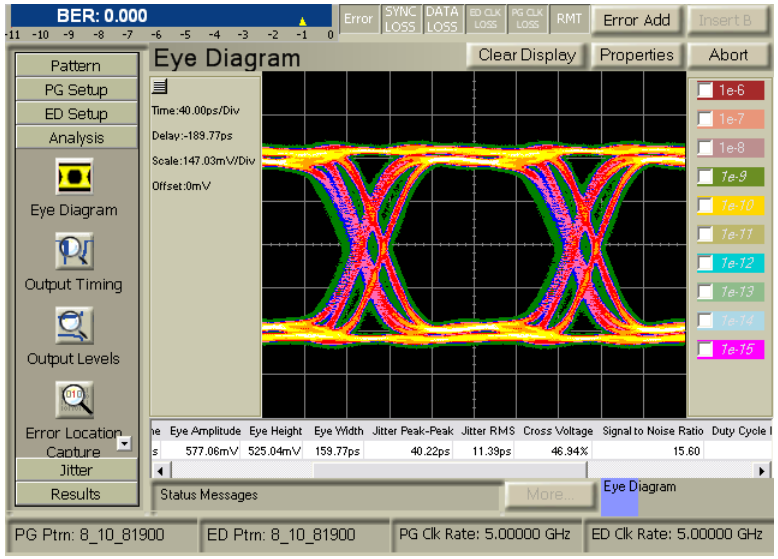
Use of VCSEL Arrays in HEP

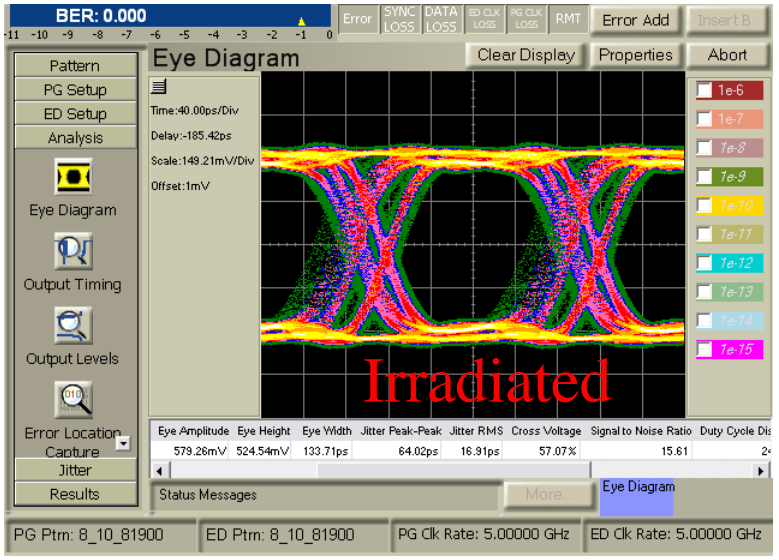
- Widely used in off-detector (no radiation) data transmission
- First on-detector implementation in pixel detector of ATLAS
  - experience has been positive
    - VCSELs used are humidity sensitive but they are installed in very low humidity location
    - modern VCSELs are humidity tolerant
    - opto-links built by OSU have ~0.1% broken links
    - ⇨ use arrays for the replacement optical links for current 3-layer pixel detector and the new inner layer (IBL)
- Currently designing 10 Gb/s VCSEL array driver
  - ⇨ aggregated bandwidth of 120 Gb/s for 12-channel array

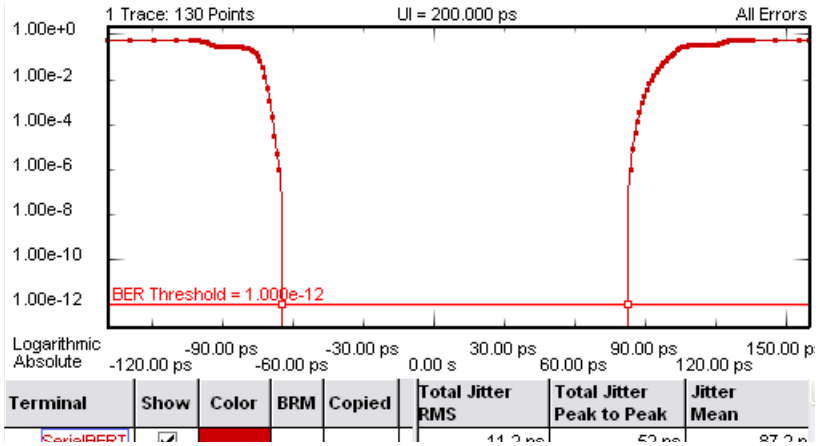
Radiation Hardness of 5 Gb/s Array Driver

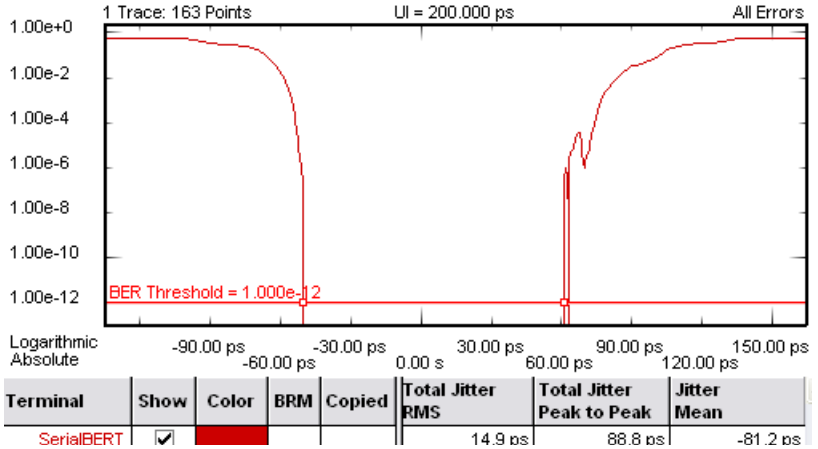
- Have fabricated 12-channel VCSEL array driver
  - 4.5 mm x 1.5 mm ASIC fabricated in 130 nm CMOS
  - LVDS signals from the inner 8 channels can be steered to any of the 4 outer channels designated as spares
  - 8 bit DAC per channel for modulation current
  - Global 8 bit DAC for bias current
- All channels work at 5 Gb/s with BER < 5×10^{-13} for all other channels active
- Performed an irradiation at LANL with 800 MeV protons to 0.92×10^{15} 1 MeV n_{eq}/cm^2
  - 2 chips irradiated (powered)

Irradiated 5 Gb/s Array Driver





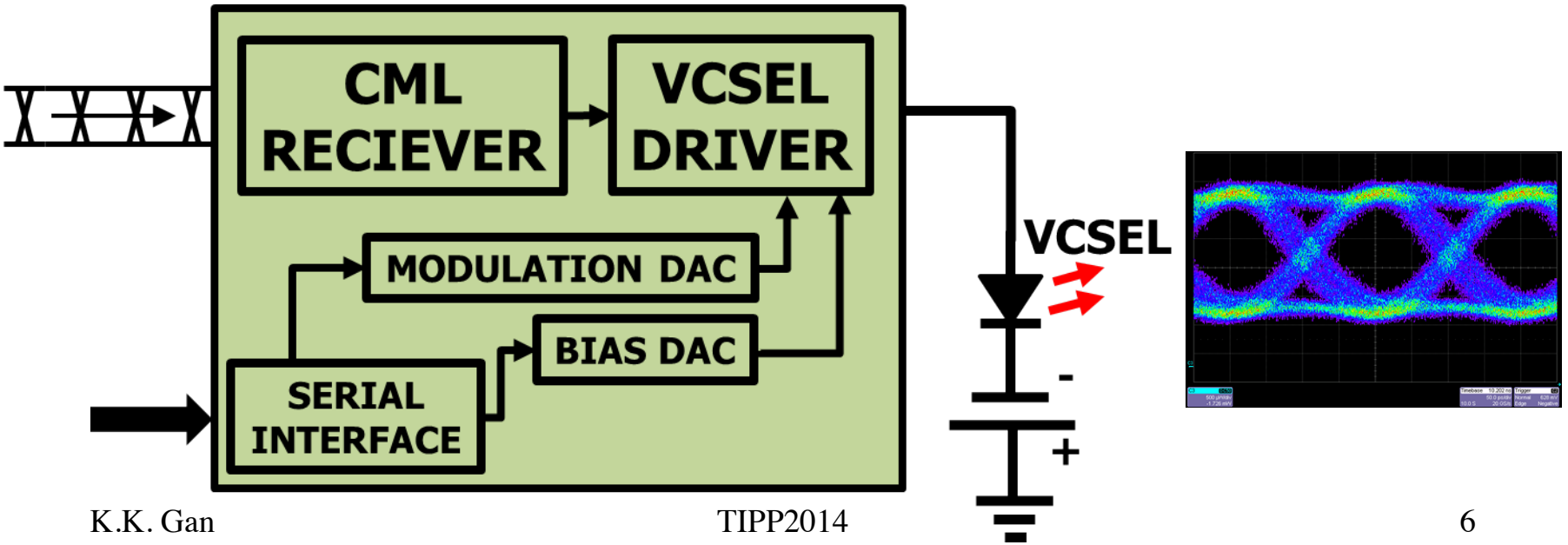




- Measurements after 10 Gb/s SFP+ receiver
- ASIC still works at 5 Gb/s but degraded rise time/jitter performance

10 Gb/s VCSEL Driver

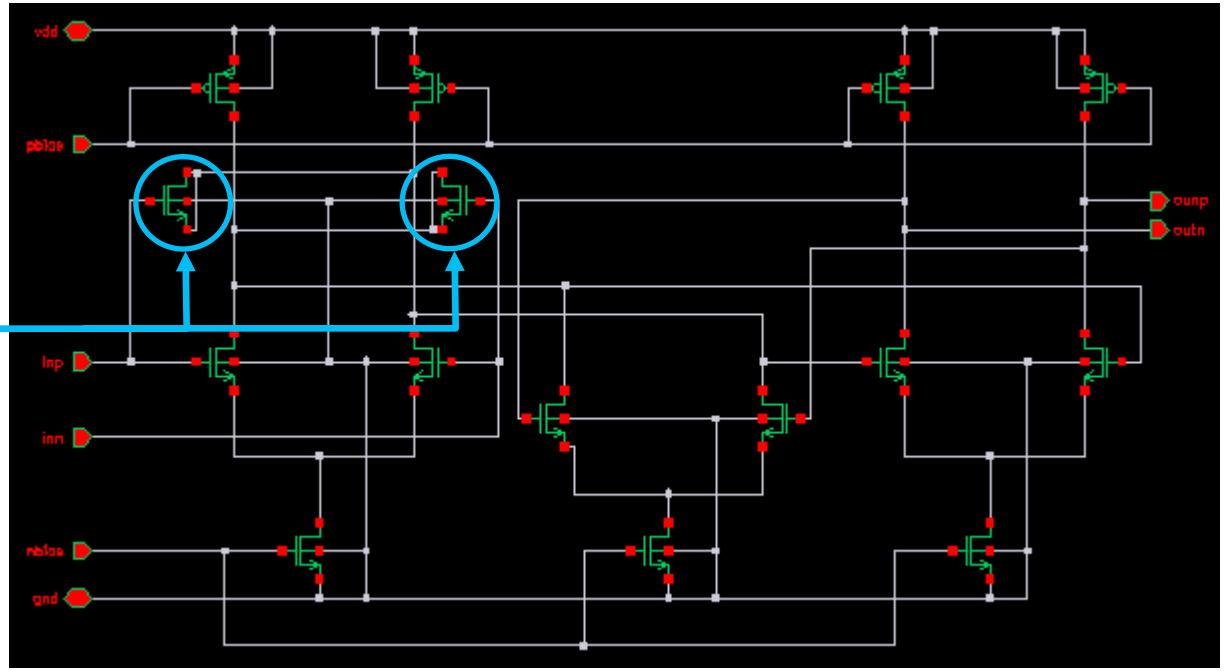
- Presently targeting a commercial 65 nm CMOS process
- Use only core transistors to achieve maximum radiation-hardness
- 8 bit DACs to control the VCSEL modulation and bias currents
- Negative VCSEL cathode bias provides voltage overhead for all other channels active
- Consumes 42 mW (35 mA @ 1.2 V)



CML Receiver

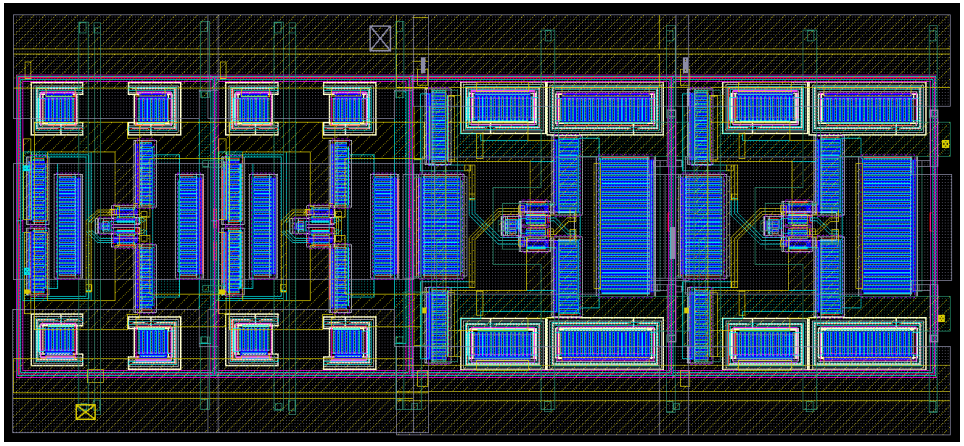
- Input signal is current mode logic (CML)
  - Commonly used in commercial 10 Gb/s links
- CML receiver is a four-stage limiting amplifier
- Each stage is a common mode feedback amplifier with feed forward capacitors on the input differential pair to enhance the higher frequency signal components

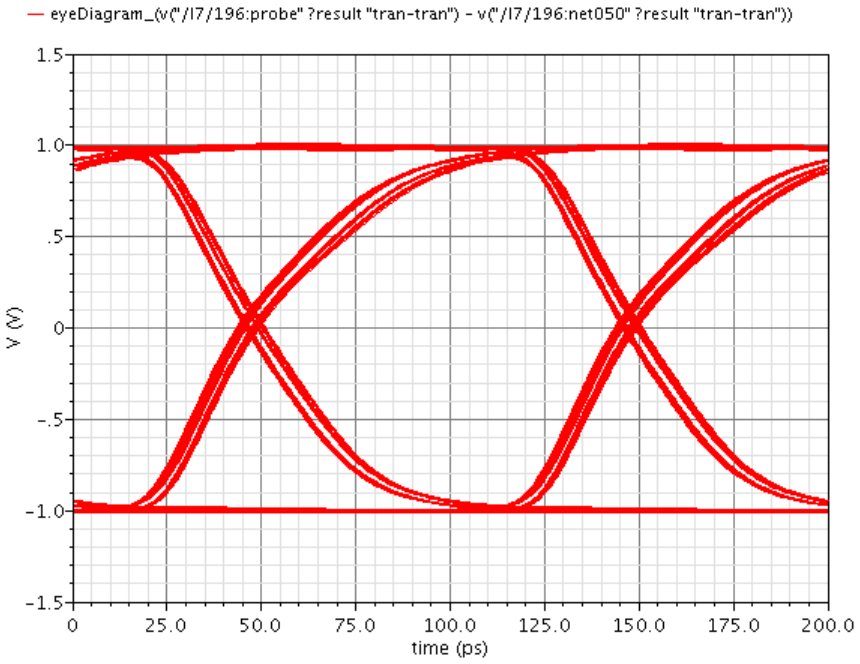
feed forward capacitance



CML Receiver (continued)

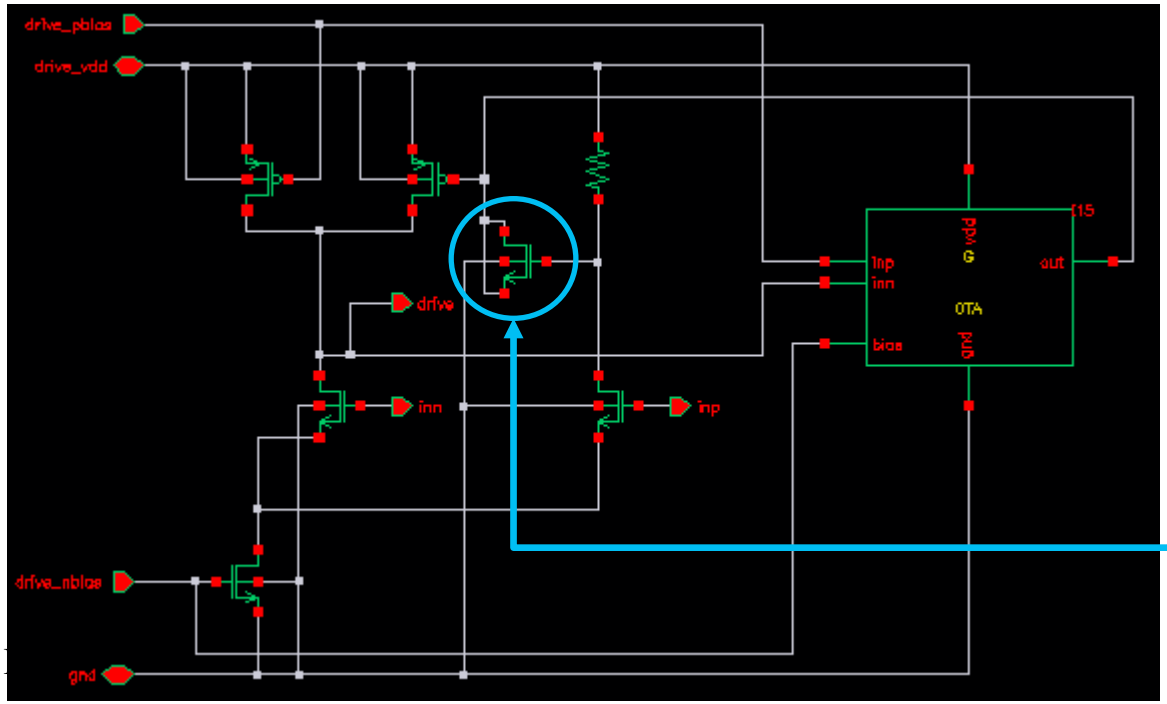
- Layout is 60 μm x 30 μm
- Consumes 26 mW (22 mA @ 1.2 V)
- Extracted layout eye diagram is acceptable





VCSEL Driver

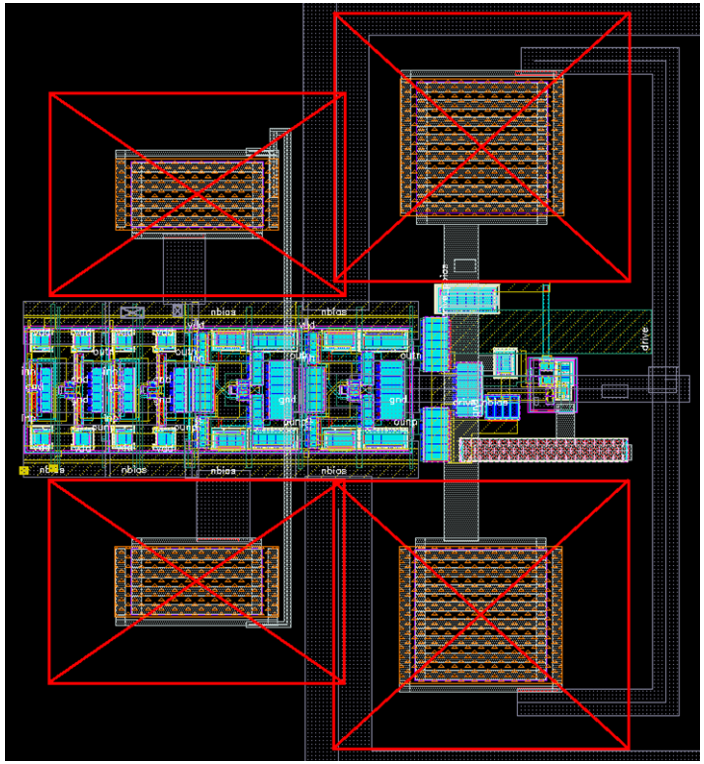
- VCSEL current is set by two transistors
  - One with constant bias
  - Second biased by a capacitive feed forward of the negative half of the differential input signal
    - Creates pre-emphasis and improves VCSEL current rise/fall time

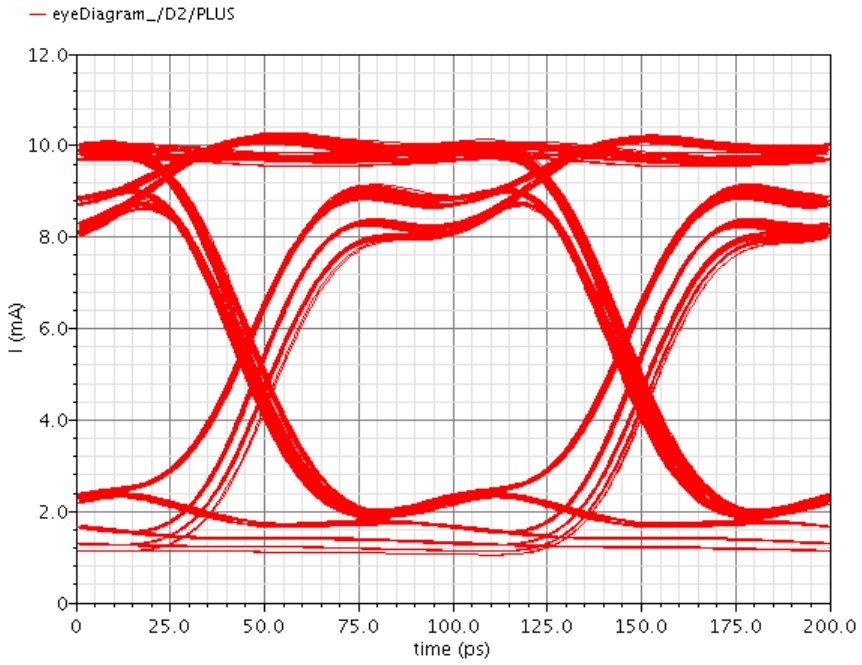


feed forward capacitance

VCSEL Driver (continued)

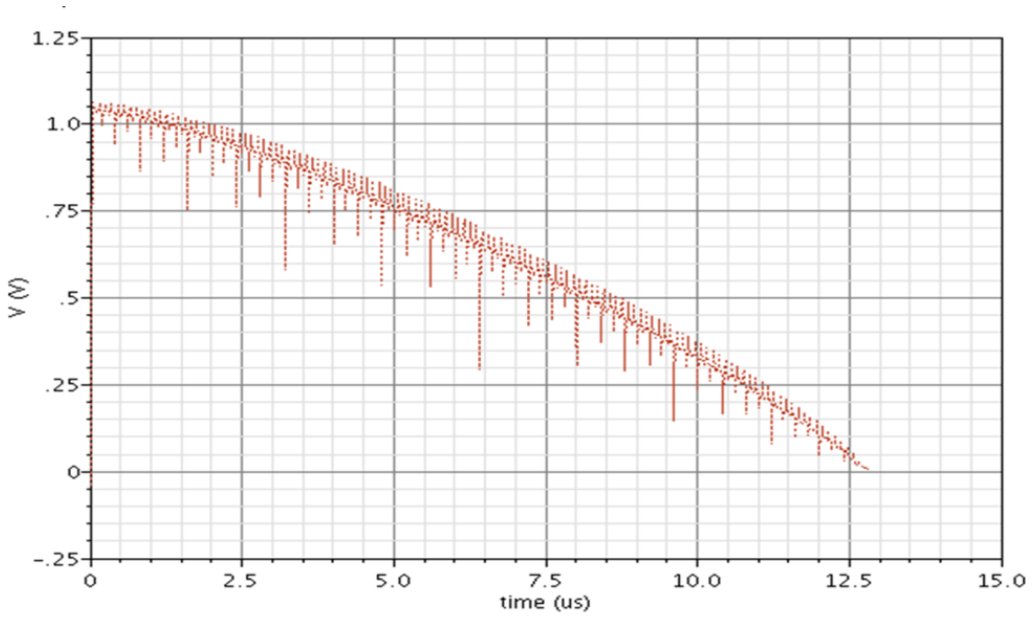
- Driver consumes 12.5 mA @ 1.2 V (15 mW)
- Layout is 125 μm x 125 μm
- Extracted layout eye diagram including pad, wire-bond, and VCSEL parasitics
  - working on improving the design

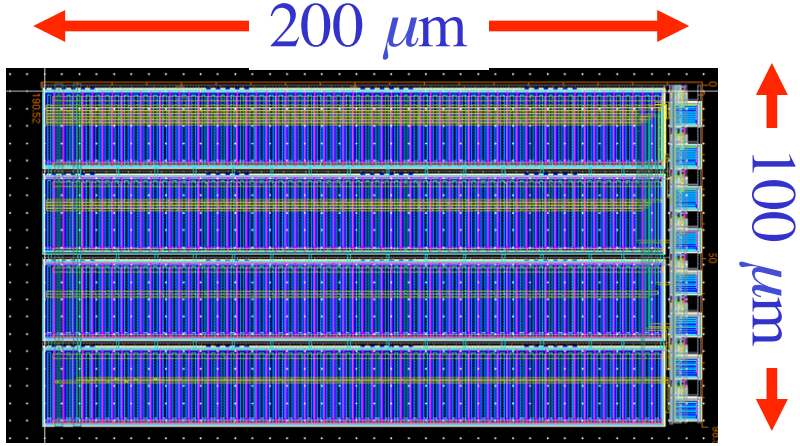




8 Bit DAC

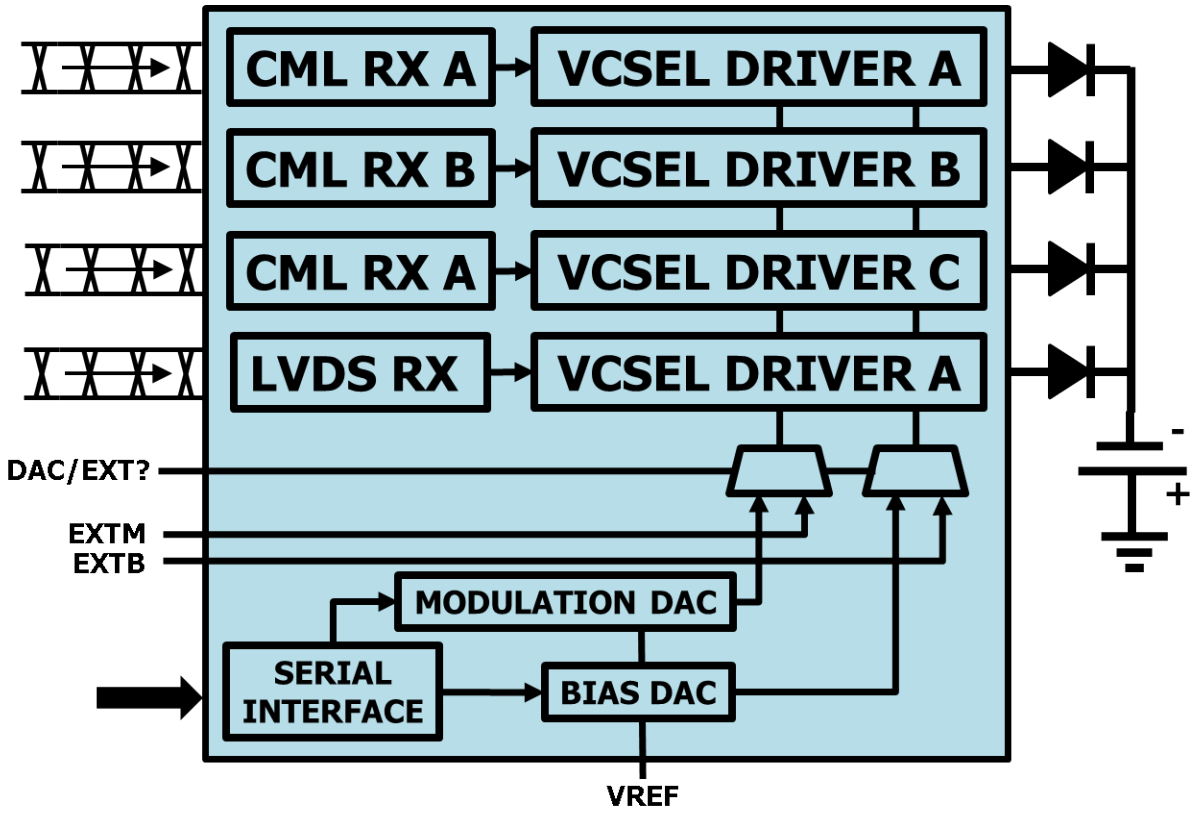
- Scaled from existing 130 nm design
- Plan to use external reference for the prototype
  - CERN bandgap reference IP should be available soon
- Consumes 270 μA @ 1.2 V
- Output sweep is not yet linear, working on improvement





4 Channel VCSEL Driver Prototype

- Currently designing a four-channel test chip
- Four separate channels have different VCSEL driver and differential receiver topologies
  - Useful to guide us in tuning and selecting a preferred topology for the design of the 12-channel ASIC



Summary

- Irradiated 12-channel VCSEL array driver
  - ASIC still works at 5 Gb/s but degraded rise time/jitter performance
- Design of 4-channel VCSEL array driver in progress
  - Completed design of CML receiver with satisfactory performance
  - have preliminary design of VCSEL driver