Summary of VCSEL Problems and Opto-Board Production Plan

W. Fernando, M. Fisher, K.K. Gan, K. Loureiro
The Ohio State University

Nov 30, 2006

Outline

- Chronology of VCSEL problems
- Summary of VCSEL problems/contradictions
- Opto-board production schedule

First Hint of Problem

- 2002:
  - an VCSEL array was observed to turn itself on & off repeatedly
  - related to the current problem?
- Feb 2005:
  - start of opto-board production
- Aug 2005:
  - board 3149 has low optical power during QA
  - investigation reveals no obvious problems
    - ⇨ remove wire bonds to supply current directly to VCSEL
    - ⇨ recovered 50% of power after passing 20 mA
  - mostly likely related to the current problem

Strange Siegen Observation

- Sept. 2005:
  - Siegen reported several D opto-boards:
    - low current consumption: ~190 mA
      - nominal current consumption: ~260 mA
    - no optical power
- Why OSU observed no problem during production?
  - OSU produced several times more opto-boards
  - OSU mounted VCSEL soon after receiving
  - Siegen mounted VCSEL months after receiving
  - ⇨ VCSEL problem takes several months to develop?
- Oct. 2005: opto-board production completed at OSU

An Unstable OSU Board

- March 2006:
  - OSU board 3088 was observed to have low power at CERN
    - ⇨ board was returned to OSU
    - ⇨ board was observed to produce good power
- What we know now:
  - some VCSEL arrays have developed large common resistance
  - some VCSEL arrays can recover on its own

Start of VCSEL Fiasco

- April-July 2006:
  - ~200 D boards passed reception test at CERN
  - optical power measurement:
    - send all "1" to channel of interest as Taiwan QA
    - send pseudo-random bit string to other channels to emulate experimental condition
- August 2006:
  - start testing of B boards
    - 2 of first 3 boards tested have low power
    - decided to measure power with all "1" in all channels
    - ⇨ 7 out of 36 boards have low or no power

Common Serial Resistance Theory

- September 2006:
  - some VCSEL arrays were observed to fail or heal instantly in LIV scan
  - ⇨ problem is electronics in nature rather than in the conductive epoxy between array and opto-board?
  - ⇨ problem was interpreted as the array developing a large common serial resistance
  - ⇨ reduce available voltage to drive the VCSEL
  - ⇨ VCSEL produces low or no power
  - Oxford irradiated 5 arrays to ~10^{16} $n_{1\ MeV}/cm^2$
    - power in 3 arrays drops to zero after some annealing but recovers after further annealing
    - related to the above problem?

Strange Mechanical Effect

- September 2006:
  - Siegen reported that board current consumption can be increased by pressing hard on VCSEL array
    - board #1:
      - current increases from 180 to 230 mA
      - VCSEL starts to produce light
    - board #2:
      - current increases from 230 to 250 mA
      - VCSEL continues to produce light
    - above observations are repeatable
  - ⇨ VCSEL problem is in the conductive epoxy?

Analysis of Conductive Epoxy

- October 2006:
  - Maurice measured thickness of conductive epoxy of both good and bad arrays:
    - silver content are about the same for both arrays
    - ⇨ no major difference
    - epoxy thickness is ~ 5 μm for both arrays
      - ★ vendor recommended thickness is ~25 μm
    - ⇨ measurement of epoxy resistance in progress
- OSU is interested to fabricate 20 opto-packs with 25 μm thick epoxy
  - ⇨ measure optical power after running at elevated temperature for extended time

Statistics on Bad Boards

- October 2006:
  - retest D boards by sending all "1" to all channels
  - ⇨ some boards were found to have low or no power
- D boards: 15 out of ~260 boards have high CSR
- B boards: 12 out of ~53 boards have high CSR
  - ⇨ why much higher fractions of high CSR arrays in B boards?

Observations/Contradictions

- why Siegen observed during production 7 bad VCSEL arrays while OSU observed only one in much larger sample?
  - Siegen mounted arrays several months after receiving
  - ⇨ high CSR takes several months to develop?
  - ⇨ will more arrays develop high CSR in the future?
    - 11 PQSR and 72 ISP arrays have no problem so far…
- why much higher fractions of high CSR arrays in B boards which were produced later in time?
- why only one D board has high CSR at CERN reception test?
  - ⇨ running all channels with all "1" creates stress?

Observations/Contradictions

- array can fail or heal instantly in LIV scan
  - ⇨ problem is inside array rather than in conductive epoxy?
  - ✔ no observable difference in epoxy thickness/silver content
  - ✘ epoxy thickness ~ 5 μm (~25 μm recommended)
  - ✘ VCSEL current can be increased by pressing
    - ✘ possible to compress 5 μm gap?

Opto-board Statistics

Board	D	B
Need	228	44
1st	195	26
1st (new)	10	1
2nd	13	12
mounted	12	18
blank	15	11
recoverable	~20	

- expect enough good boards for all but one service panel in 2006