Status of the Development of On-Detector Array-based Optical Link

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Outline

- Introduction
- Current work with IBL
- Schedule

Introduction

- A proposal to develop on-detector array-based opto-links was presented at the last ATLAS Upgrade Week (Nov. 2009):
  http://indico.cern.ch/getFile.py/access?contribId=4&resId=0&materialId=slides&confId=72471
  - ATLAS Upgrade Technical Coordinator (Nigel Hessey) wants the development schedule be presented at the Joint Opto WG meeting for comments and suggestions

IBL

- ATLAS proposed to add one more layer to the current pixel detector:
  - "Inner B-Layer" or IBL
  - to be installed ~ 2014
  - optical links will use VCSEL/PIN array as in current pixel detector
  - an updated version of current driver (VDC) and receiver (DORIC) with redundancy and individual VCSEL current control would be a logical improvement
    - experience gained from the development/testing of such new chips would help the development of on-detector array-based opto-links for SLHC
      - ⇨ submission of 1st IBL prototype chip (130 nm) in 2/2010

16 Channel Mux. (SLHC)

Spare VDC

VDC (3)

VDC (2)

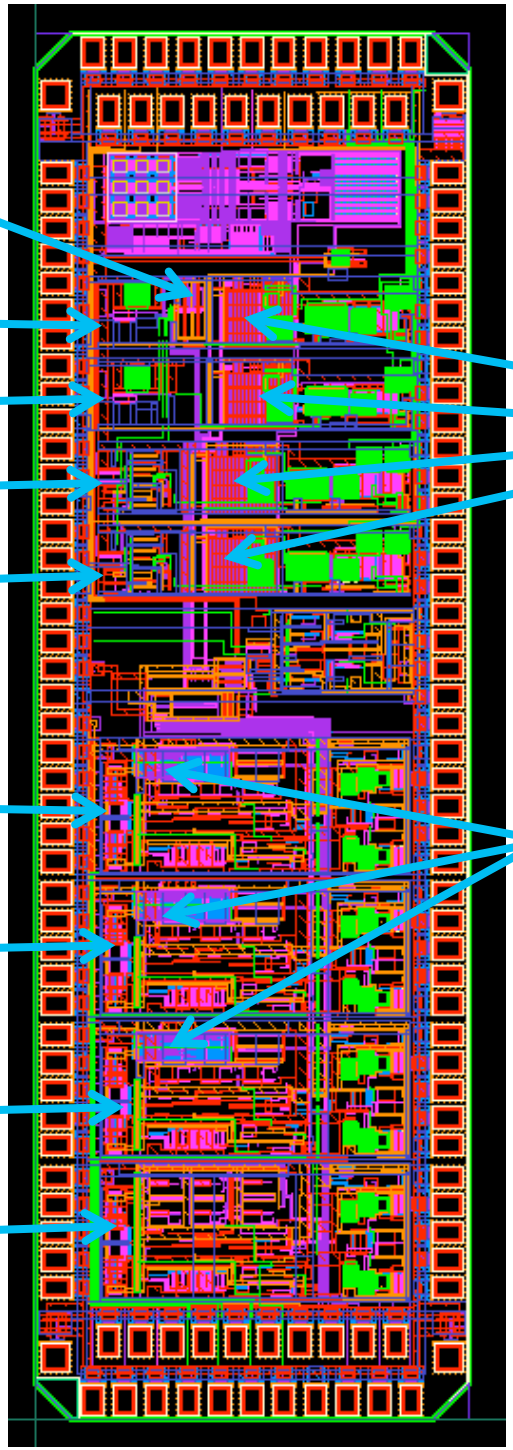
VDC (1)

DORIC (1)

DORIC (2)

DORIC (3)

Spare DORIC

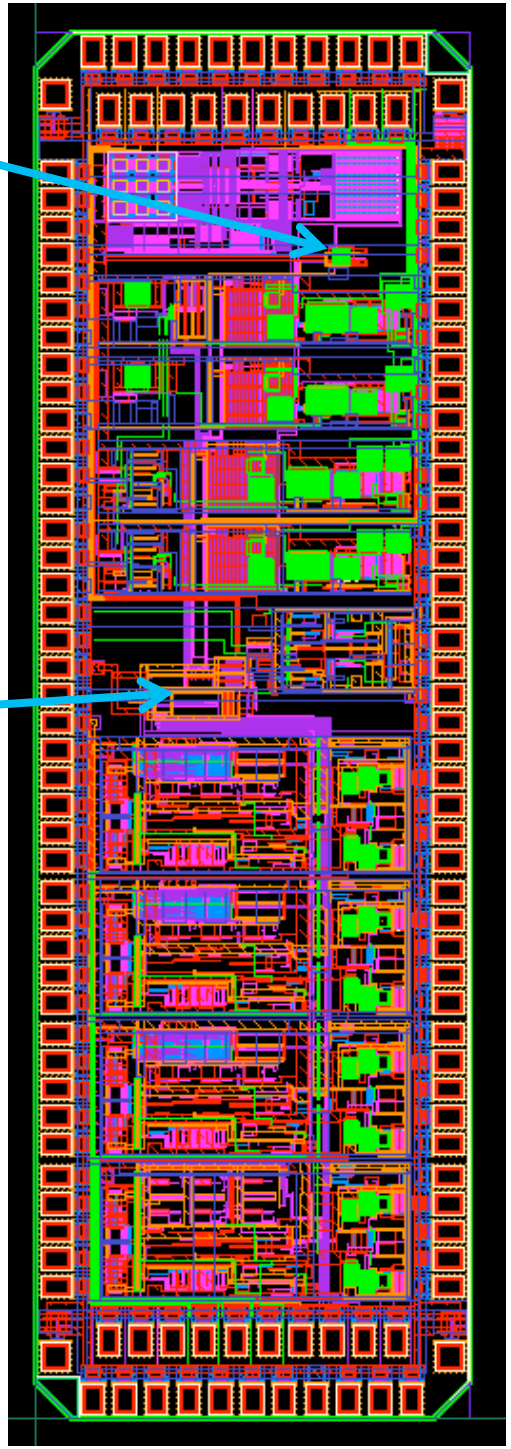


DAC (SLHC)

FE-I4 Command decoder

- control channel routing in VDC/DORIC
- used to set VDC DACs
- control of opto-chip based on majority vote of the three command decoders

Power on reset circuit



Opto-Chip Control Logic

- Interfaces opto-chip controls to the 3 FE-I4 command decoders
- Contains SEU tolerant DICE latches from FE-I4
- Power on reset circuit to set default VCSEL current to 10 mA

Schedule

- The proposed schedule called for SLHC array chip submission in 11/2010 (4 channels) and 12/2011 (12 channels), followed by irradiation of chips from each submission.
- There is no urgency to submit in 11/2010
  - chip should be submitted when a design has been thoroughly simulated
  - all are invited to join the effort!