



Array-Based Opto-Link R&D Activity and Plan

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Motivation



- ATLAS Pixel detector:
 - ◆ signal from FE transmitted on ~ 1 m skinny wires to patch panels
 - signal transmitted off patch panels using VCSEL arrays
 - similarly using PIN arrays for transmission in other direction
 - a compact solution
- ATLAS Insertable B Layer ($\sim 2015-16$):
 - ◆ will be an array-based system
 - ◆ economical redundancy system
- ATLAS SLHC Pixel detector:
 - ◆ signal from FE will be transmitted on ~ 5 m skinny wires
 - ◆ develop array-based solution to take advantage of experience



Current Activity

- ATLAS Insertable B Layer:
 - ◆ optical links will use VCSEL/PIN array as in current pixel detector
 - ◆ design an updated version of current driver and receiver with redundancy and individual VCSEL current control
 - experience gained from the development/testing of such new chips would help the development of on-detector array-based opto-links for SLHC
 - ⇒ submission of 1st prototype chip (130 nm) in 2/2010
 - a collaborative research between Siegen and Ohio State



Summary of IBL Prototype Chips

- prototyped 4-channel driver/receiver:
 - ✓ redundancy to bypass broken PIN or VCSEL channel
 - ✓ individual VCSEL current control
 - ✓ power-on reset to set VCSEL current to several mA on power up
 - ✓ VCSEL driver can operate up to ~ 5 Gb/s with $\text{BER} < 5 \times 10^{-13}$
 - ✓ PIN receiver/decoder properly decodes signal with low threshold
 - ◆ next submission of 12-channel chip: 2/2011



SLHC Array ASIC R&D Plan

- VCSEL driver/PIN receiver developed by GBT/VL need to be laid out as an array
 - ◆ will work closely with GBT/VL groups
 - ◆ special thanks to P. Moreira for thoughtful advice
 - ◆ first submission: 2011/2012?
 - 4-channel prototype only
- Continue evaluation of radiation-hardness of new high-speed PIN/VCSEL arrays