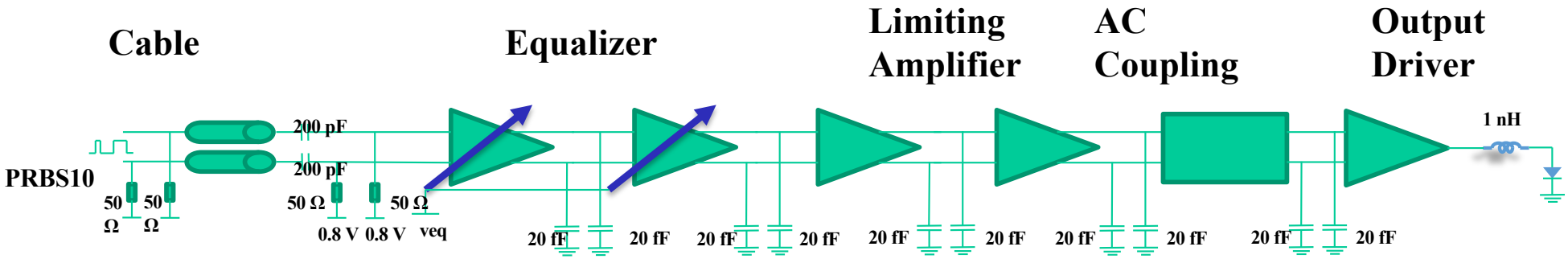
Status of Equalizer Design

K.K. Gan
The Ohio State University

Introduction

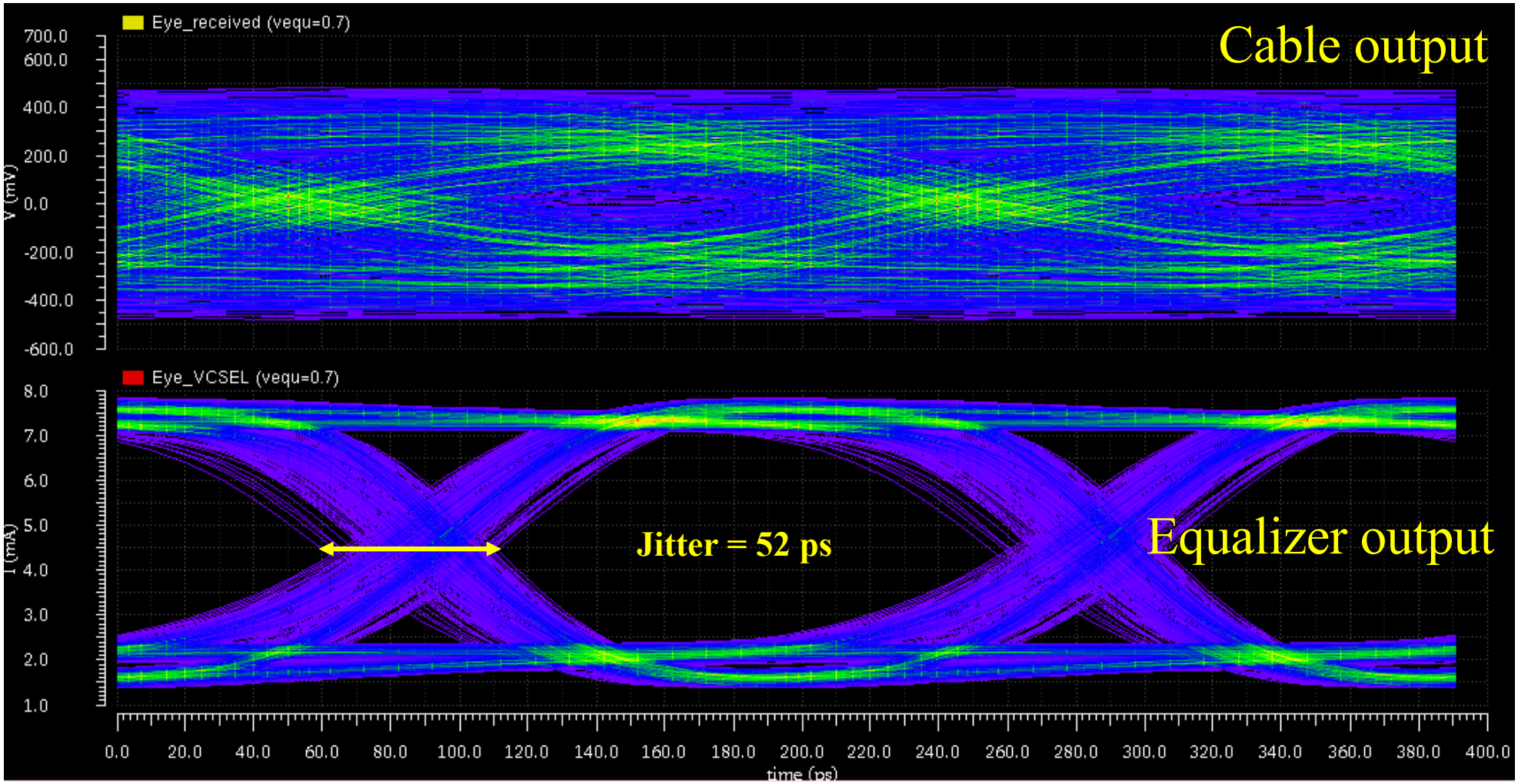
- data is transmitted at 5.12 Gb/s via 5.5 m of skinny cable (twin-ax) from data aggregator to optical module
  - jitter < 70 ps for bit error rate (BER) < 10^{-12}
- equalizer is needed to compensate for loss of high frequency components of the signal
- organizing an effort to design the equalizer with bi-weekly meetings
- institutions: Ohio, Siegen, SMU

SMU Design

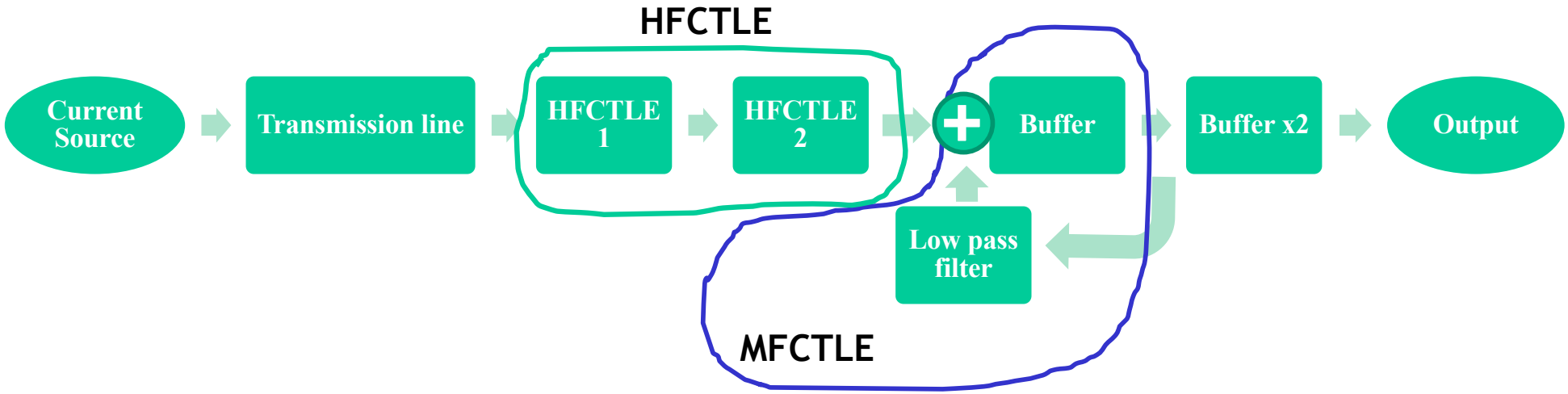

Cable
Equalizer
Limiting Amplifier
AC Coupling
Output Driver
PRBS10
50 Ω
50 Ω
200 pF
200 pF
50 Ω
50 Ω
0.8 V
0.8 V
veq
20 fF
20 fF
20 fF
20 fF
20 fF
20 fF
20 fF
20 fF
20 fF
20 fF
1 nH

SMU Results

- eye diagram from schematic level simulation

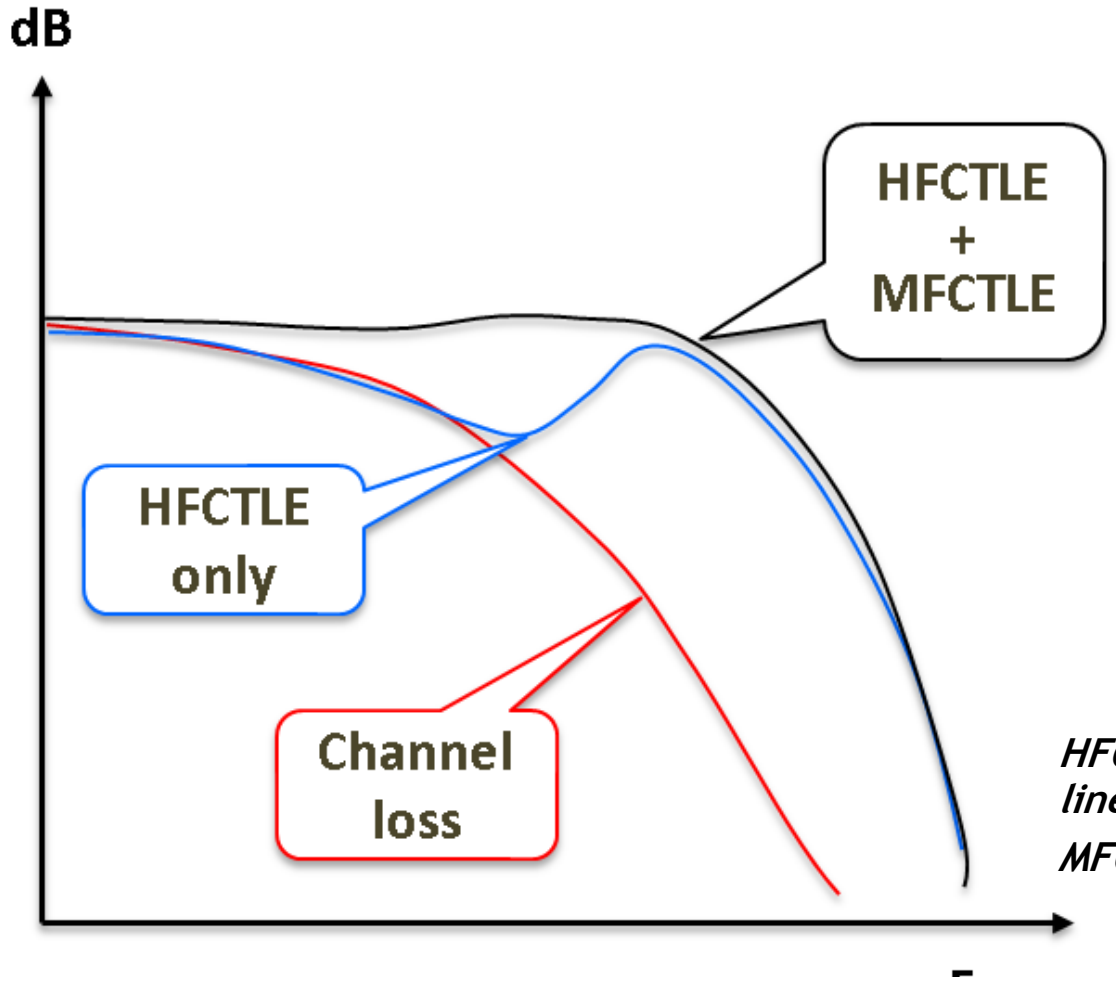


Ohio/Siegen Design



Ohio/Siegen Equalizing Scheme

- conventional HFCTLE has a dip in frequency response at the mid-frequency
  - higher jitter
- MFCTLE compensate for mid-frequency attenuation

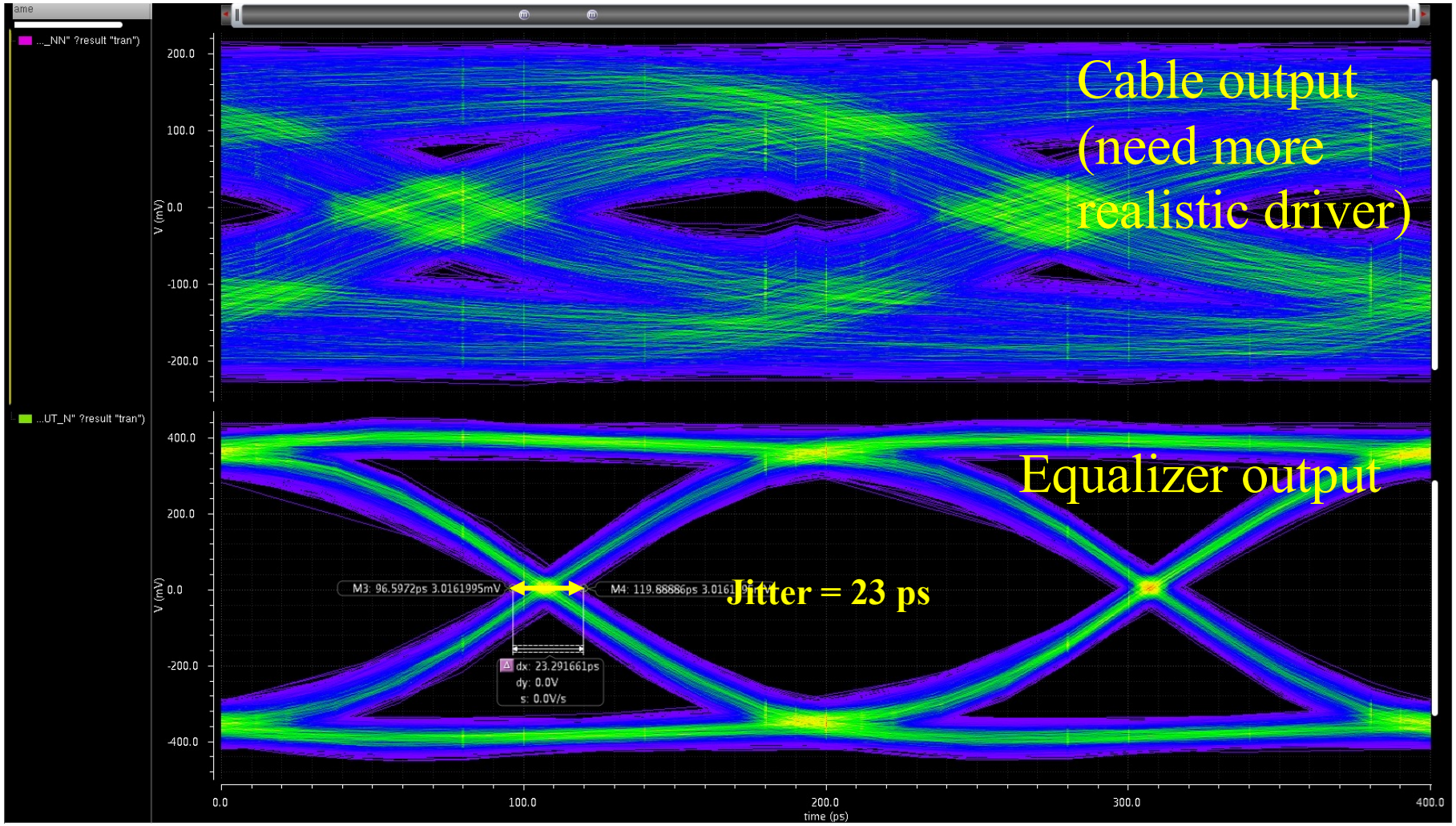


HFCTLE: High frequency continuous time linear equalizer

MFCTLE: Middle frequency CTLE

Ohio/Siegen Result

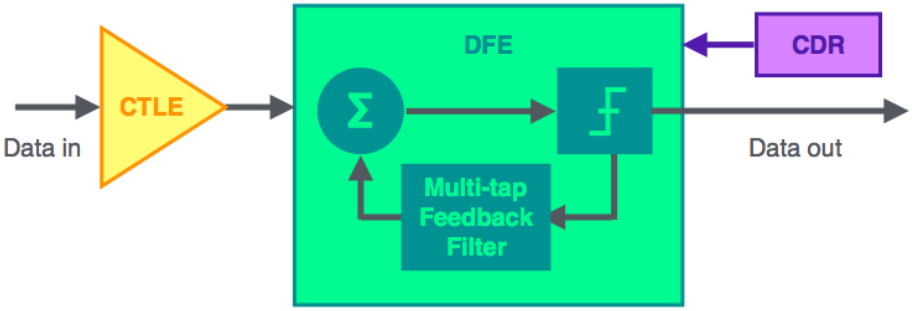
- eye diagram from schematic level simulation



LBNL Design

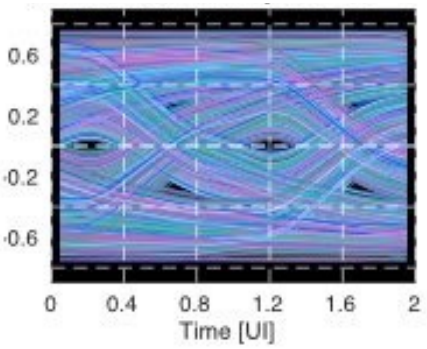
- Equalization chain with CTLE + DFE (Decision Feedback Equalizer) being developed at LBNL

- Goal: implement full commercial-like equalization chain by reusing design blocks from Berkeley Wireless Research Center (bwrc.eecs.berkeley.edu)

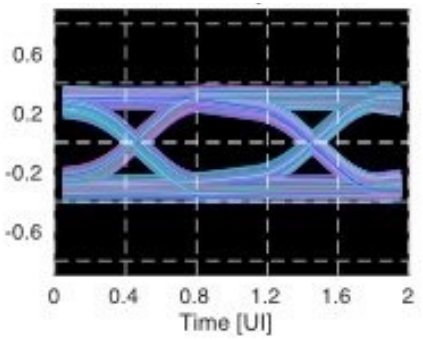


- CTLE only gets one half of the way there. Would like to get the type of performance possible with FPGA MGT ports

Simulation before DFE



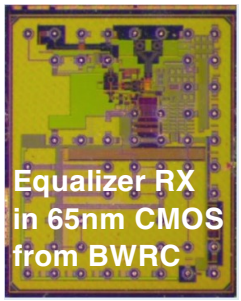
Simulation after DFE



- BWRC Matlab-based analysis framework for high-speed links used to determine needed number of DFE taps from prototype cable S-parameters

- 65nm circuit design using Berkeley Analog Generator (BAG) tool: Python-based circuit design platform to make design process faster

- Aim to have a chip design this summer



Equalizer Development Plan

- Need to compare the two designs under same condition
  - select the best equalizer for layout/extraction/simulation
- Need to develop the clock and data recovery (CDR) circuit to retime the data signal to reduce jitter
- submit the ASIC (65 nm TSMC) for fabrication in August?