Radiation-Hard Miniature Optical Engine with High Bandwidth

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December 18, 2019

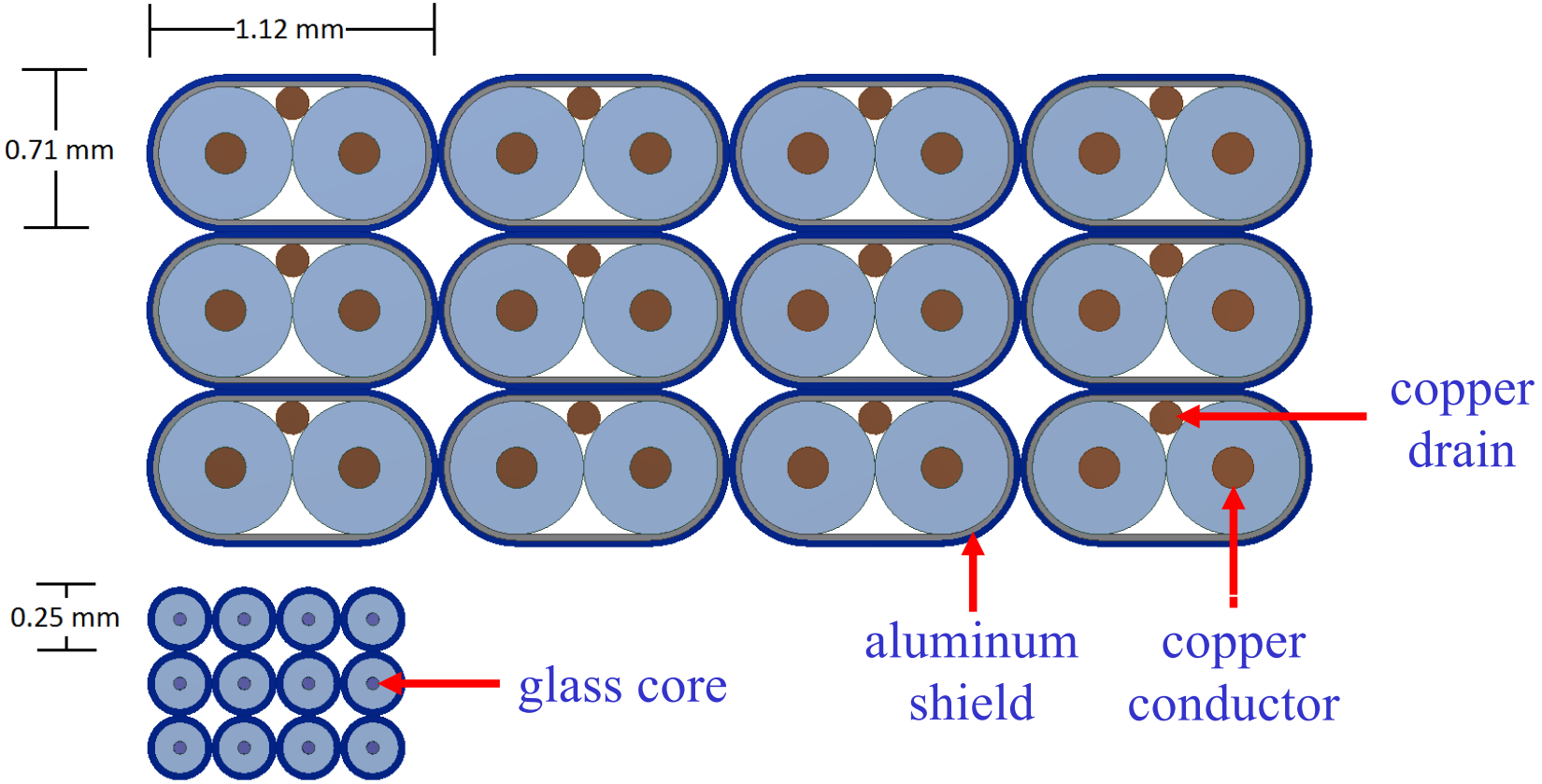
Outline

- Introduction
- Results @ 1.28 Gb/s
- Results @ 5.12 Gb/s
- Summary

Pixel Detector Data Transmission

- Run I: 3-layer ATLAS pixel detector:
  - speed: 80 Mb/s
  - data transmitted via ~1 m of skinny twisted pairs to opto-modules
- Run 2/3: 4-layer ATLAS pixel detector:
  - speed: 80 or 160 Mb/s
  - data transmitted via ~5 m of skinny twisted pairs to opto-modules
- Run 4 (HL-LHC): 5-layer ATLAS pixel detector:
  - speed: 1.28 Gb/s
  - data transmitted via ~5 m coaxial pairs (TwinAx) to opto-modules

Coaxial Cables vs. Fiber Ribbon

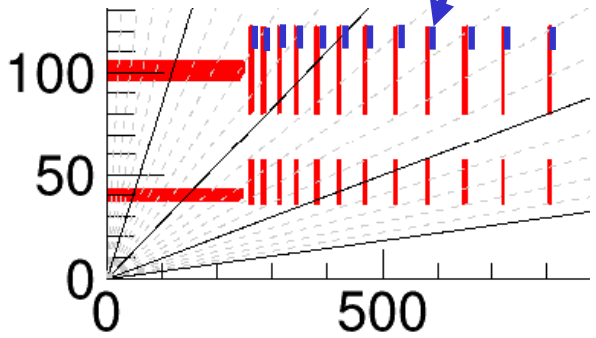


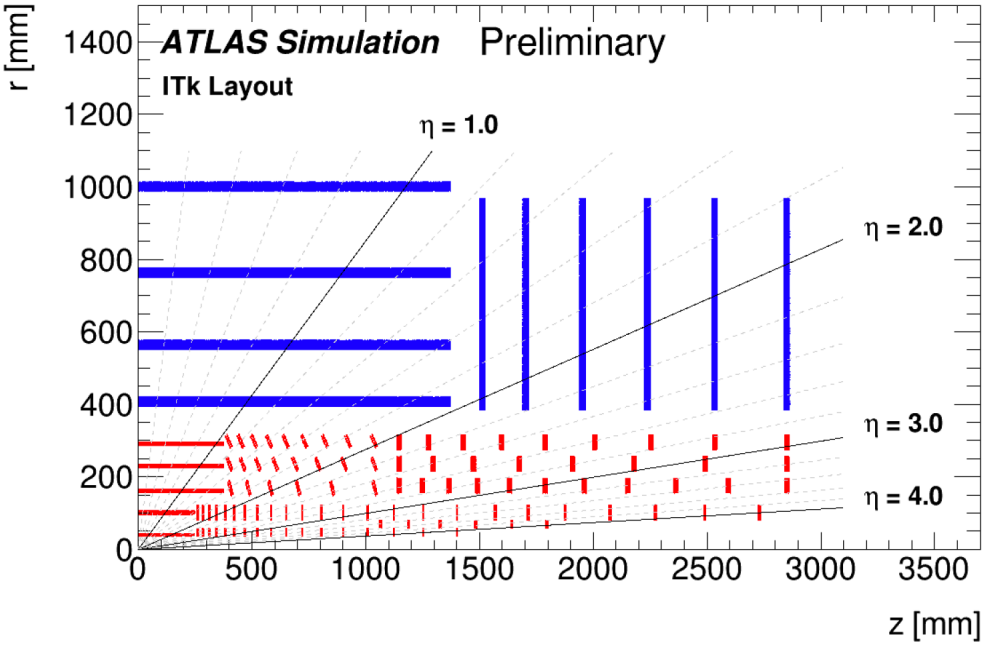
- ~2 m of TwinAx inside sensitive region of detector
  - produced more interactions in pixel and outer detectors
  - require more data bandwidth for transmission
- fiber ribbon has significantly less material

Layout

No need to build hundreds of opto-boxes (crates) to house opto-boards

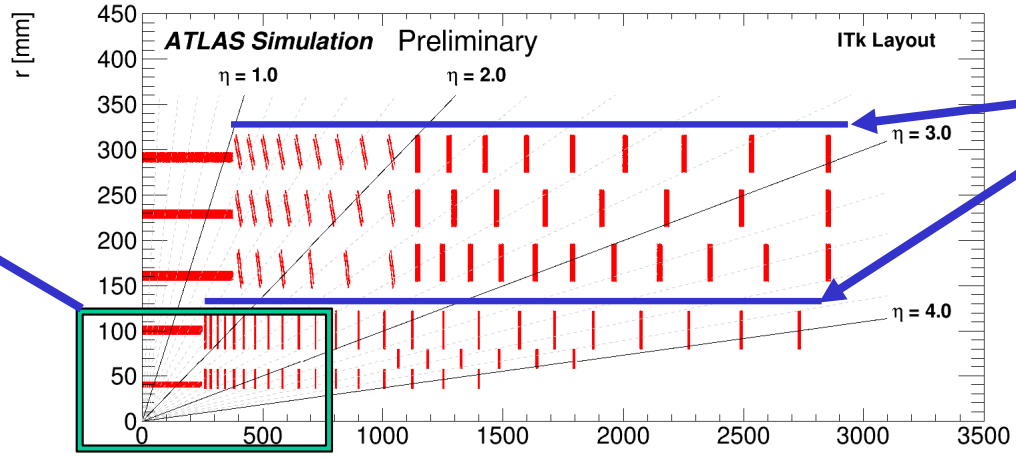
mini opto-board





strip

pixel

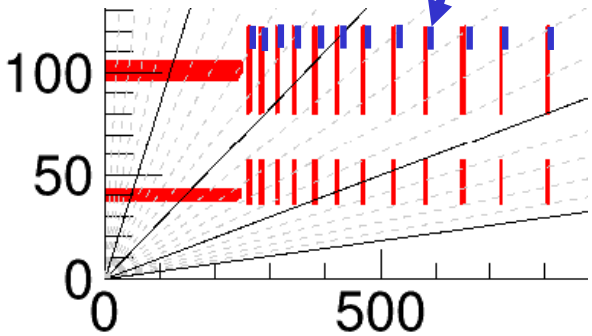


cable routing

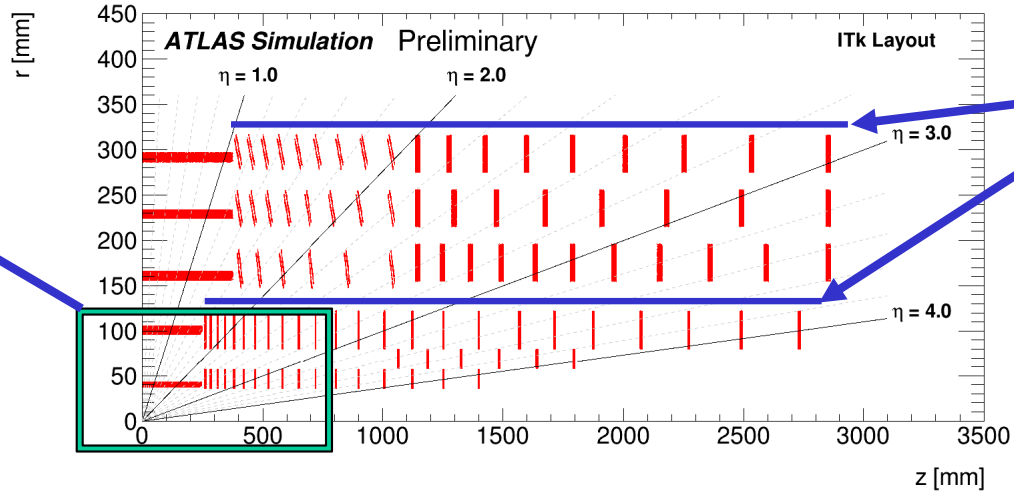
Layout

No need to build hundreds of opto-boxes (crates) to house opto-boards

mini opto-board

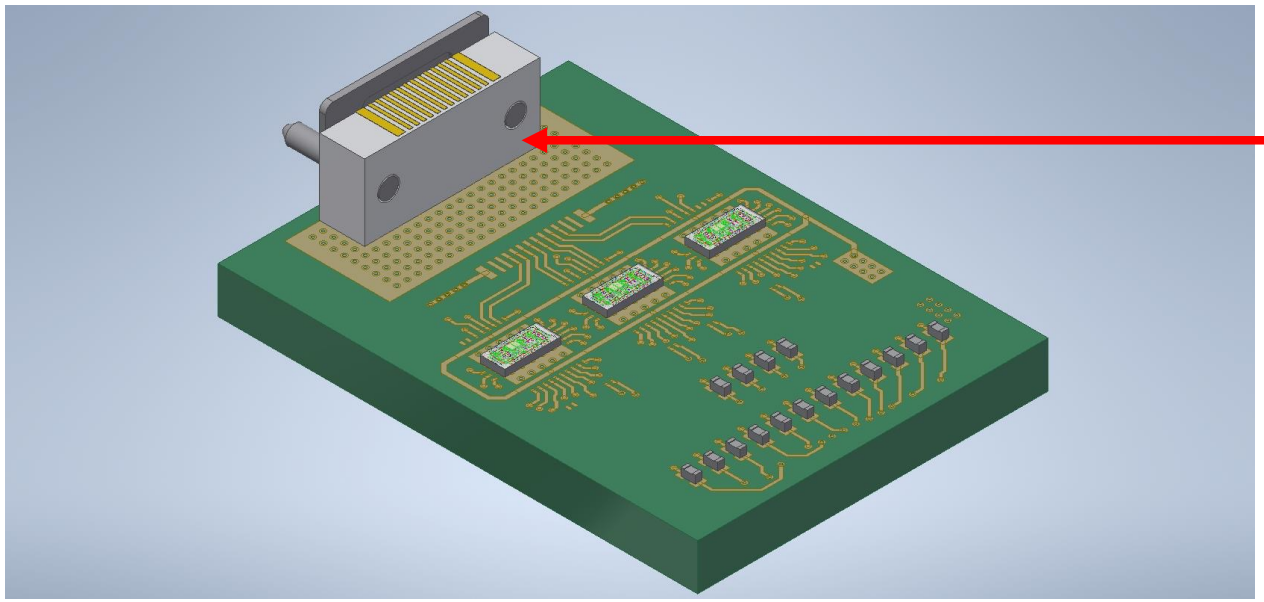


cable routing

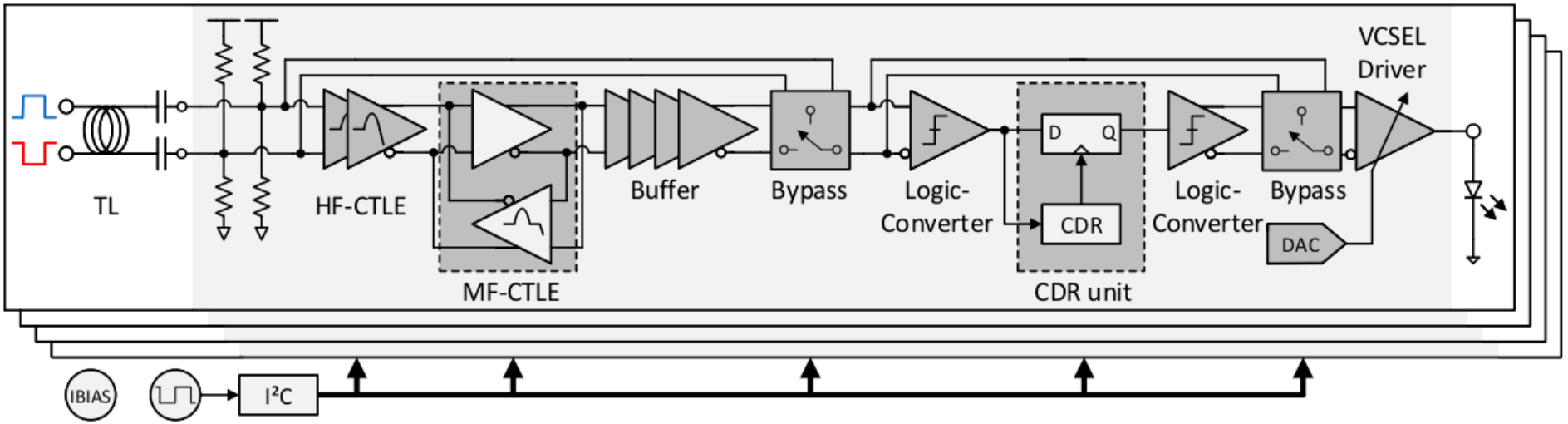


Mini Opto-Board

- prototyping mini opto-board with 12-channel VCSEL driver
  - model after Run 1-3 opto-boards
  - use same simple optical package
  - detachable fiber ribbon
  - 1 x 1 cm

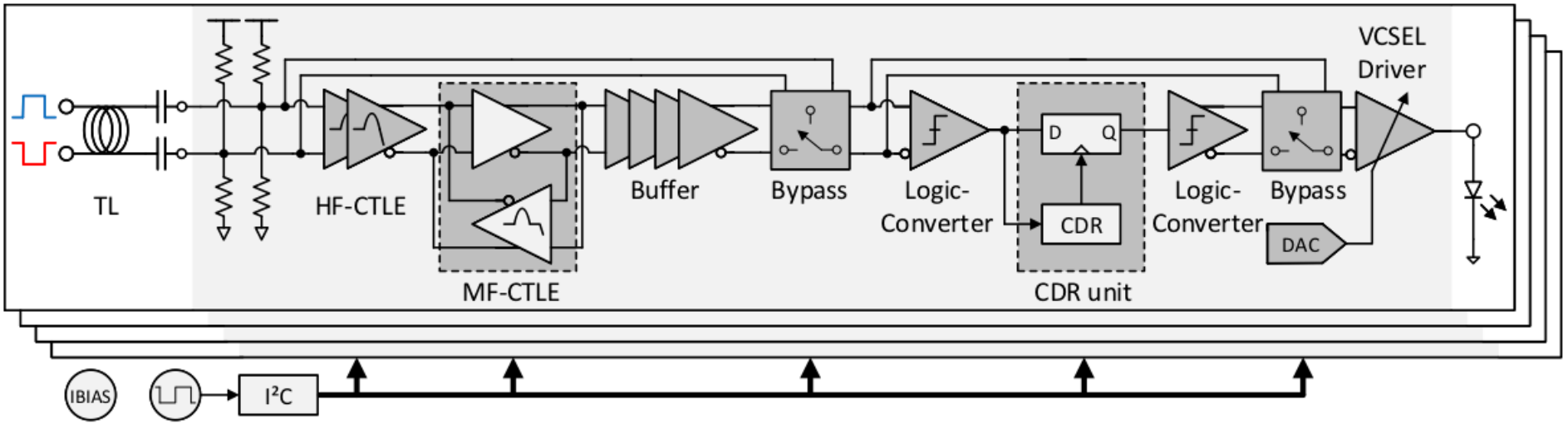


VCSEL Driver Chip



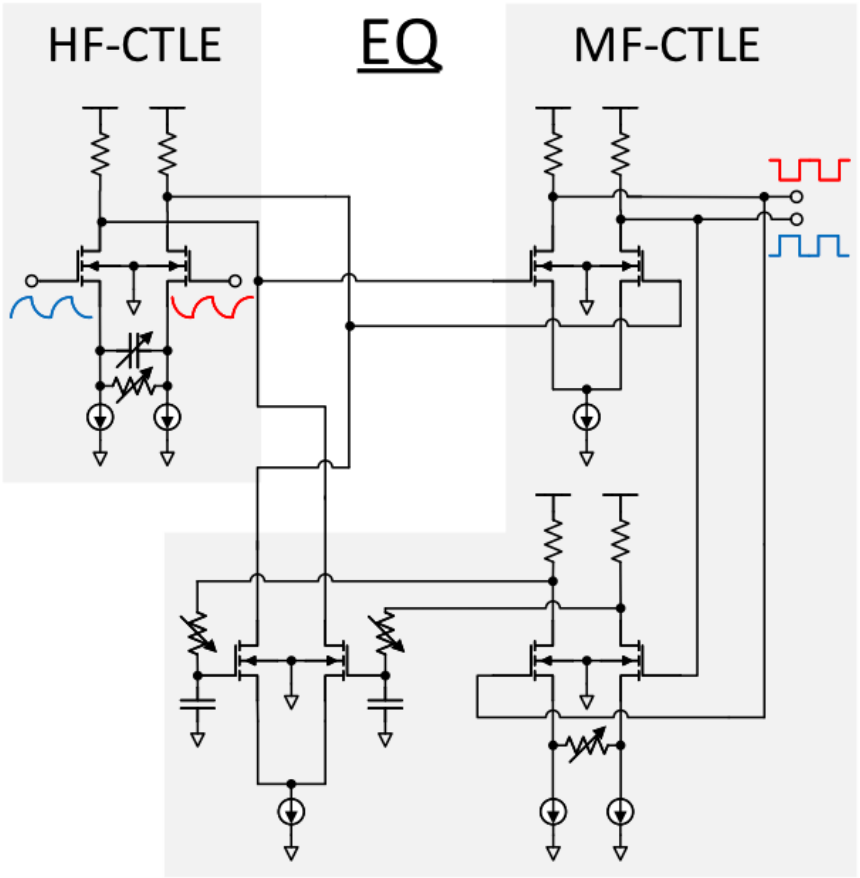
- fabricated in 65 nm technology
- external AC-coupling with large high broadband capacitors to prevent low frequency jitter
- cable loss compensation with 2x HF- and MF-equalizers for smoothing and increasing the signal bandwidth
- 4 stage buffers as current amplifier to decrease amplitude jitter and decoupling

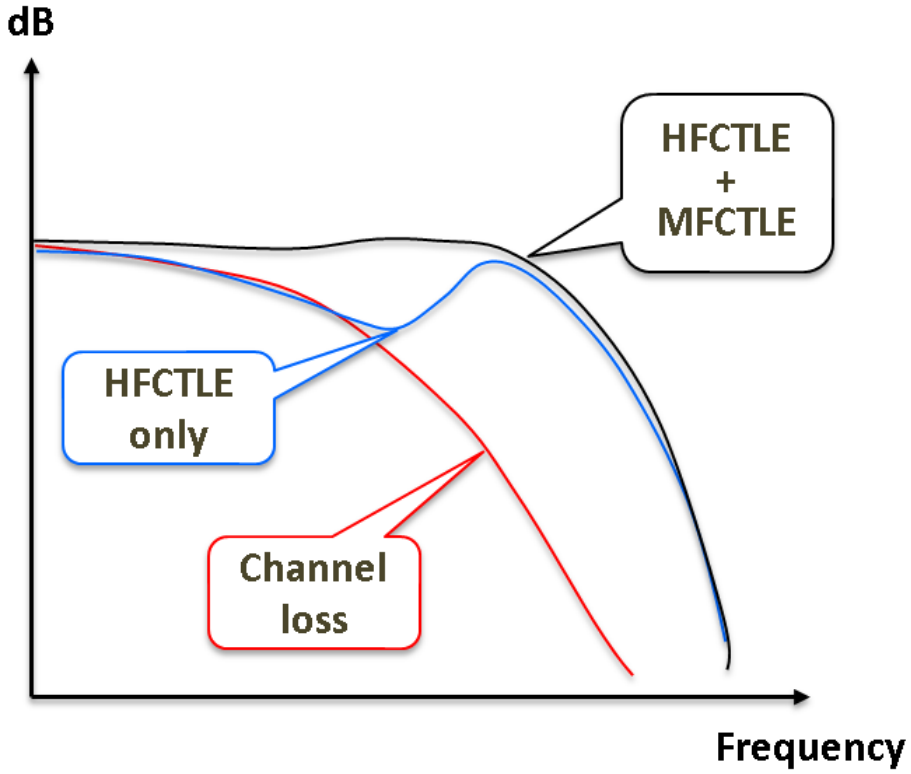
VCSEL Driver Chip (continue)



- bypass circuit to check EQ and CDR separately
- logic converter to switch between CML and CMOS levels
- CDR to reduce timing jitter
- DAC controlled current of VCSEL Driver
- triple redundancy I²C bus and circuit for controlling and adjusting frequency parameter of EQ and CDR

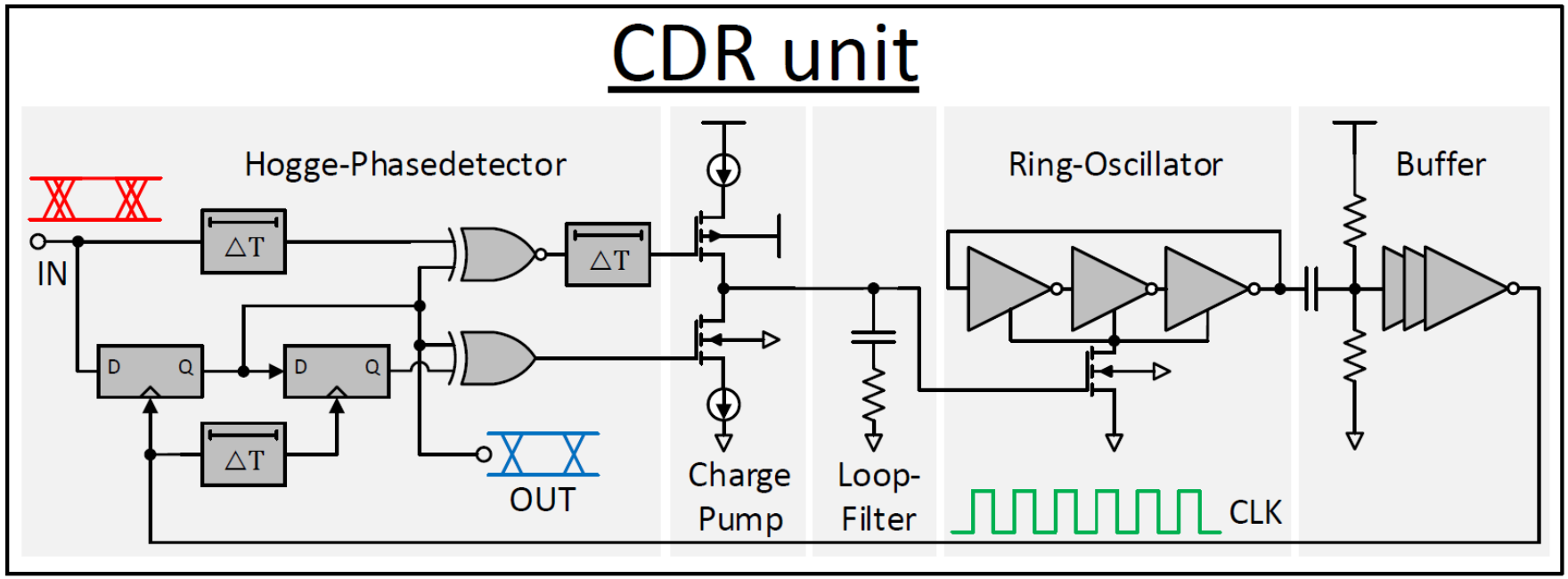
Signal Equalization





- HF-CTLE: High frequency continues time linear equalizer
- MF-CTLE: Middle frequency continues time linear equalizer

Clock Data Recovery



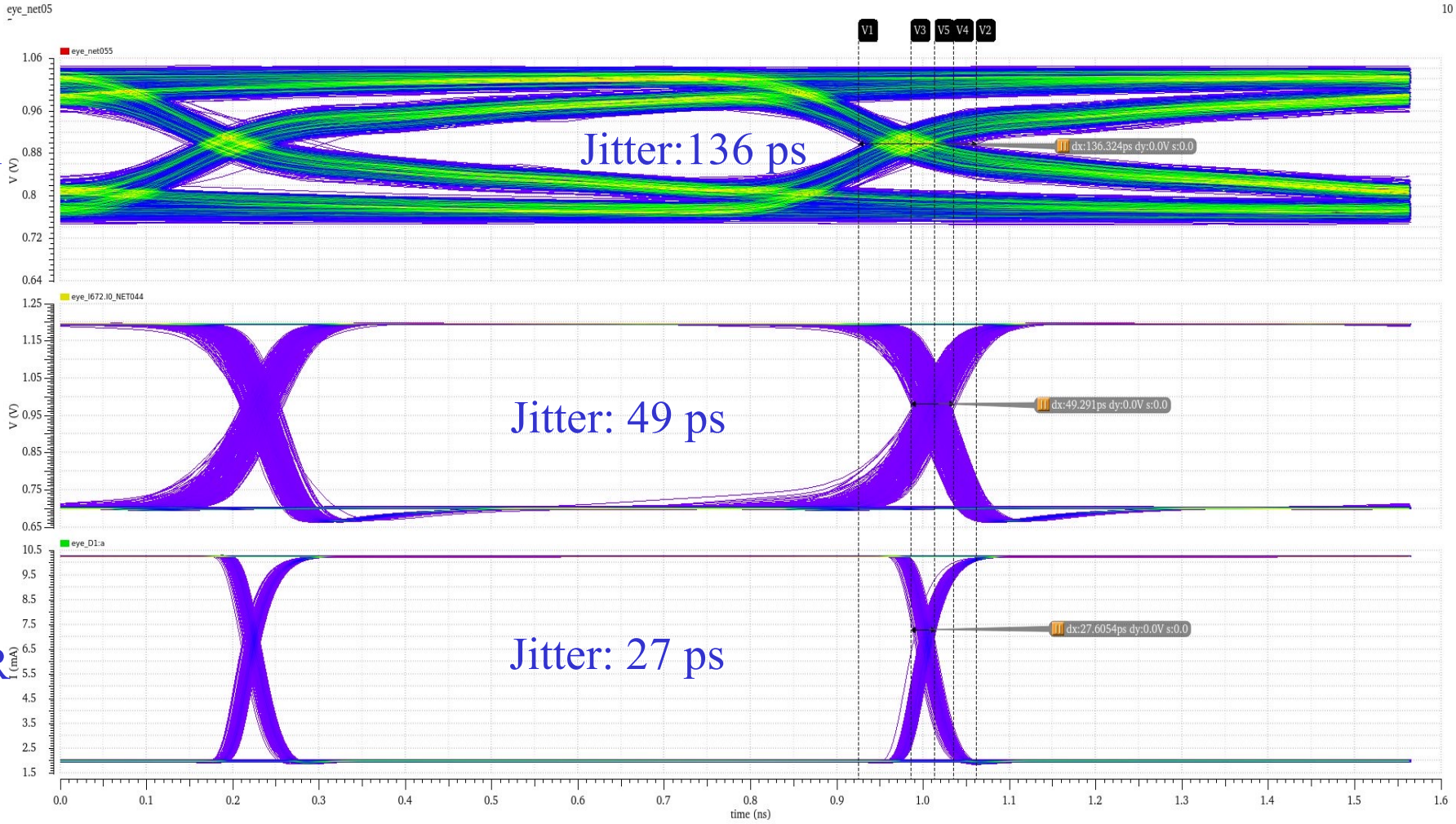
- CDR circuit designed for 1.28 and 5.12 Gb/s
- phase detector implemented with delay elements to compensate propagation delays of D-Flip Flops
- external loop filter capacitor (not shown, in parallel to the existing one) for decreasing clock jitter

Eye Diagram @ 1.28 Gb/s

After 5 m

After EQ

After CDR



Post layout simulation

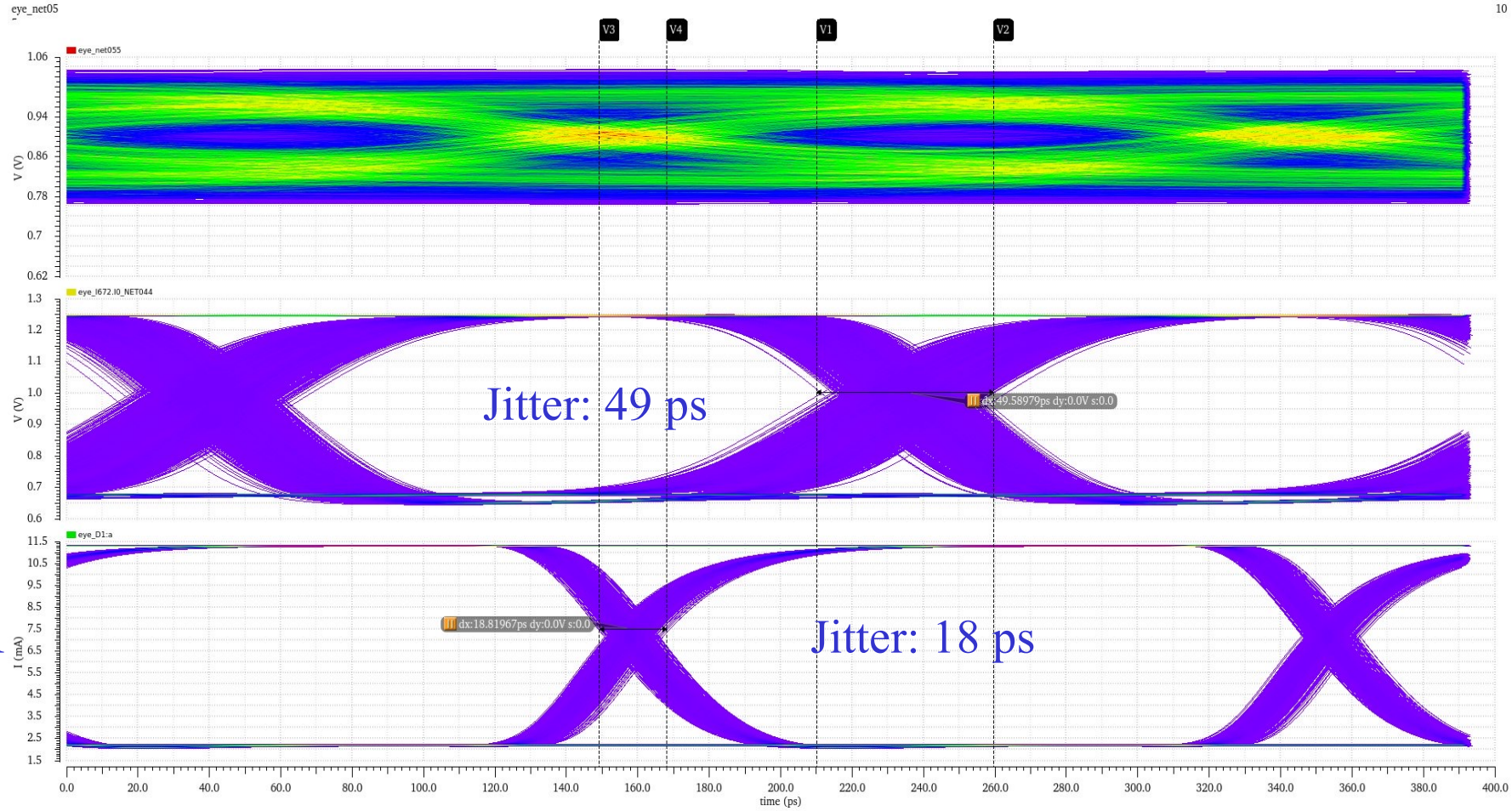
Bitpattern lenght 5,120 bits/ PRBS-15

Eye Diagram @ 5.12 Gb/s

After 5 m

After EQ

After CDR



Post layout simulation

Bitpattern length 10,240 bits/ PRBS-15

Summary

- mini opto-module being prototyped
  - 12 channels
  - transmit data at 1.28 and 5.12 Gb//s
  - ⇨ offer the possibility to greatly reduce detector material in sensitive region of detector

Received ASIC late last week.
Result too preliminary to show.