A Possible Redundancy System for Opto-Links

A. Adair, W. Fernando, K.K. Gan, H.P. Kagan, R.D. Kass,
H. Merritt, J. Moore, A. Nagarkar, S. Smith, M. Strang
The Ohio State University

P. Buchholz, A. Wiese, M. Ziolkowski
Universität Siegen

October 28, 2010

Outline

- Implications of New Quarter Service Panel Project
- Result on Driver/Receiver Chips with redundancy
- Implication of Redundancy on other Sub-systems
- Summary

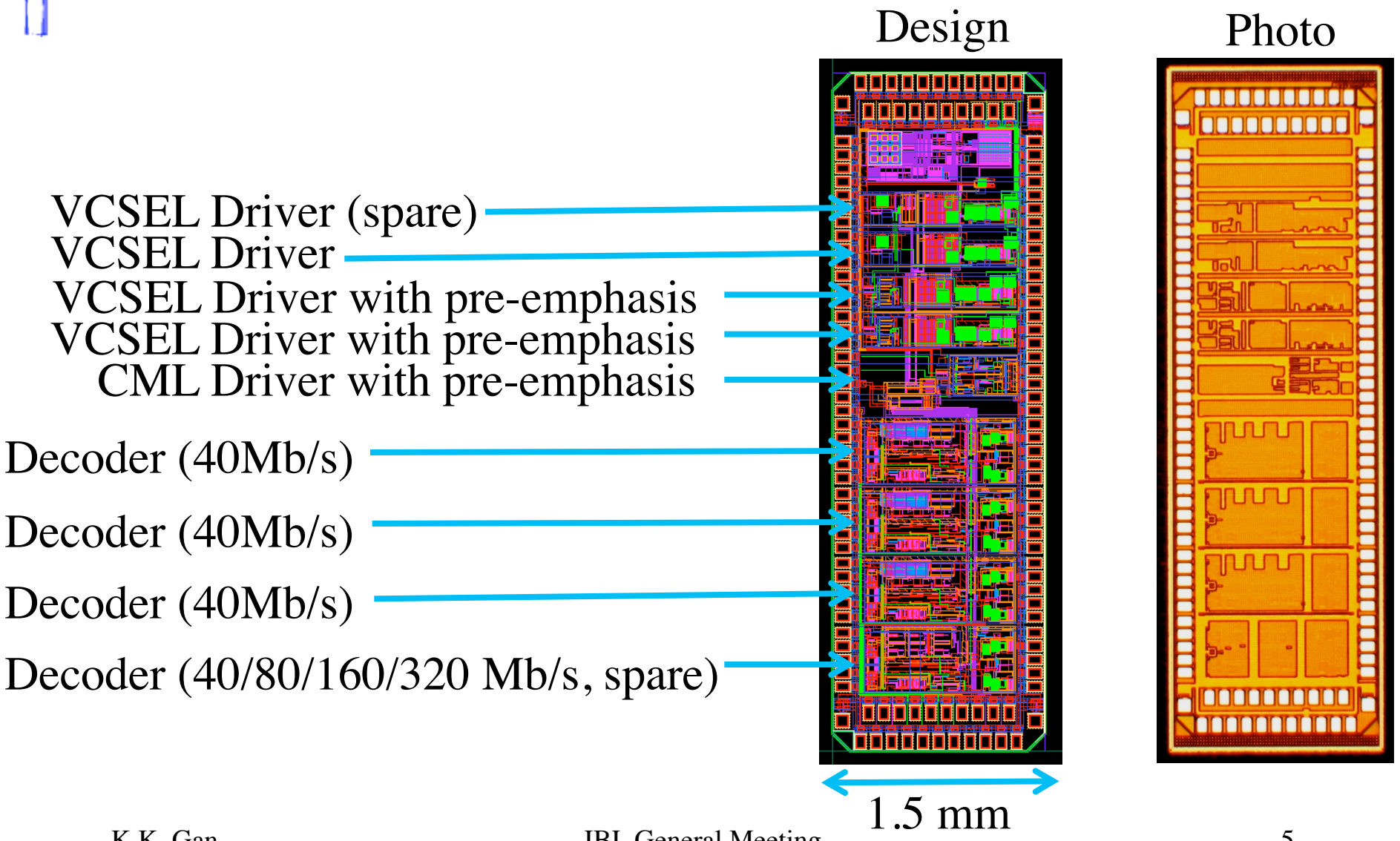
Implications of New QSP Project

- New QSP Project pushes the opto-boards schedule forward:
  - VCSEL/PIN opto-pack FDR ~ Feb 2011?
  - opto-board FDR ~ March 2011?
  - VCSEL/PIN opto-pack PRR ~ August 2011?
  - opto-board PRR ~ August 2011?
  - new opto-board will be designed to be compatible with IBL
    - a further improved opto-boards with redundancy etc. might still be used for B-layer and IBL

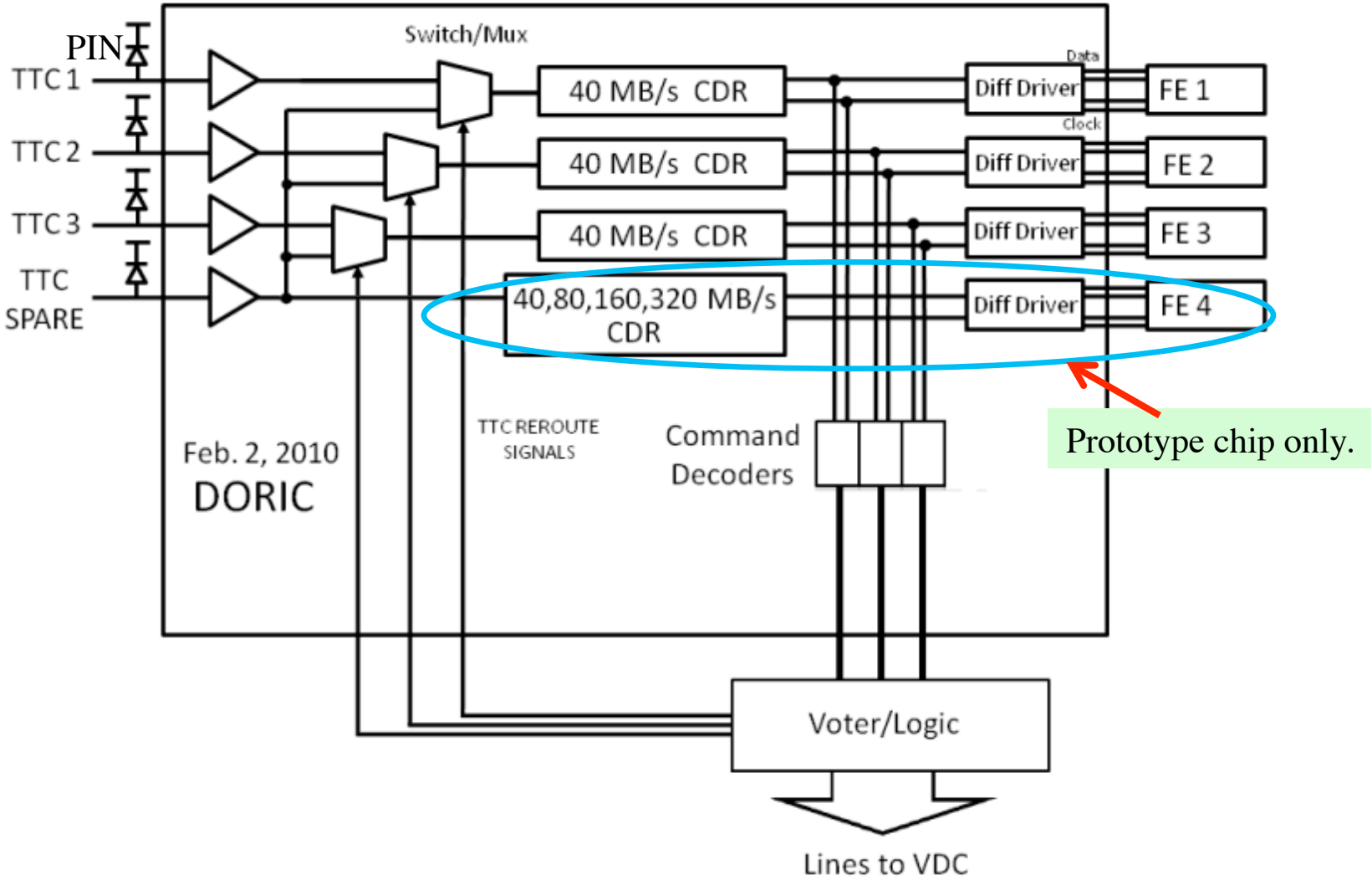
Motivations for Redundancy

- Not yet learned how to build a highly reliable opto-links
  - ~1.5% of non operable pixel modules are links related
    - don't know the fraction of problematic links that are opto related
    - don't know how the problems will evolve with time
  - TXs for Pixel/SCT have been all replaced once
  - 194 out of 272 TXs of Pixel from second batch have been replaced
  - unlikely to get yearly access for opto-link repairs
  - some redundancy circuits developed will be useful for SLHC
  - ⇨ redundancy allows operation of IBL with 100% efficiency

Chip Content



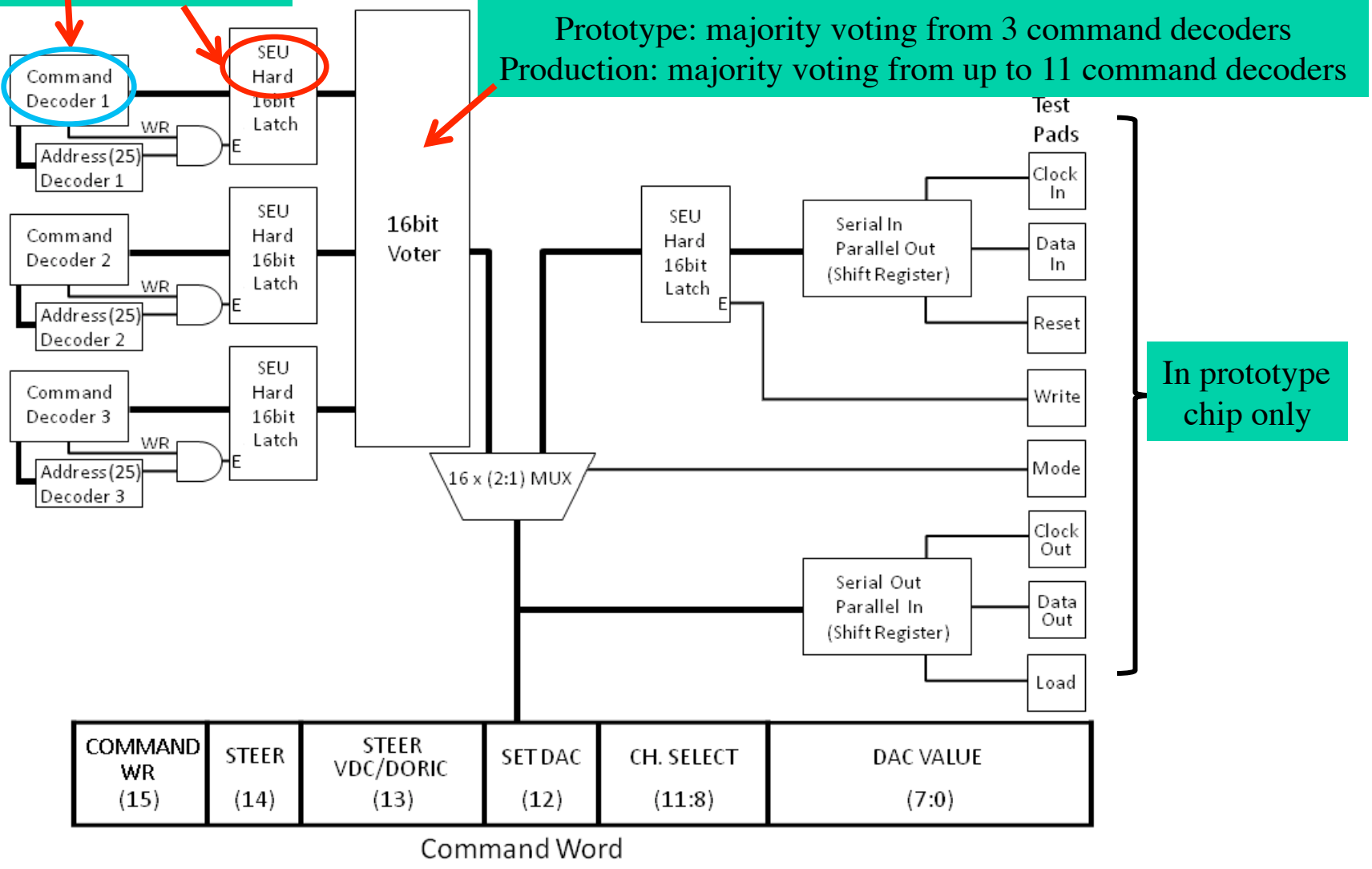
PIN Receiver/Decoder



Command Decoder Interface

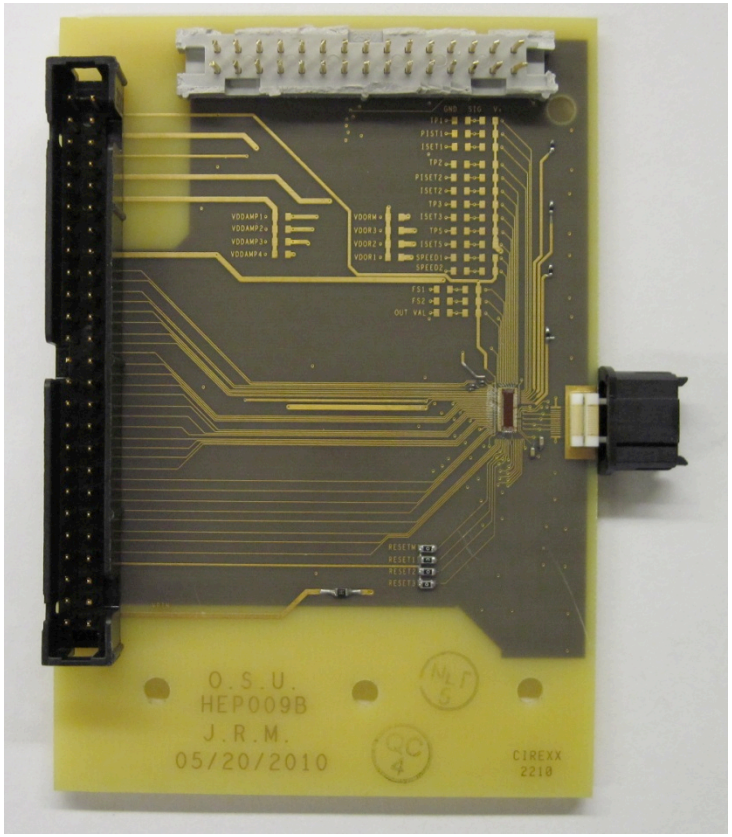
Courtesy of FE-I4 of IBL

Prototype: majority voting from 3 command decoders
Production: majority voting from up to 11 command decoders



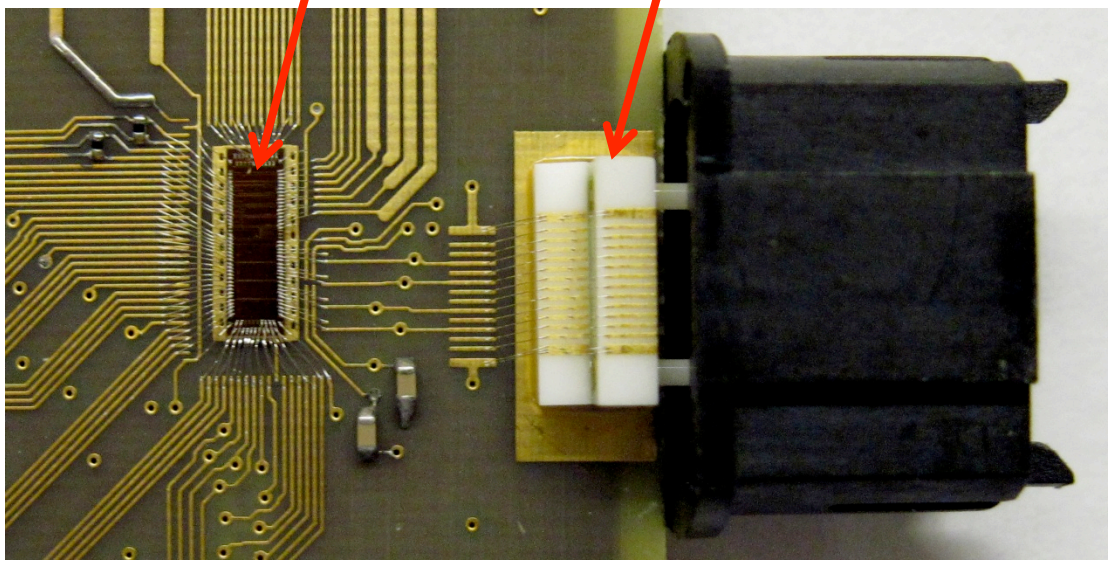
Test Card

Test card



chip

PIN opto-pack
ULM 5 Gb/s



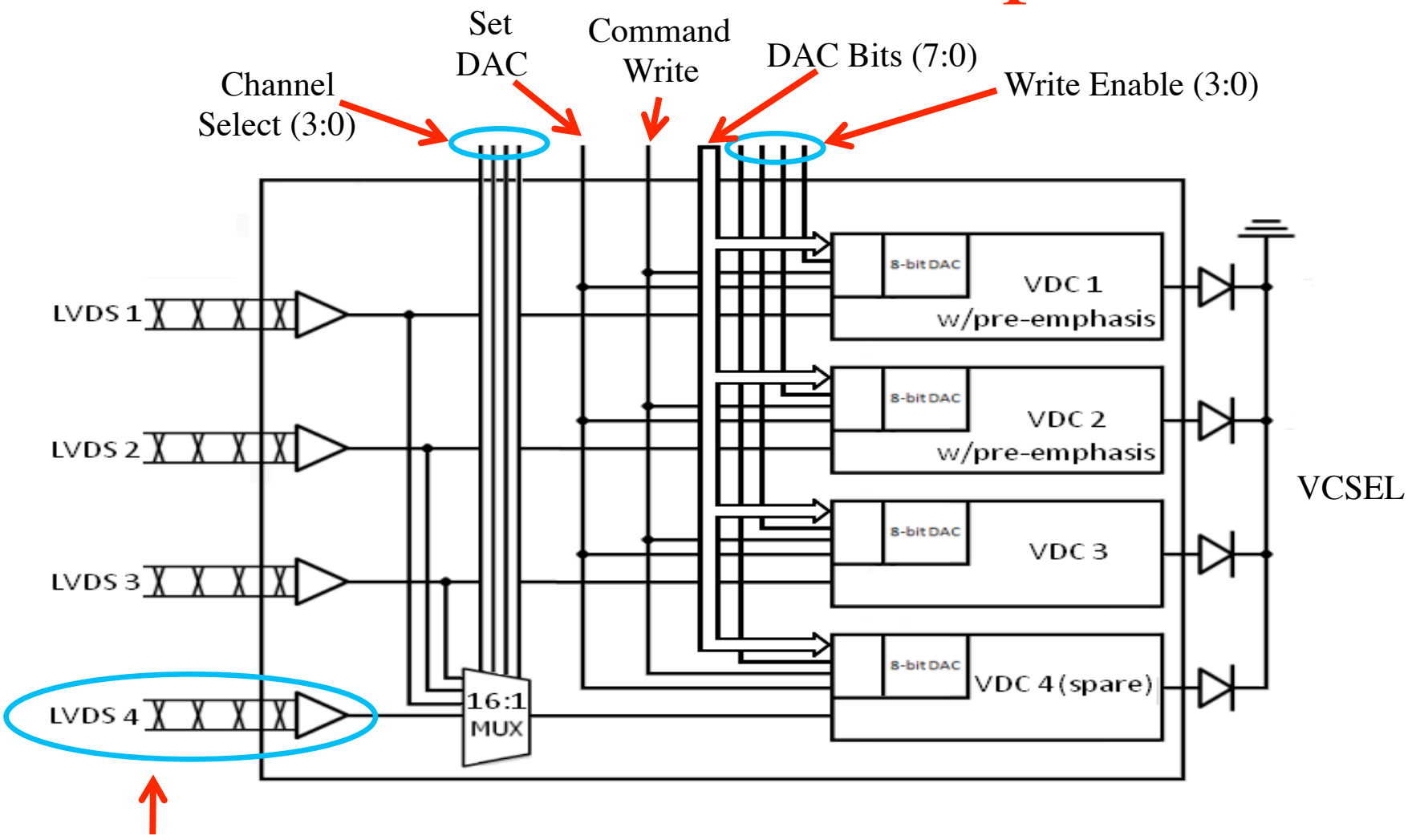
Jitters/Thresholds

- ✔ Peak-to-peak clock jitter: 132 ps
- ✔ Threshold for no bit errors:
  - spare: 40 μA
  - Ch 1: 19 μA
  - Ch 2: 22 μA
  - Ch 3: 20 μA

PIN Receiver/Decoder

- ✔ All channels work at 40 Mb/s
- ✔ Steering signal to the spare channel works with test port
  - ✘ steering via command decoder from FE-I4 not working
    - ◆ mis-communication between Ohio/Genova
    - ⇨ scan chain enable left floating

VCSEL Driver Chip

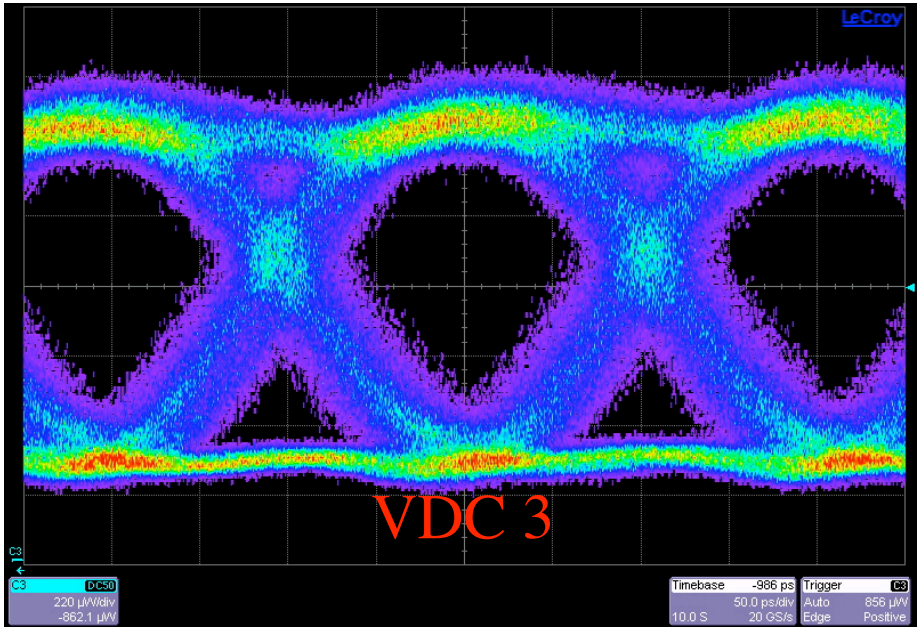


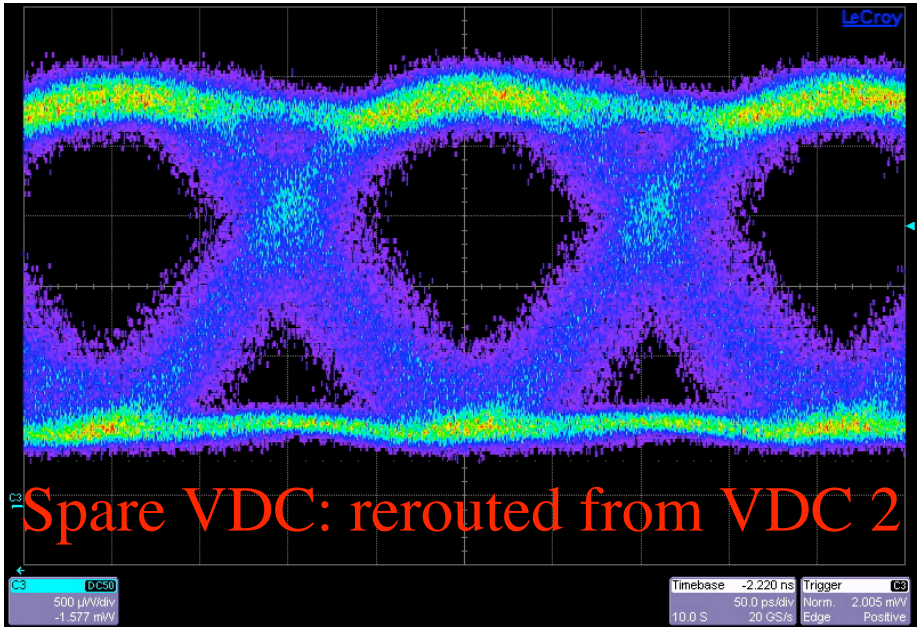
LVDS input added for prototype chip only.

VDC Results

- Power-on reset circuit
  - an open control line disables 6 opto-links in current pixel detector
    - ⇨ implemented power-on reset circuit in prototype chip
    - ✔ chips power up with several mA of VCSEL current
- Test port
  - ✔ can steer signal received to spare VDC/VCSEL
  - ✔ can set DAC to control individual VCSEL currents
- ✔ All 4 channels run error free at 5 Gb/s
  - ✔ includes the spare with signal routed from the other LVDS inputs

Eye Diagrams @ 4.8 Gb/s



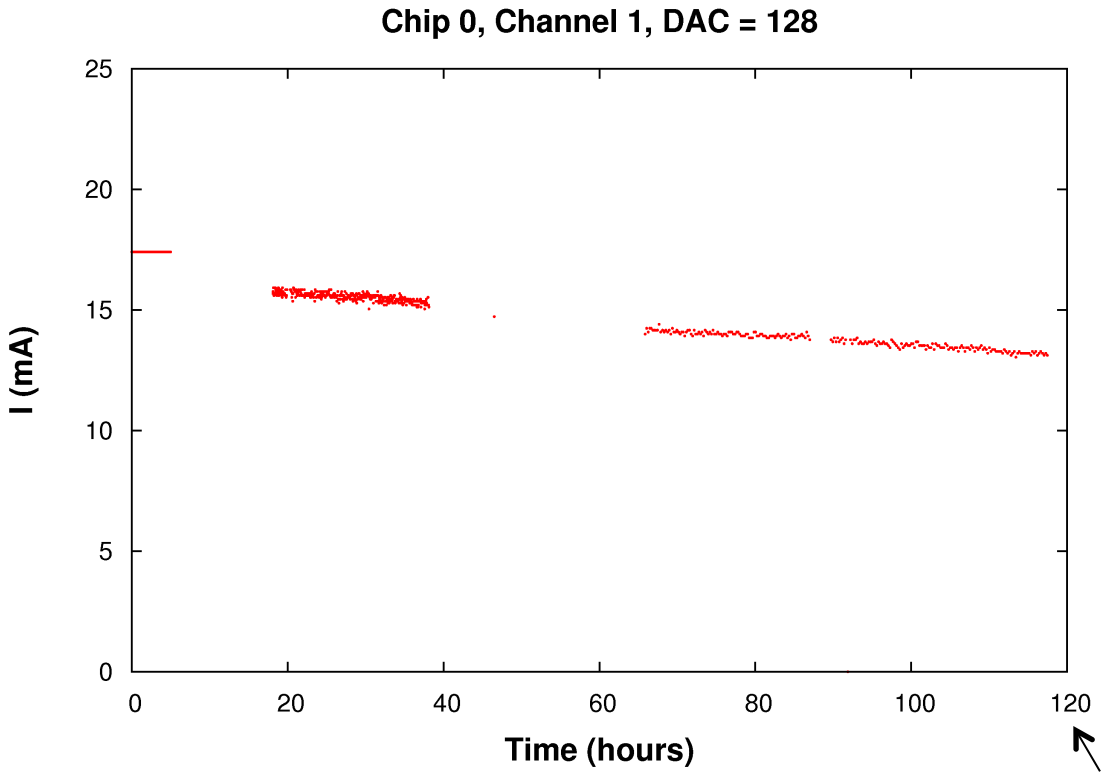


- No pre-emphasis
- Rise/fall times: ~60-90 ps
  - Measured with 4.5 GHz optical probe
- Bit error rate < 5×10^{-13}

Irradiation

- 2 chips were packaged for irradiation with 24 GeV/c protons at CERN in August
  - each chip contains 4 channels of drivers and receivers
  - total dose: 1.6 x 10^{15} protons/cm^2
  - all testing are electrical to avoid complications from degradation of optical components
    - ⇨ long cables limited testing to low speed
  - ✔ observe little degradation of devices
    - evaluation of full performance await return of devices to labs

VDC Irradiation 2010



1.6×10^{15} p/cm^2

- New VDC also drives 25 Ω with constant control current
- Decrease in drive current is small!
  - Fixed the problem observed in previous prototype

Single Event Upset

- SEU harden latches or DAC could be upset by traversing particles
  - 126 latches per 4-channel chip
  - SEU tracked by monitoring the amplitude of VDC drive current
  - 13 instants (errors) of a channel steered to a wrong channel in 71 hours for chip #1
    - similar upset rate in chip #2
    - ⇨ $\sigma = 1 \times 10^{-16}\ cm^2$
    - particle flux $\sim 3 \times 10^{9}\ cm^{-2}$/year @ opto-link location
    - ⇨ SEU rate $\sim 3 \times 10^{-7}$/year/link

Implications for Other Sub-systems

- FE: none
- Fibers: none
- Electrical service: need 1.5 V power supply
  - recommend: add wires for 1.5 V supply
  - working on regulator to derive 1.5 V from 2.5 V supply
- TX/BOC:
  - none if use fiber patch cords to reroute at USA15 to bypass dead links
  - recommend: 12-channel TX/BOC

Summary

- New QSP project advances IBL opto-links schedule significantly
- New 4-channel driver/receiver chips with redundancy and other improvements work well
- Propose to submit 12-channel version in February 2011