



# Radiation-Hard/High-Speed Parallel Optical Links

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# Outline



- Introduction to a compact solution
- Results with 5 Gb/s VCSEL array driver
- Summary



# Use of VCSEL Arrays in ATLAS



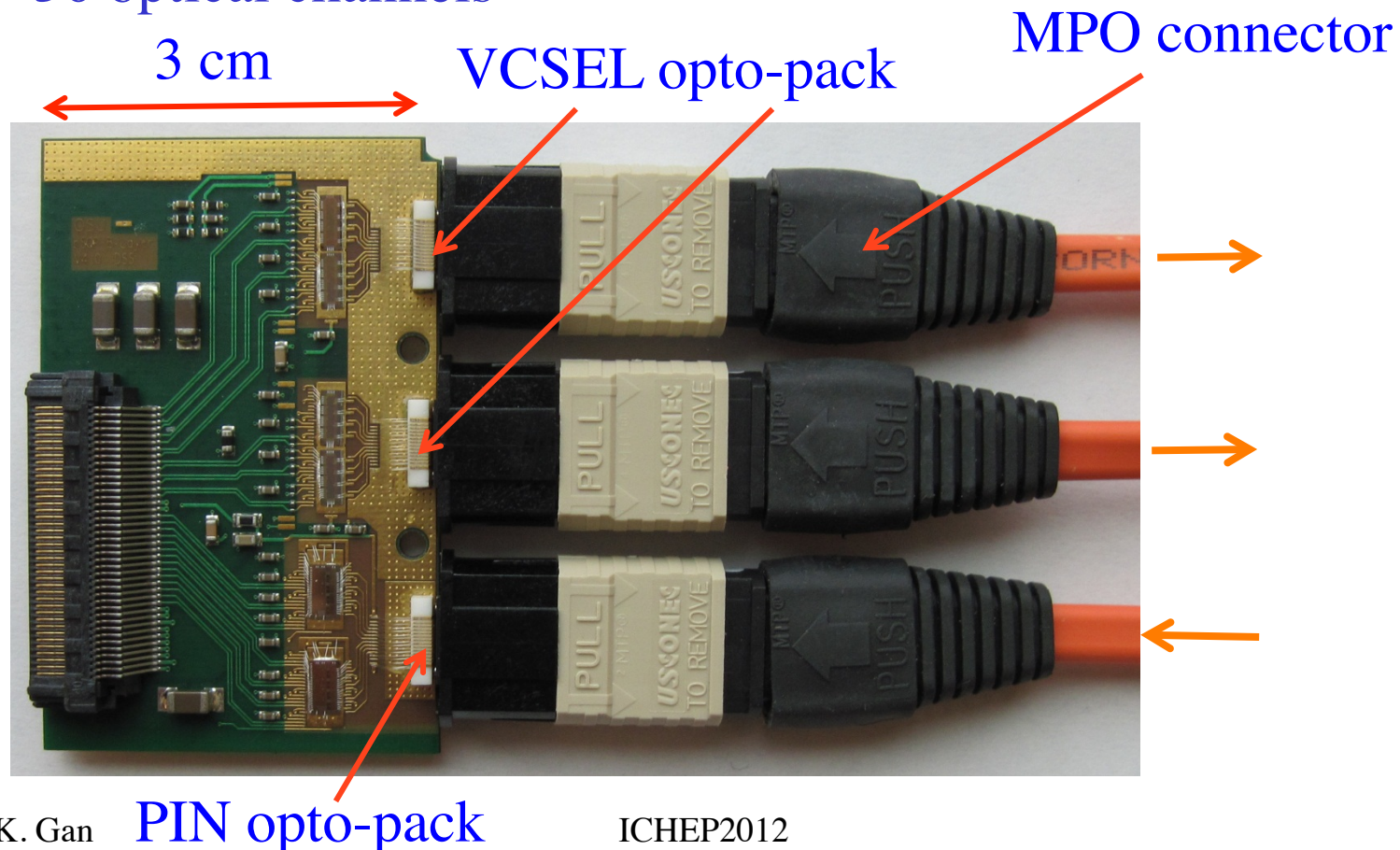
- Widely used in off-detector data transmission
- First on-detector implementation in pixel detector
  - ◆ experience has been positive
    - VCSELs used are humidity sensitive but they are installed in very low humidity location
    - modern VCSELs are humidity tolerant
    - ⇒ will use arrays for next pixel detector upgrade (IBL)



# New Parallel Optical Engine



- Improved design for new pixel layer of ATLAS
  - ◆ use 12-channel VCSEL and PIN arrays
  - ⇒ 36 optical channels





# New 12-Channel VCSEL Driver



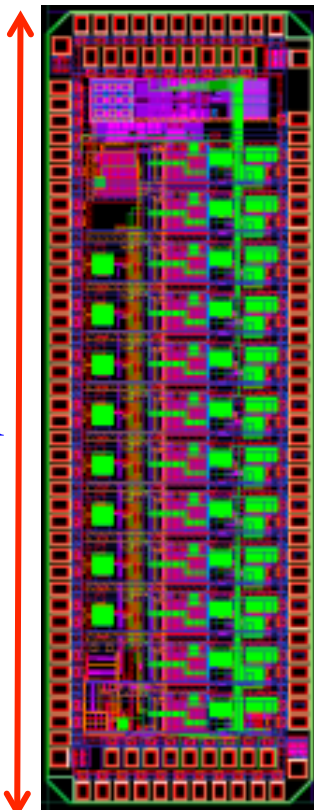
- New ASIC designed using 130 nm CMOS
- Incorporate improvements taking advantage of experience from 1<sup>st</sup> generation parallel optical engine:
  - ◆ redundancy to bypass a broken VCSEL
    - special thanks to FE-I4 group (Roberto Beccherle et al.) for command decoder circuit
  - ◆ power-on reset in case of communication failure:
    - no signal steering
    - 10 mA modulation current (on current)
    - 1 mA bias current (off current)
- Will only operate at 160 Mb/s for new pixel layer but designed ASIC to operate at much higher speed (5 Gb/s) to gain experience in designing high-speed parallel driver



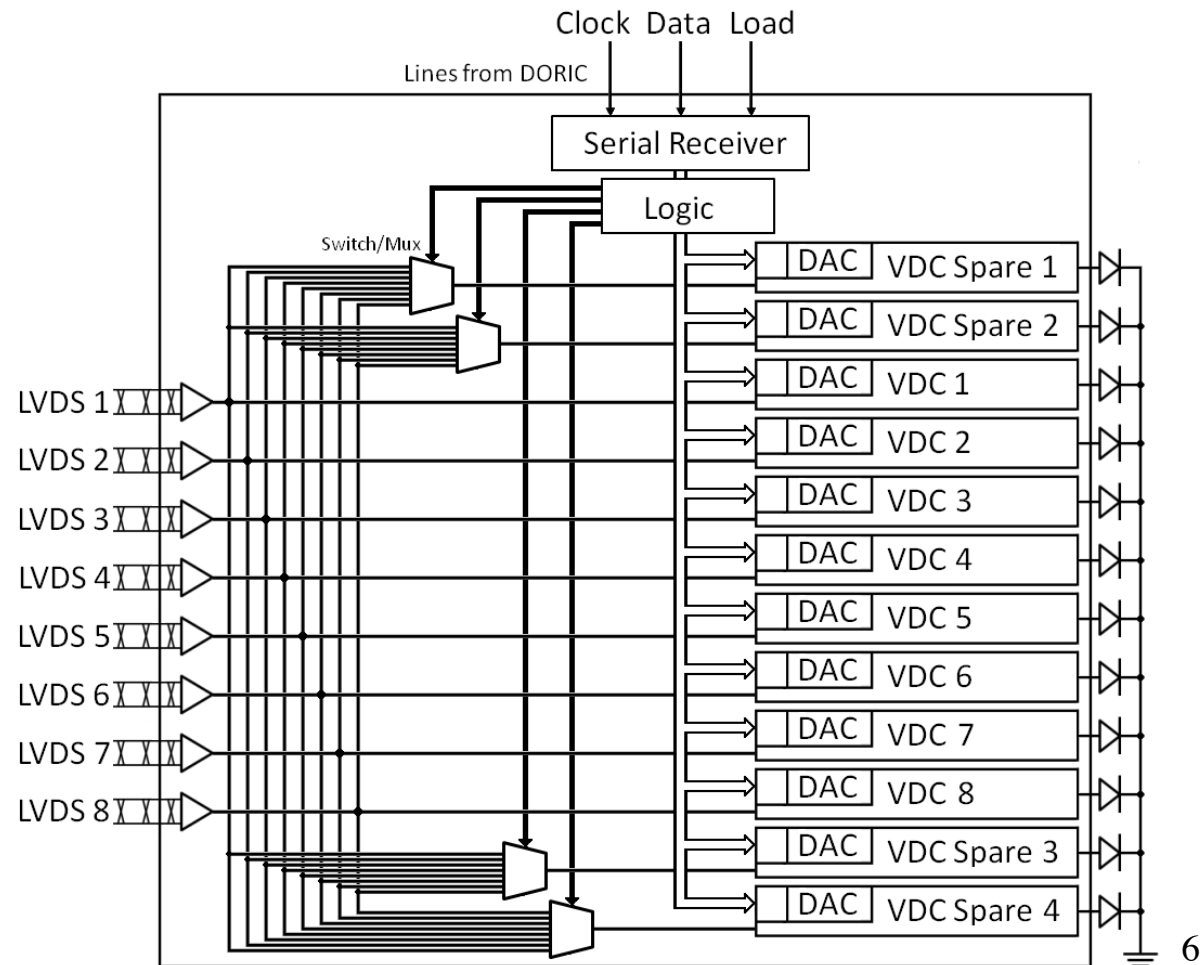
# New VCSEL Array Driver

- Only inner 8 channels connected to new pixel modules
  - ◆ future driver should reserve only one channel for redundancy

4.5 mm



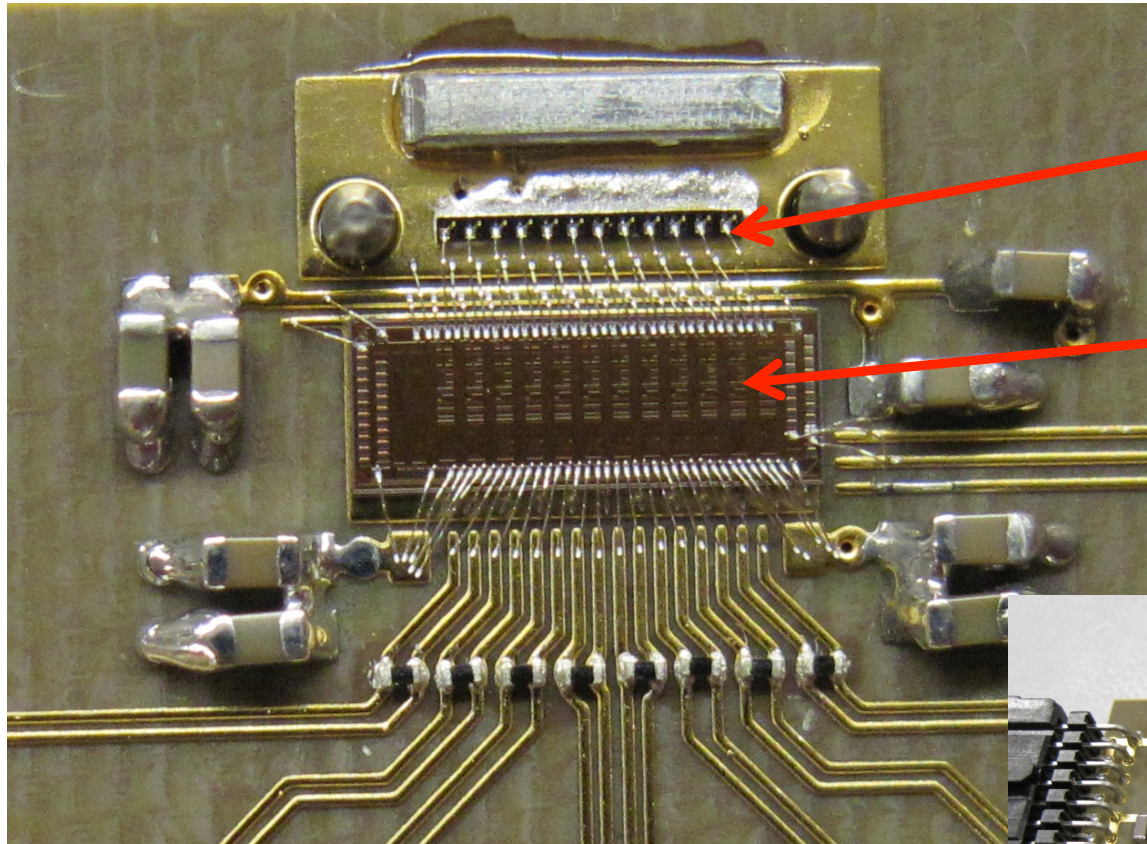
K.K. Gan







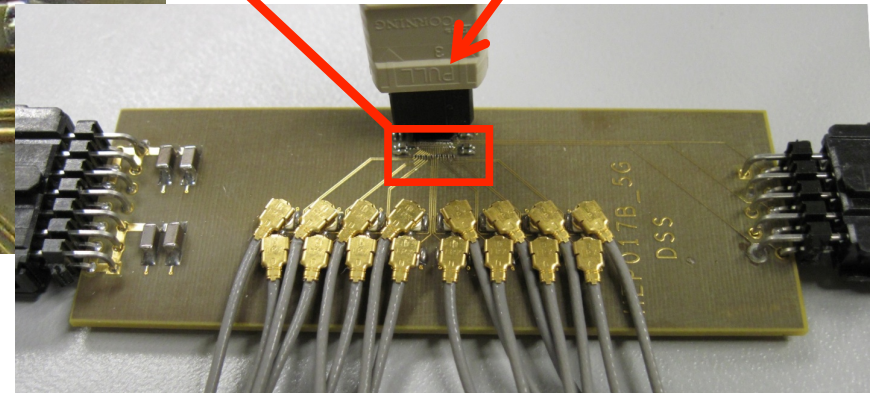
# High-Speed Test Configuration



10 Gb/s ULM  
VCSEL array

VCSEL  
array driver

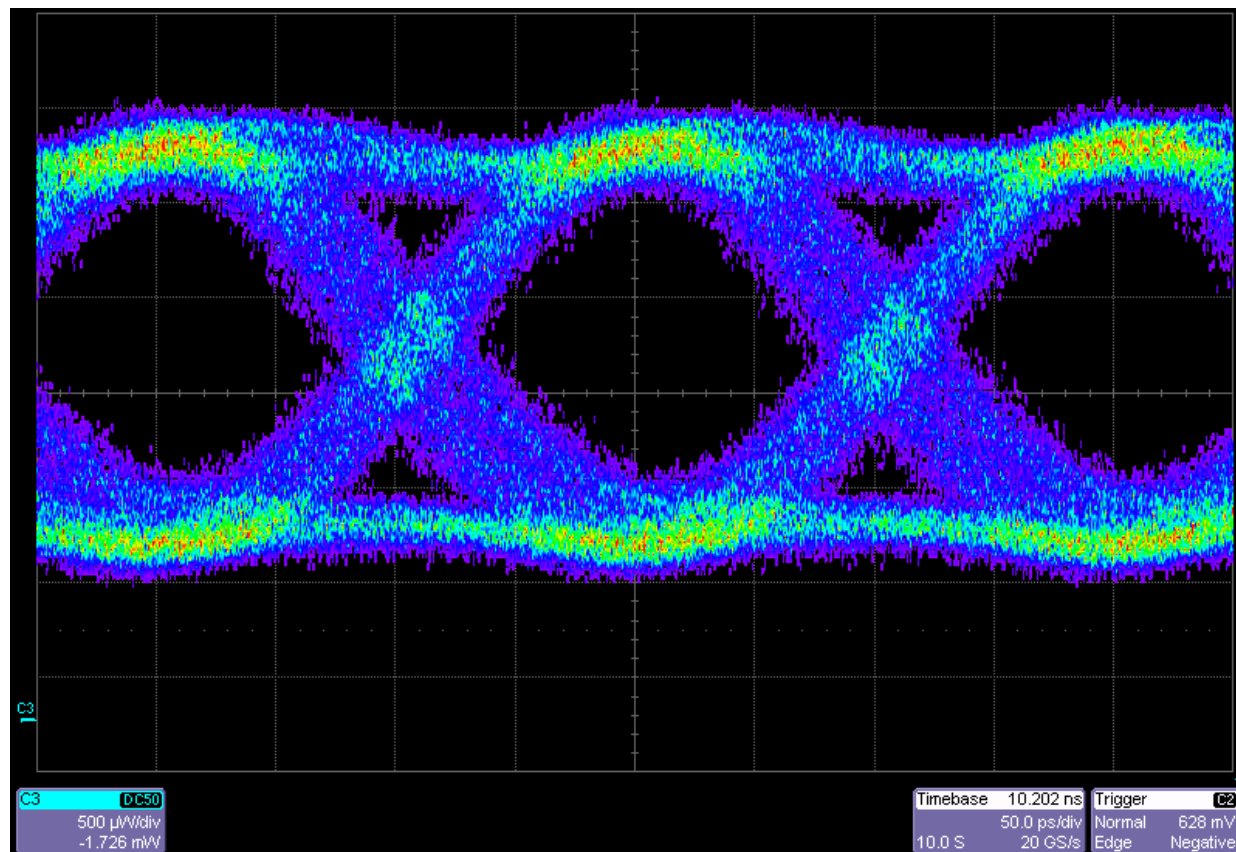
MPO connector





# Optical Eye Diagram

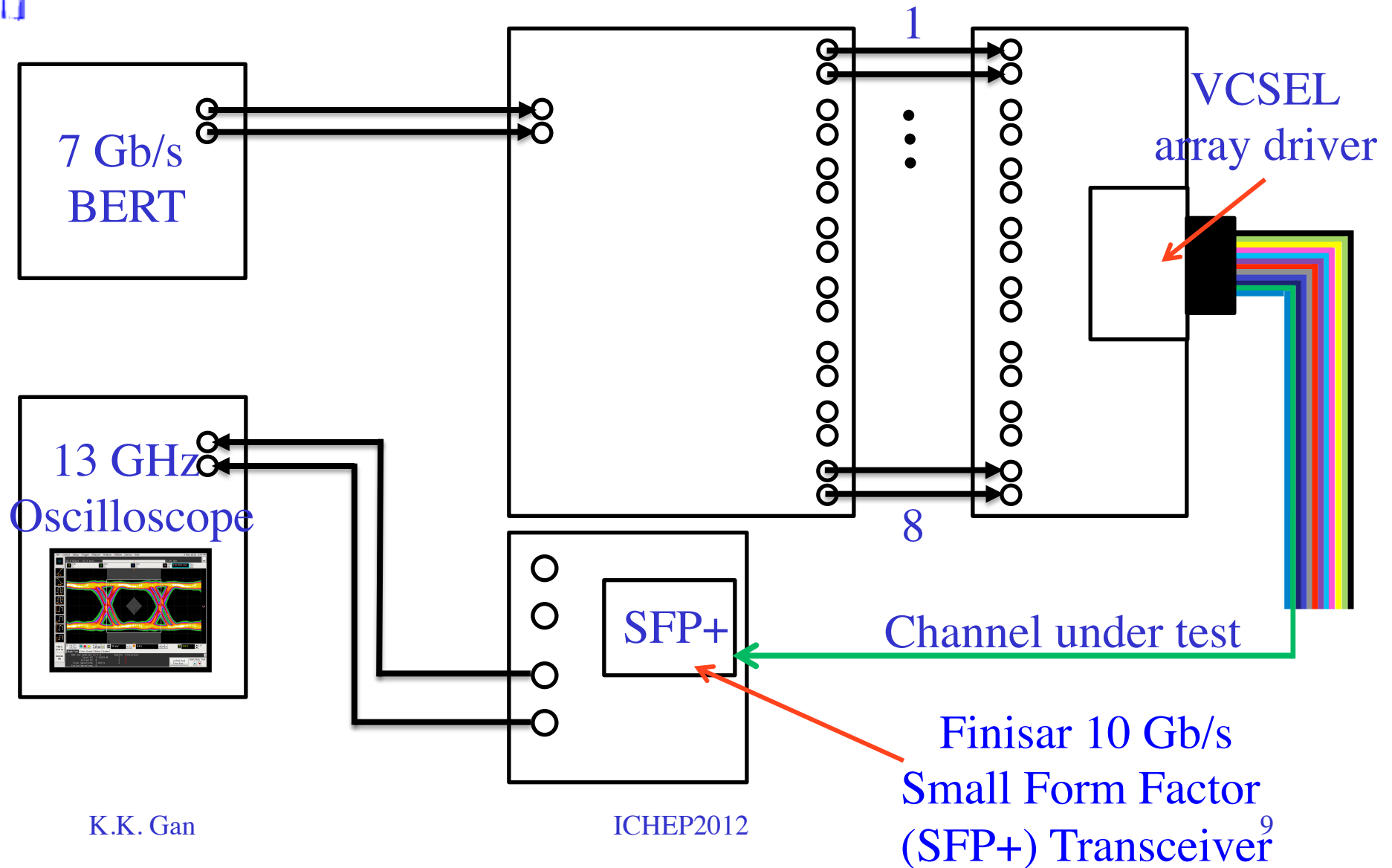
- Difficult to judge eye diagram with 4.5 GHz optical probe...







# SFP+ as Optical Probe



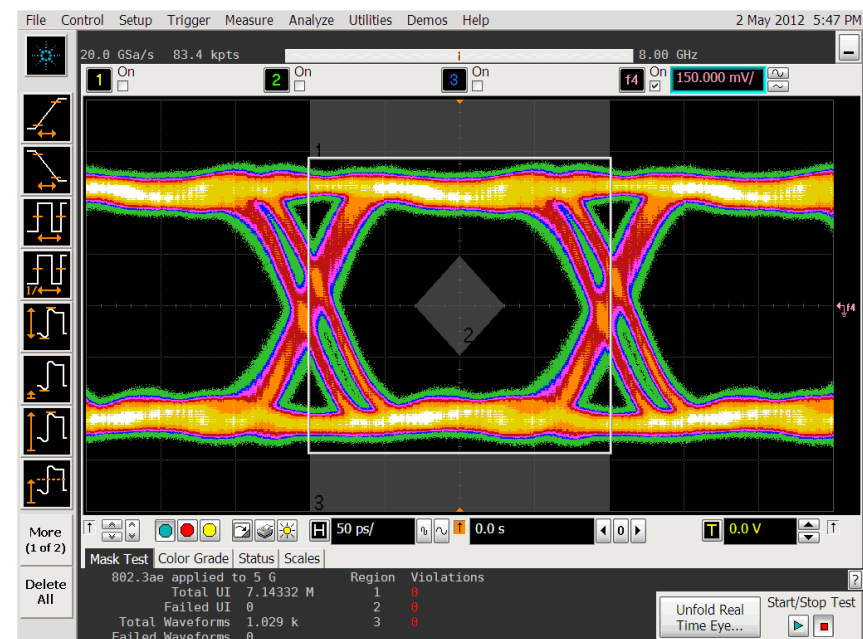
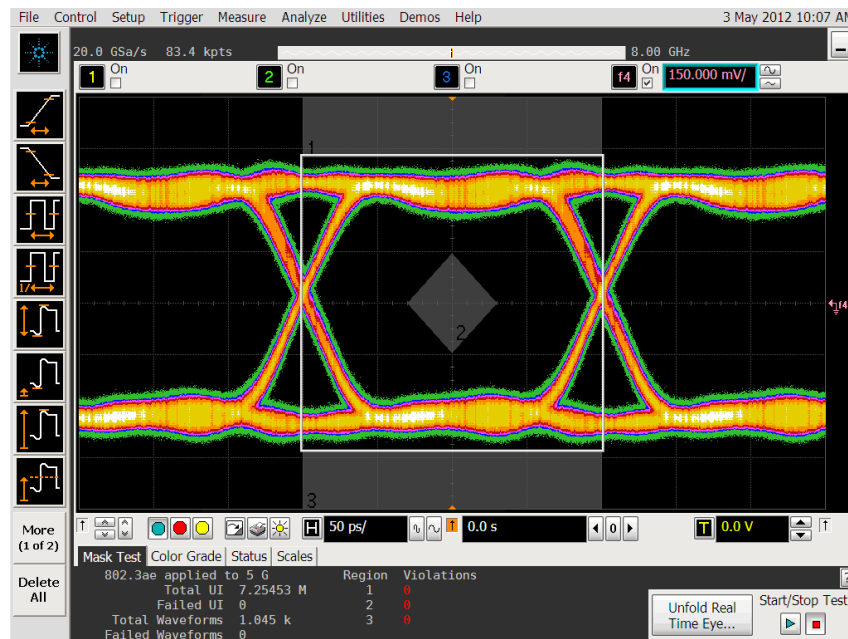


# SFP+ Loopback vs VCSEL Driver



10 Gb/s SFP+ transceiver @ 5 Gb/s  
with optical loopback

VCSEL driver @ 5 Gb/s  
after 10 Gb/s SFP+ receiver

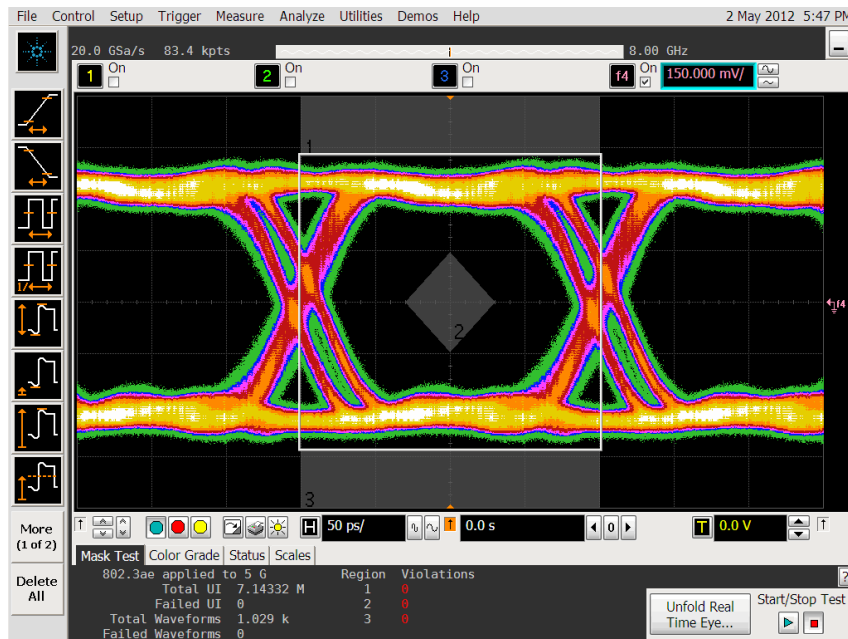




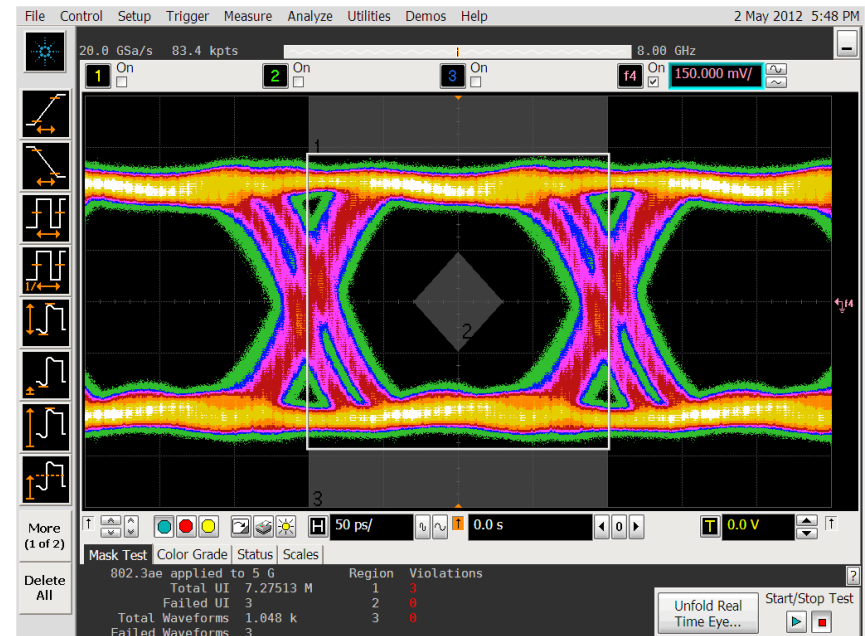
# Eye with One/All Channels Active



One channel active



All channels active

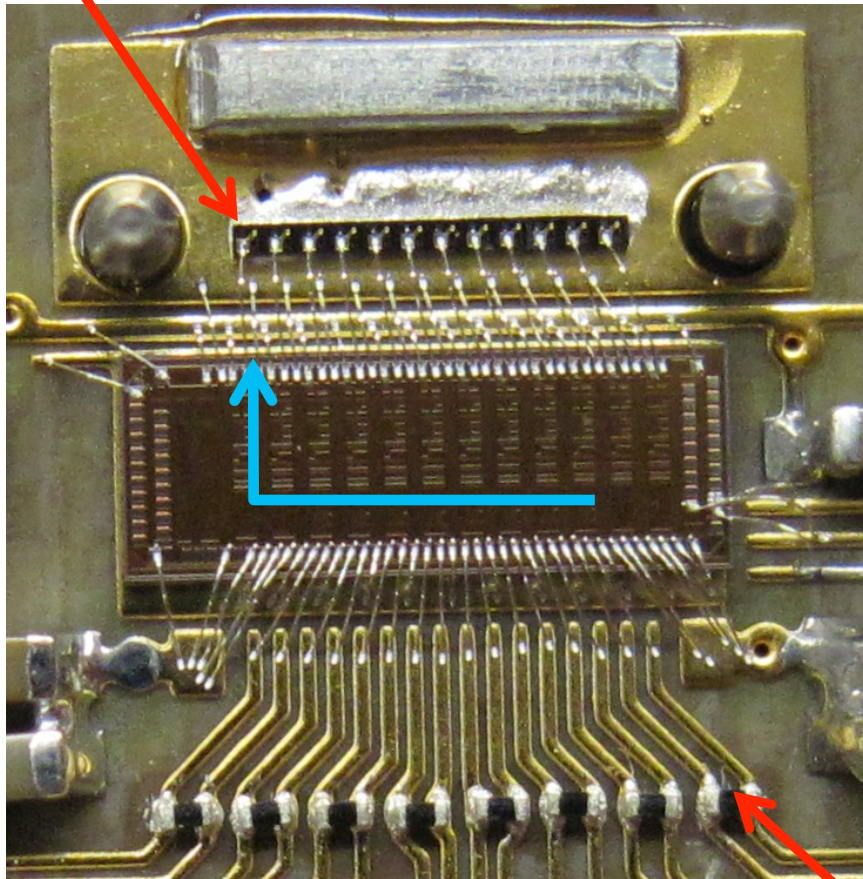


- all channels work @ 5 Gb/s with bit error rate  $< 5 \times 10^{-13}$  for all channels active
- jitter increases with all channels active but still passes the mask test



# Effect of Steering on Eye

VCSEL spare 1



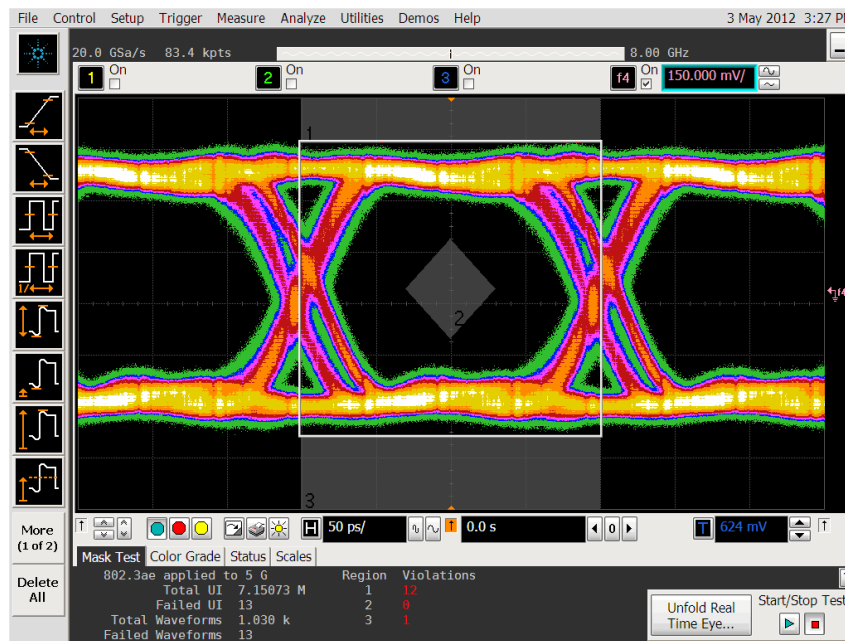
Receiving LVDS signal  
from channel 8, steering  
to VCSEL spare 1

LVDS in channel 8  
ICHEP2012

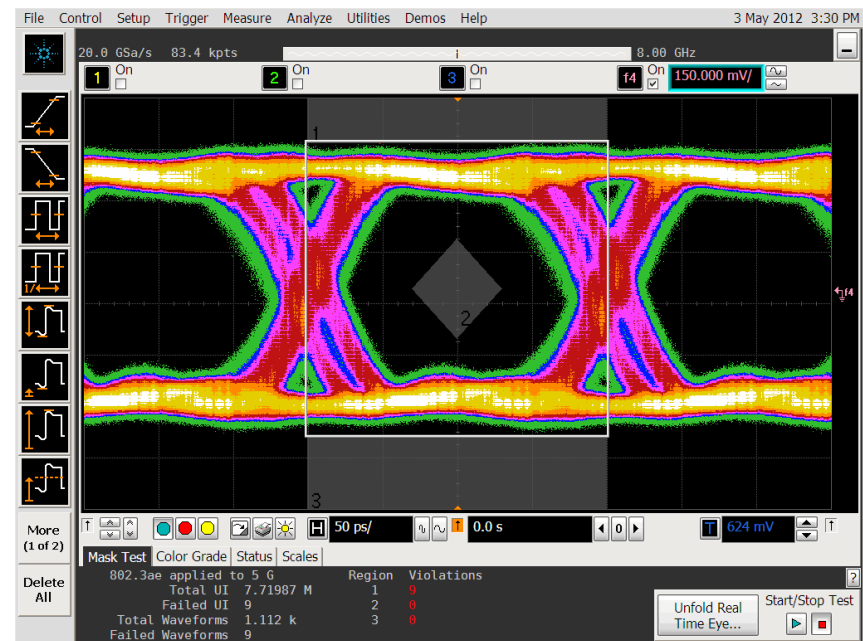


# Effect of Steering on Eye

Spare 1 output with other channels off



Spare 1 output with all channels active



- steered channel still passes the mask test
- ◆ jitter increases with all channels active



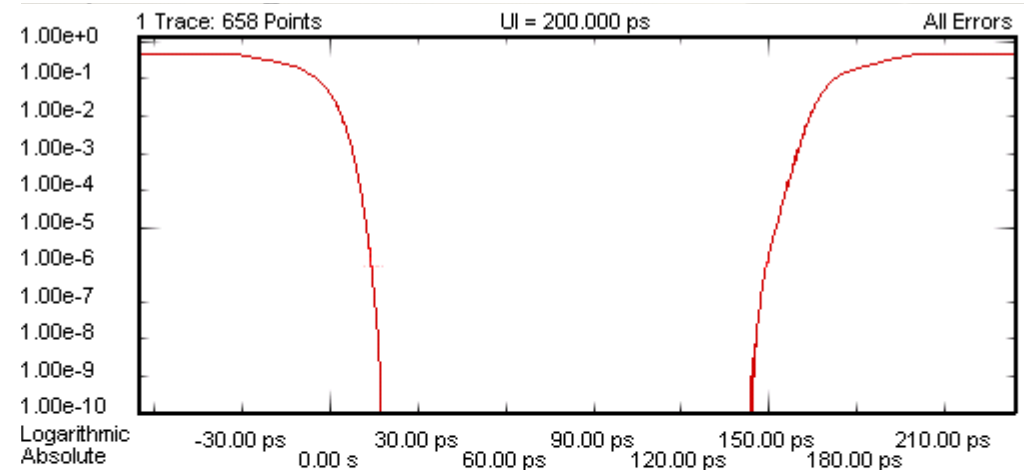


# Jitter Measurement



- measured on the spare channel with signal rerouted across die
  - ◆ should be the worse case scenario
- all other channels active

Total Jitter @ BER $10^{-12}$	65 ps
Random Jitter	3.1 ps
Total DJ	36.8 ps





# Radiation Hardness



- 10 Gb/s VCSEL arrays have been proven to be radiation hard to tens of Mrad
  - ◆ send signal on ~1 m micro co-ax cables to less radiation and more serviceable location
- Radiation hardness of VCSEL array driver will be verified in the summer



# Future Plan



- 10 Gb/s transmission needed for ATLAS inner pixel layer and LAr readout upgrades
  - ◆ joint ATLAS/CMS proposal funded via US DOE generic R&D program
- Layout array VCSEL driver/PIN receiver using GBLD and GBTIA with redundancy for possible pixel applications



# Summary



- VCSEL array offers compact solution to data transmission
- 5 Gb/s VCSEL array driver successfully prototyped
- Currently designing 10 Gb/s VCSEL array driver