Radiation-Hard ASICS for Optical Data Transmission in the First Phase of the LHC Upgrade

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Outline

- Introduction
- Result on VCSEL Driver Chip
- Result on PIN Receiver/Decoder Chip
- Summary

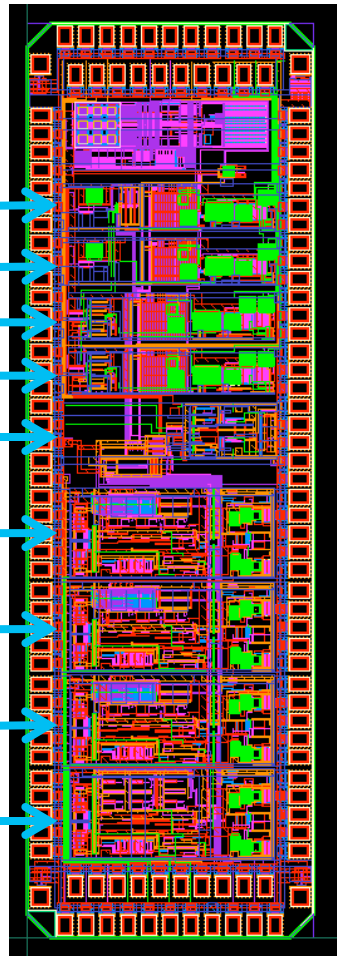
IBL

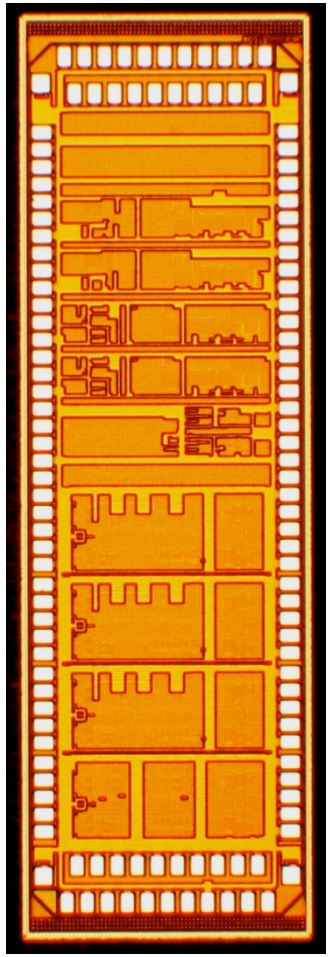
- ATLAS proposed to add one more layer to the current pixel detector:
  - "Inner B-Layer" or IBL
  - installation ~ 2014-6
  - optical links will use VCSEL/PIN array as in current pixel detector
  - an updated version of current driver (VDC) and receiver (DORIC) with redundancy and individual VCSEL current control would be a logical improvement
    - experience gained from the development/testing of such new chips would help the development of on-detector array-based opto-links for SLHC
      - ⇨ submission of 1st prototype chip (130 nm) in 2/2010

Chip Content

Photo

Design





VCSEL Driver (spare)
VCSEL Driver
VCSEL Driver with pre-emphasis
VCSEL Driver with pre-emphasis
CML Driver with pre-emphasis

Decoder (40Mb/s)

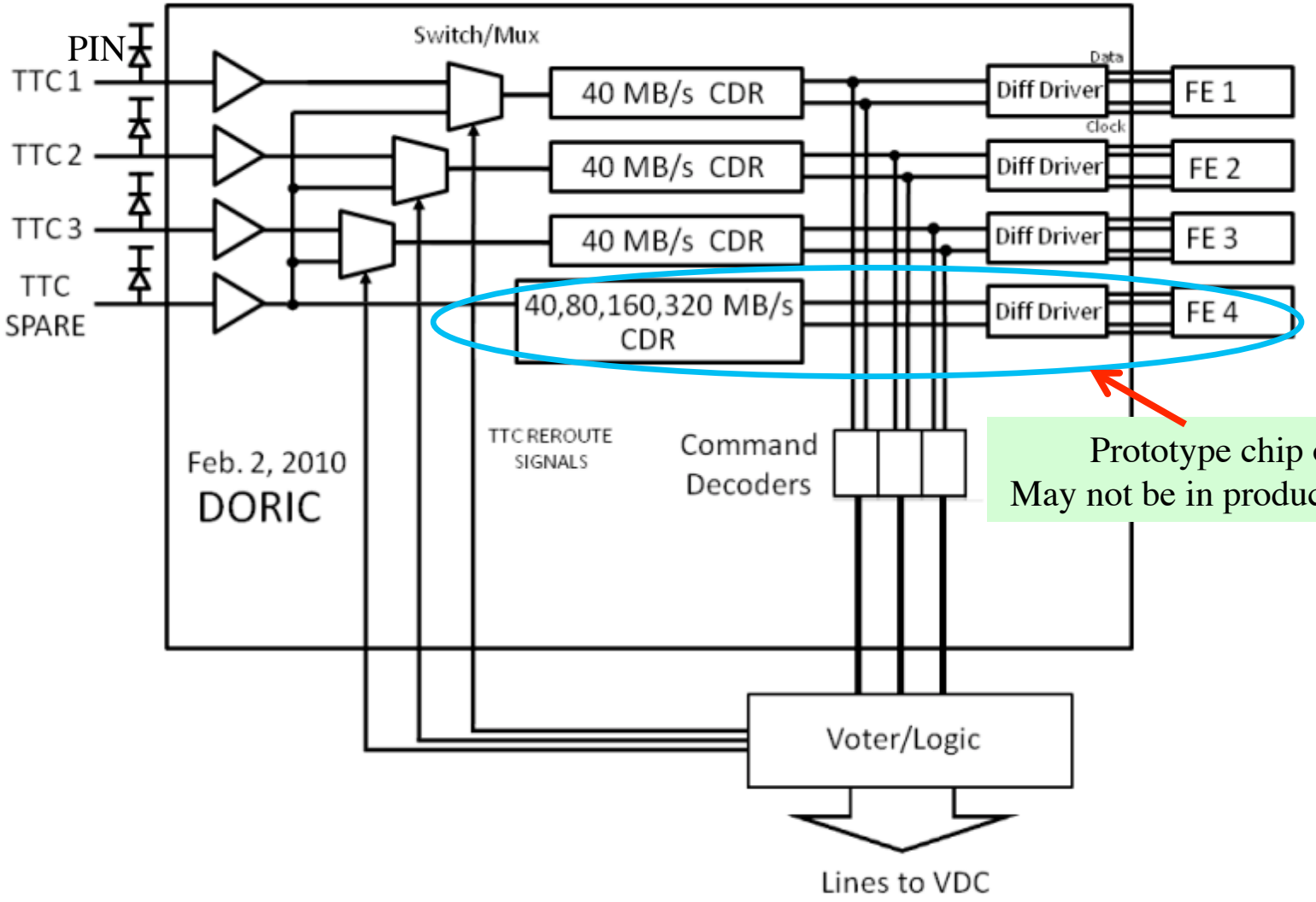
Decoder (40Mb/s)

Decoder (40Mb/s)

Decoder (40/80/160/320 Mb/s, spare)

1.5 mm

PIN Receiver/Decoder

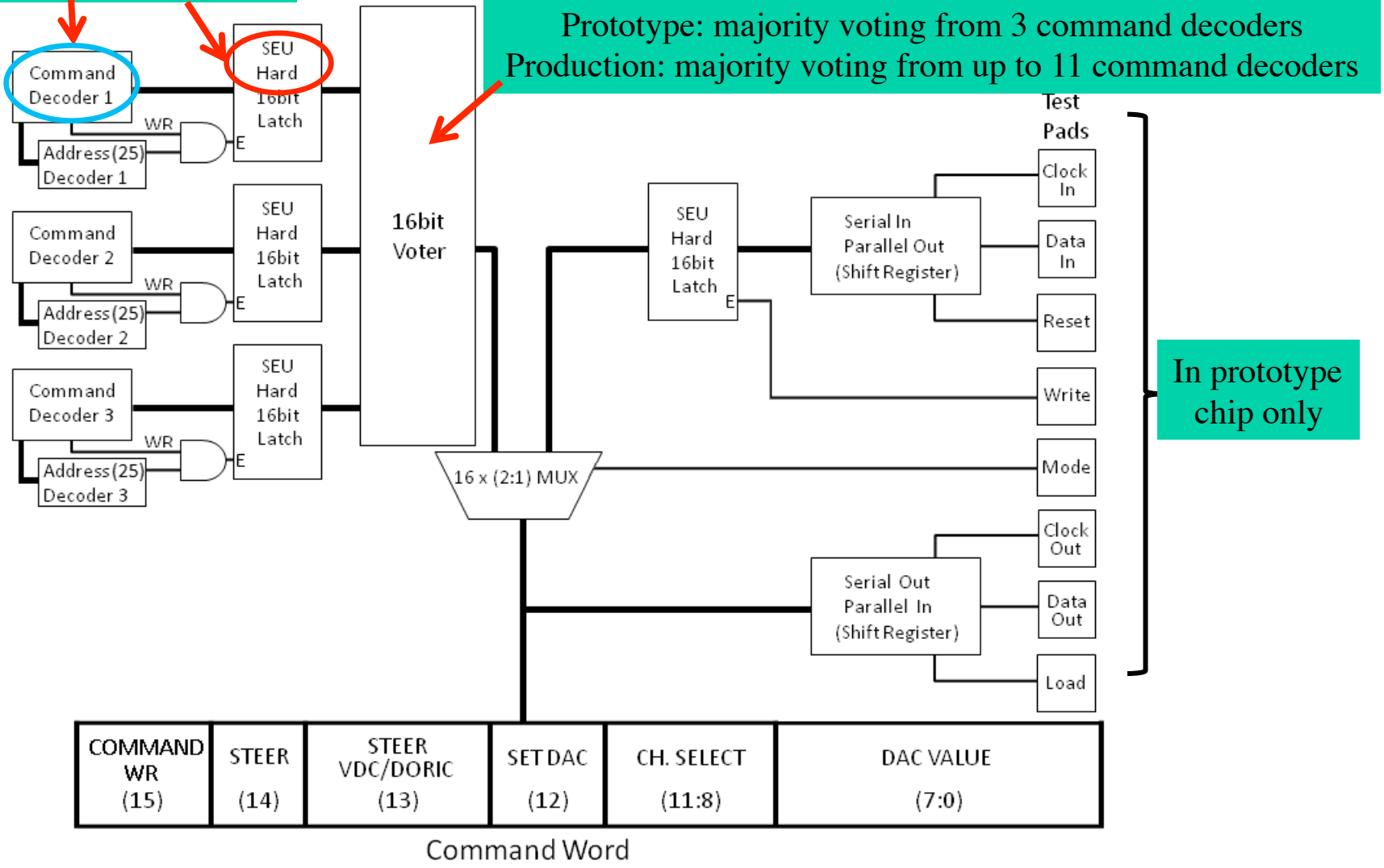


Prototype chip only.
May not be in production chip.

Command Decoder Interface

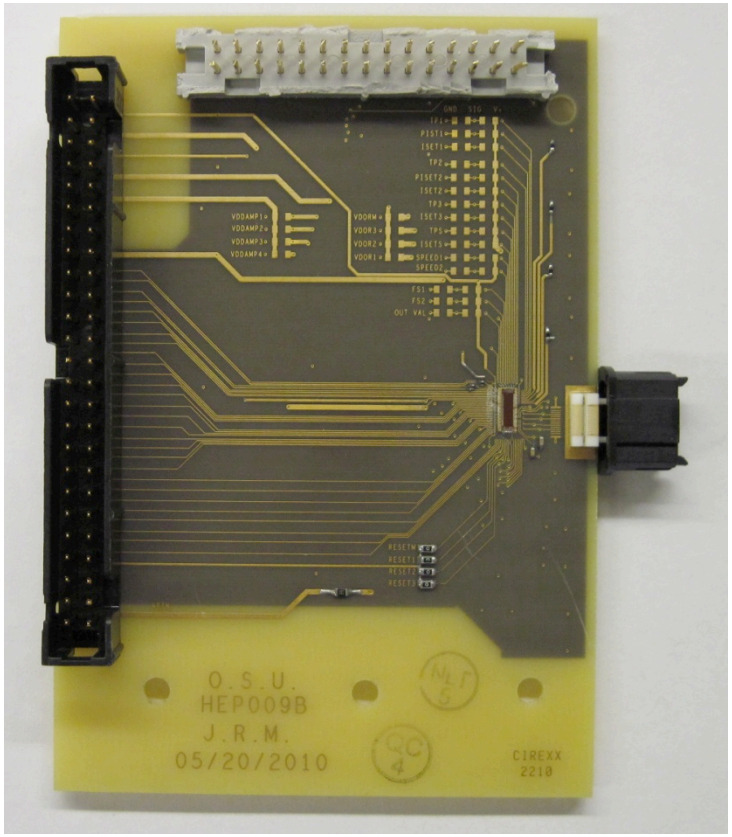
Courtesy of FE-I4 of IBL

Prototype: majority voting from 3 command decoders
Production: majority voting from up to 11 command decoders



Test Card

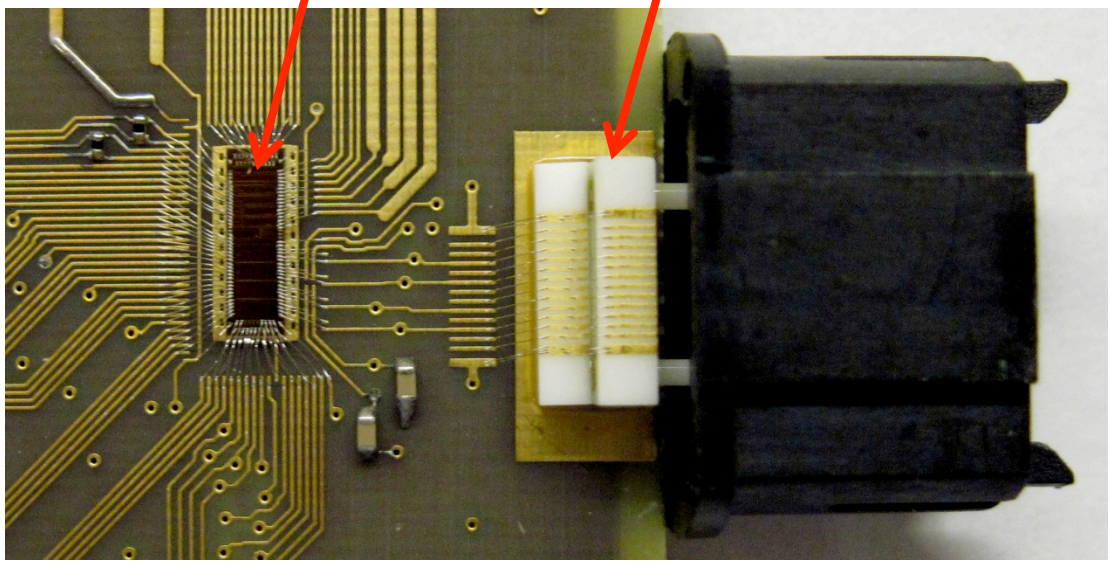
Test card



PIN opto-pack

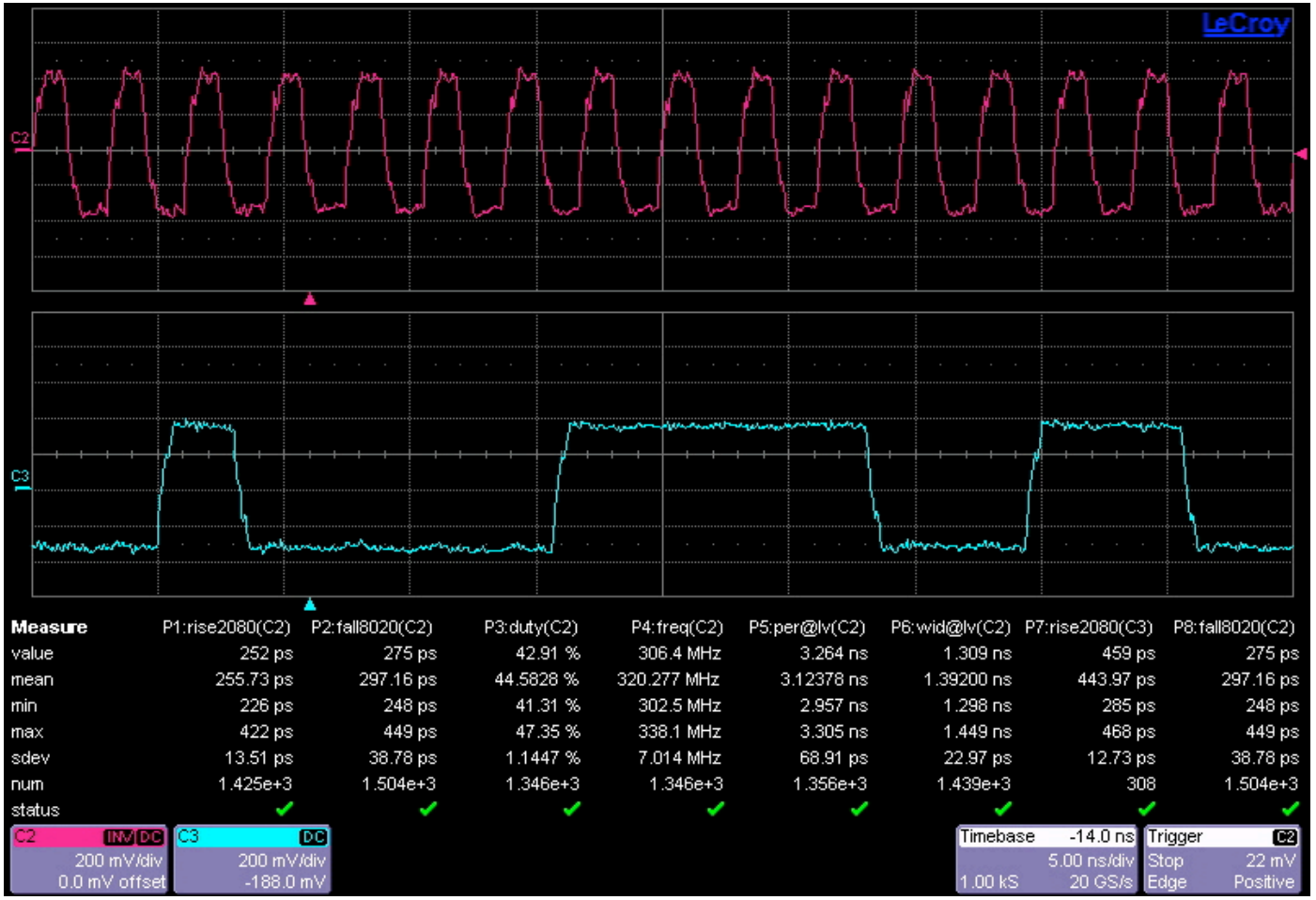
chip

ULM 5 Gb/s



Recovered Clock/Data

320 Mb/s



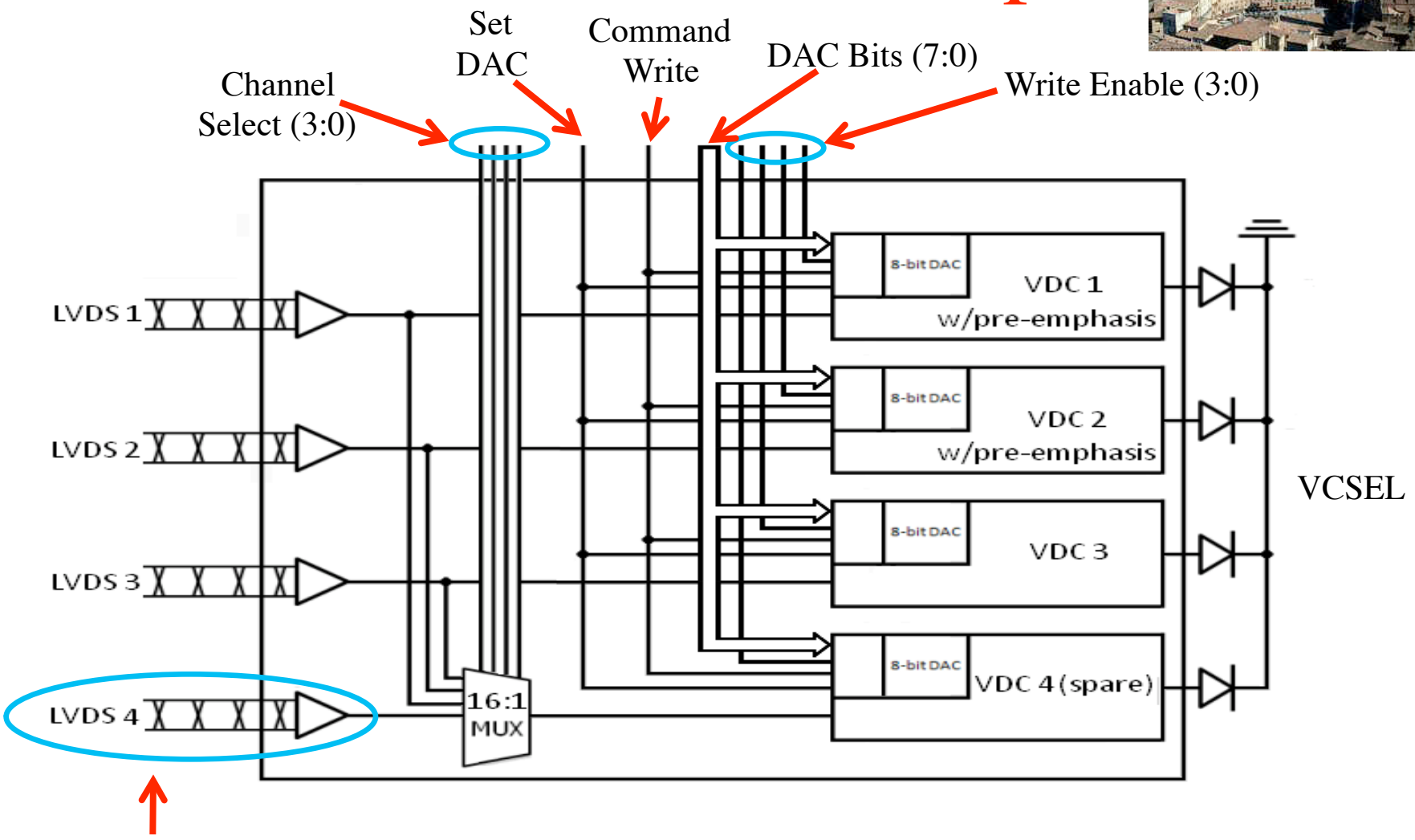
Jitters/Thresholds

- Peak-to-peak clock jitter:
  - 40 Mb/s: 132 ps (normal)
  - 40 Mb/s: 1420 ps (multi speed)
  - 80 Mb/s: 750 ps
  - 160 Mb/s: 193 ps
  - 320 Mb/s: 103 ps
- Threshold for no bit errors:
  - 40 Mb/s:
    - Multi speed: 40 μA
    - Ch 1: 19 μA
    - Ch 2: 22 μA
    - Ch 3: 20 μA
  - 80 Mb/s: 58 μA
  - 160 Mb/s: 74 μA
  - 320 Mb/s: 110 μA

PIN Receiver/Decoder

- ✔ All channels work at 40 Mb/s
- Multi Speed version works at 40, 80, 160, and 320 Mb/s
  - 160 and 320 Mb/s need external bias tuning for proper operation
- ✔ Steering signal to the spare channel works

VCSEL Driver Chip



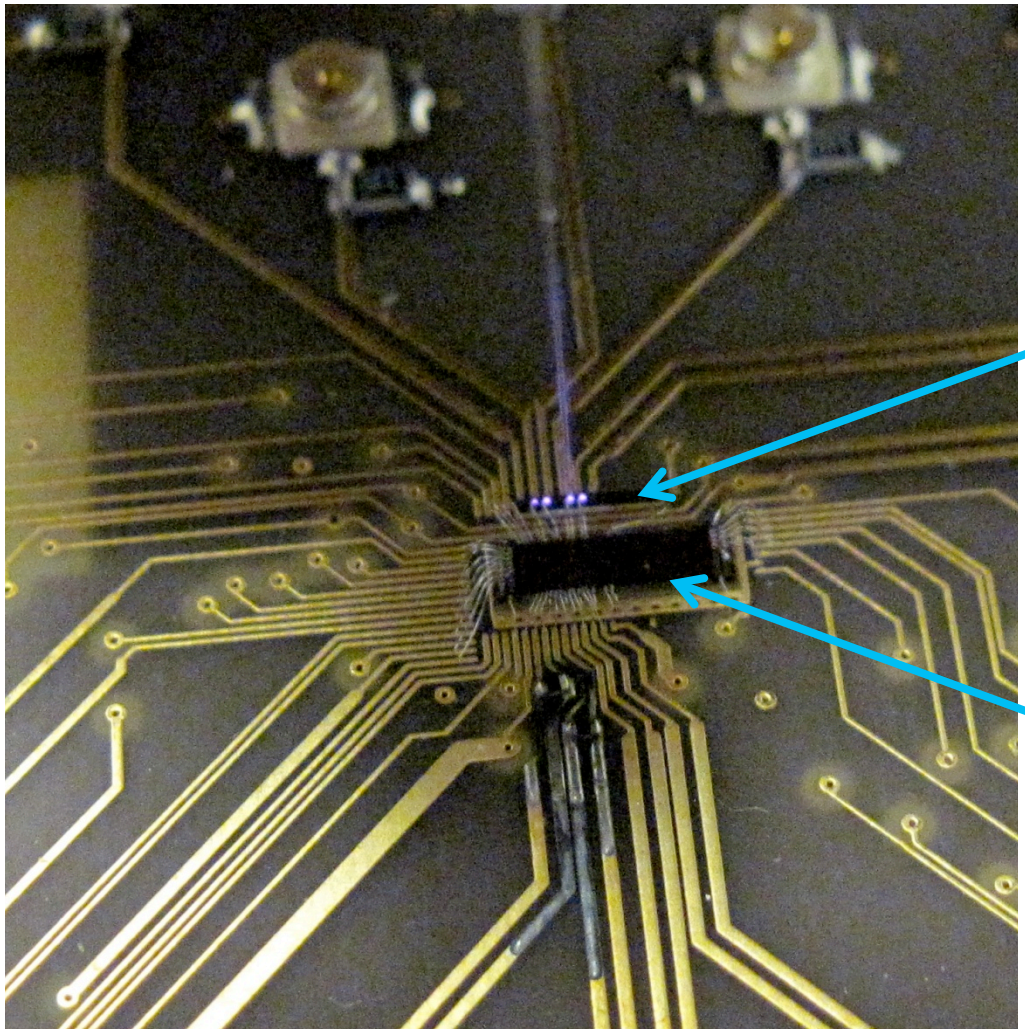
LVDS input added for prototype chip only.
May not be in production chip.

VDC Results

- Power-on reset circuit
  - an open control line disables 6 opto-links in current pixel detector
    - ⇨ implemented power-on reset circuit in prototype chip
    - ✔ chips power up with several mA of VCSEL current
- Test port
  - ✔ can steer signal received to spare VDC/VCSEL
  - ✔ can set DAC to control individual VCSEL currents
- ✔ All 4 channels run error free at 5 Gb/s
  - ✔ includes the spare with signal routed from the other LVDS inputs

VDC Test Setup

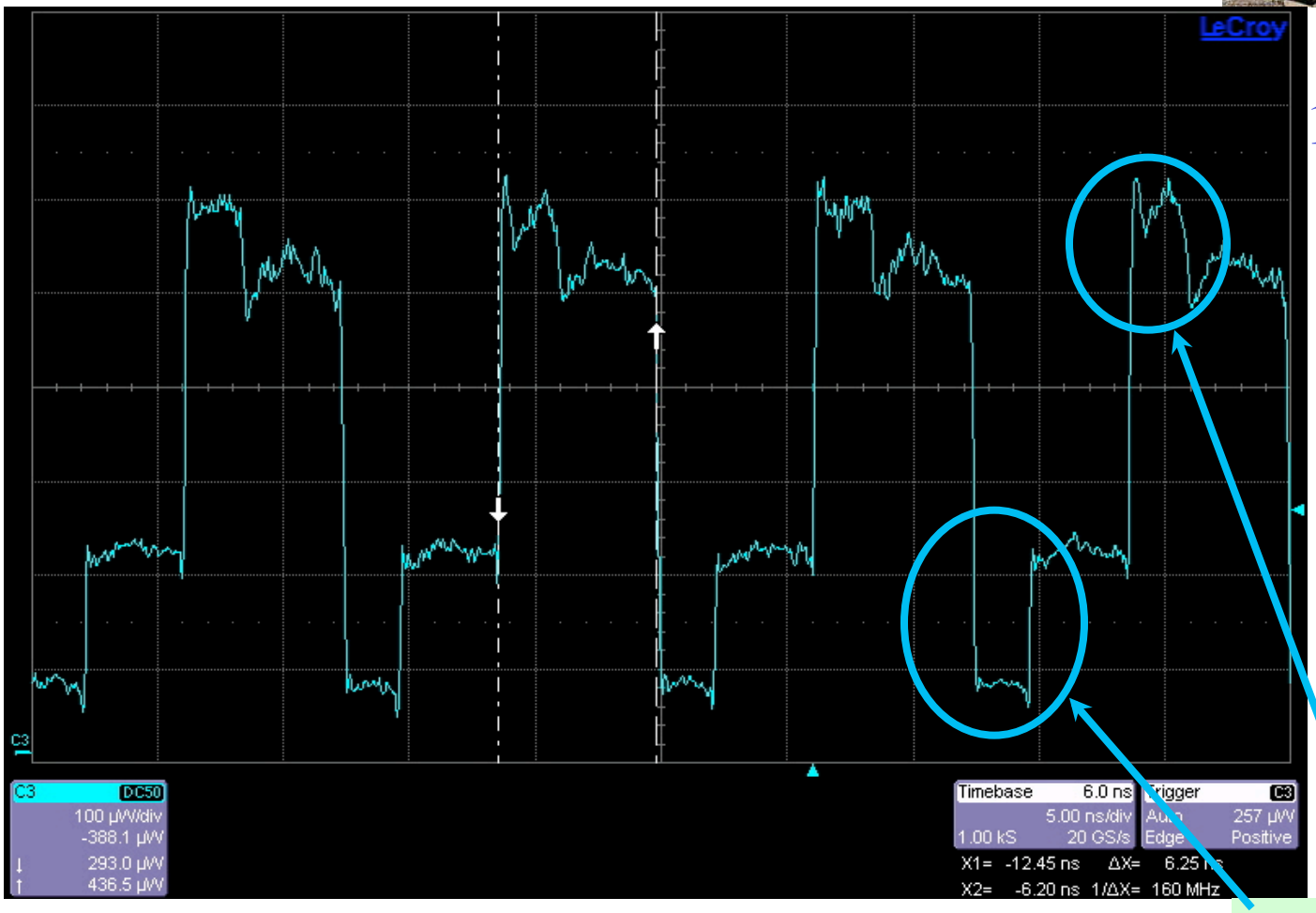
- Light from the 4 VCSELs:
  - Fiber aligned over VDC/VCSEL 2



VCSEL Driver with Pre-Emphasis

160 Mb/s

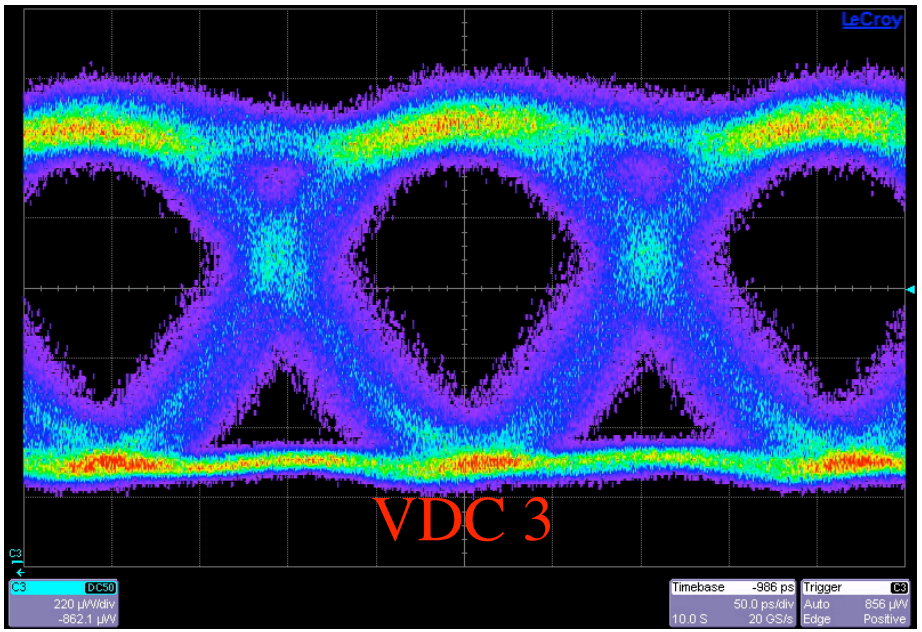
Main amplitude

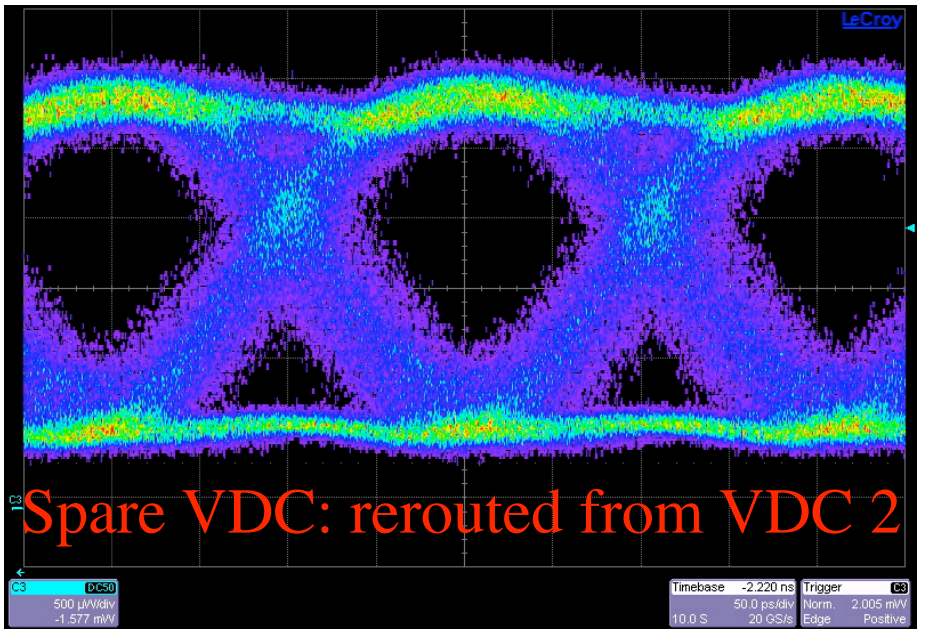


Pre-emphasis

✔ Pre-emphasis working with tunable width and height

Eye Diagrams @ 4.8 Gb/s





- No pre-emphasis
- Rise/fall times: ~60-90 ps
  - Measured with 4.5 GHz optical probe
- Bit error rate < 5×10^{-13}

Summary

- prototyped opto-chip for 2nd generation ATLAS pixel opto-links incorporated experience gained from current links
  - add redundancy to bypass broken PIN or VCSEL channel
  - add individual VCSEL current control
  - add power-on reset to set VCSEL current to several mA on power up
  - ✔ VCSEL driver can operate up to ~ 5 Gb/s with BER < 5×10^{-13}
  - ✔ PIN receiver/decoder properly decodes signal with low threshold
  - ✔ all added functionalities work!

All results are preliminary