Results/Plan on ITK-Pixel Optical Links

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Outline

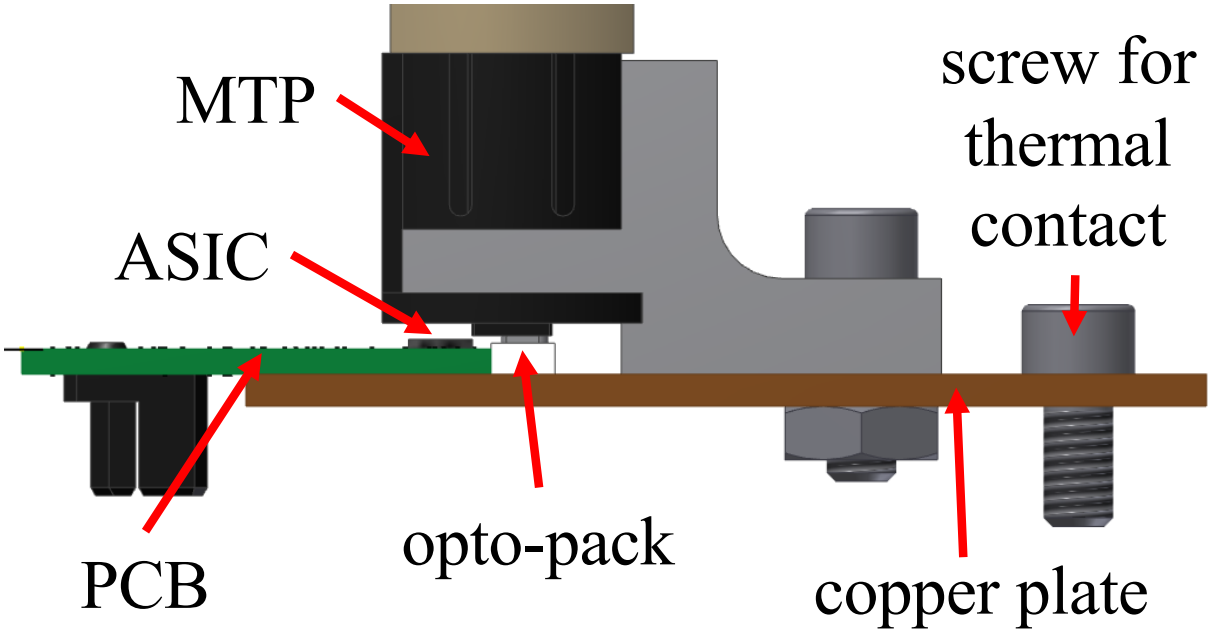
- Introduction
- Results/Plan for Transmitter Opto-Board
- Plan for Receiver Opto-Board
- Summary

Use of VCSEL Arrays in HEP

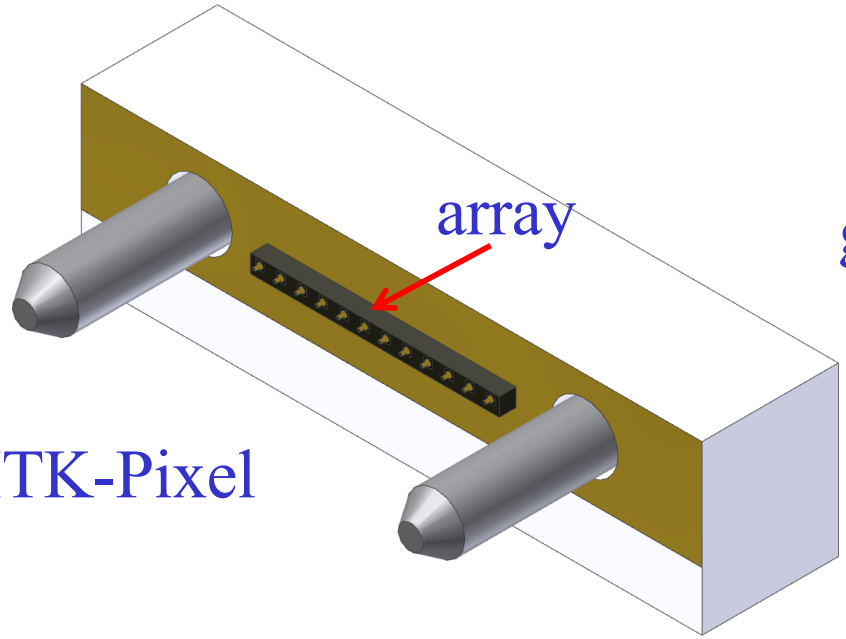
- Widely used in off-detector (no radiation) data transmission
- First on-detector implementation in pixel detector of ATLAS
  - experience has been positive
    - ⇨ use arrays for the second generation opto-links
    - ⇨ logical for HL-LHC ATLAS pixel detector to use 12-channel arrays as in the 1st and 2nd generation optical modules (opto-boards)

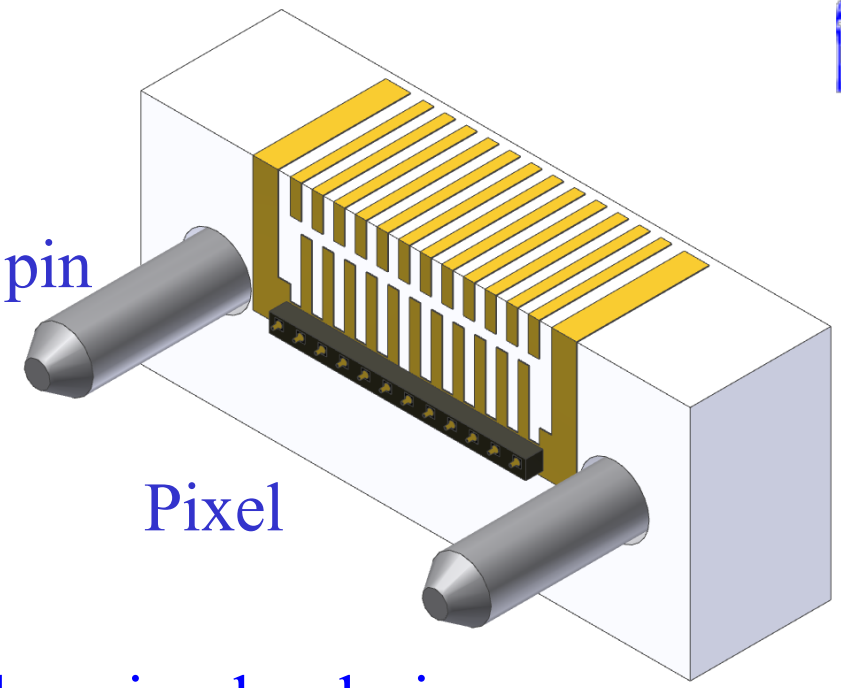
ITK-Pixel Opto-Board Concept

- Keep optical package (opto-pack)
- Keep copper backed PCB
- Keep MTP connector
- Compatible with an opto crate (opto-box) concept
- No lenses/mirrors to turn the light



Opto-Pack for ITK-Pixel

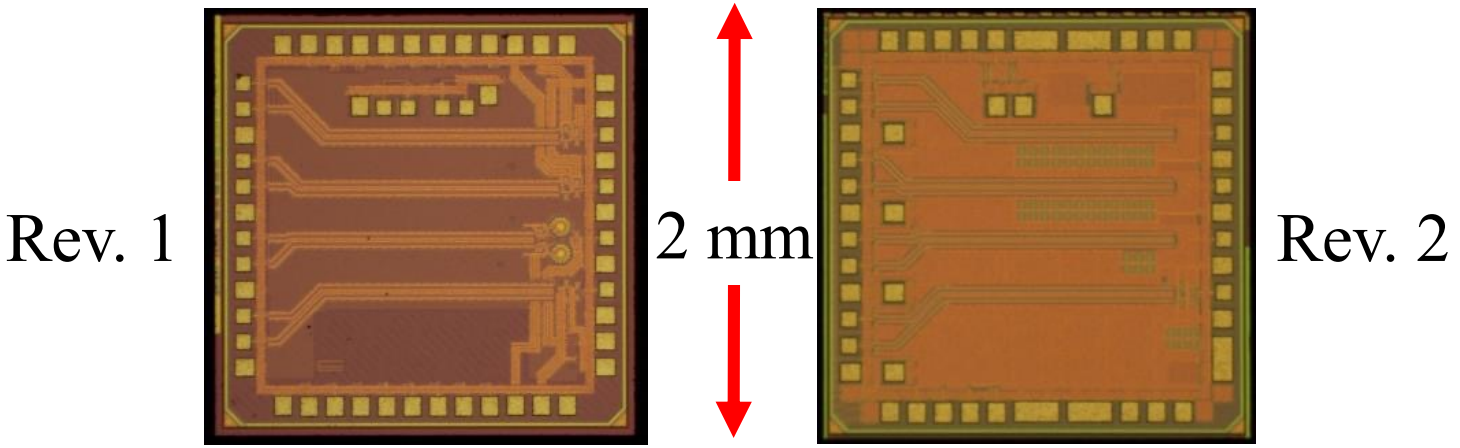




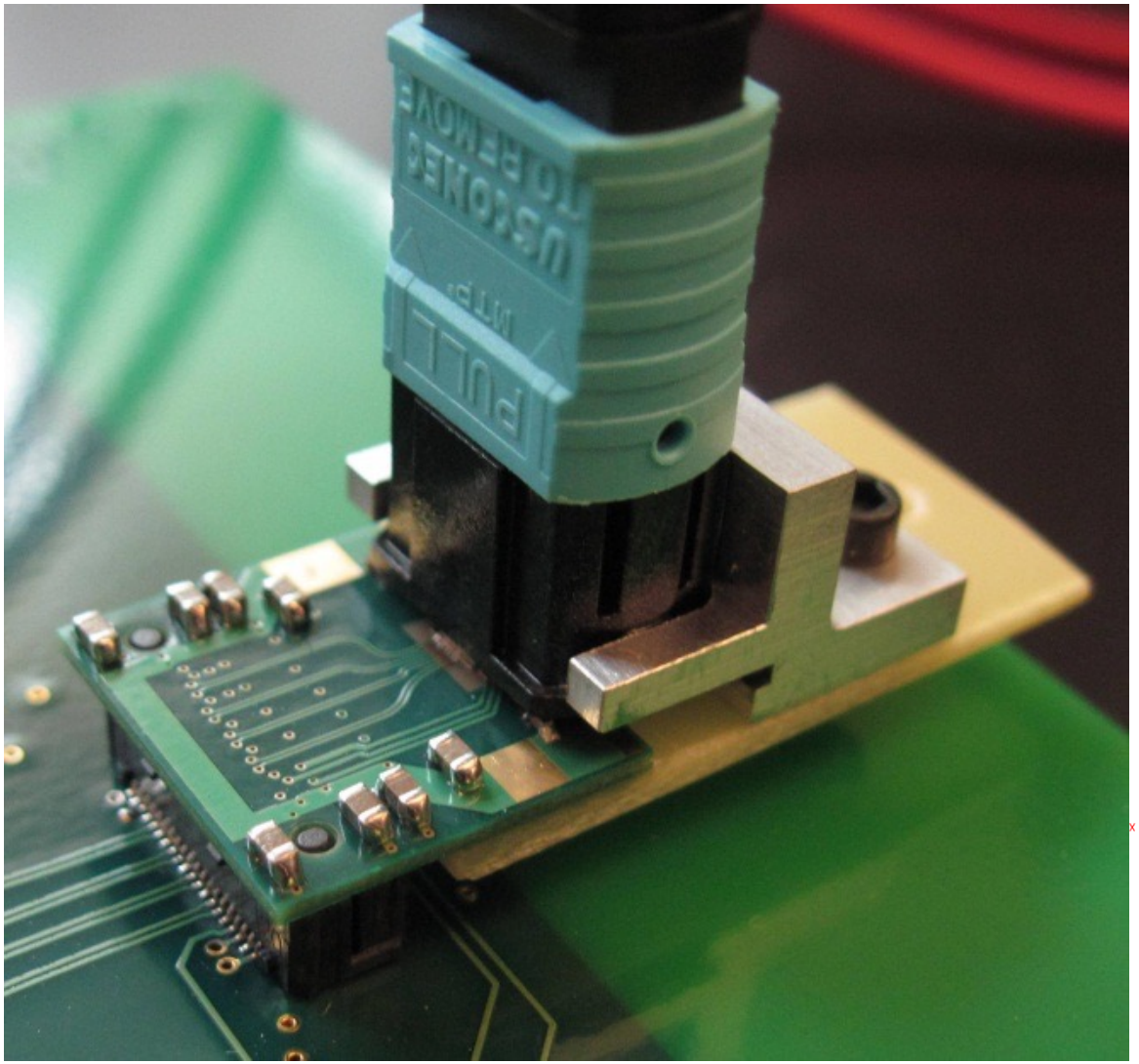
- Proposed opto-pack for ITK-Pixel has simpler design
  - continue to use BeO as substrate for heat management
- experience in building large quantity of opto-packs
  - fabricated 1,200 opto-packs for pixel opto-boards
  - fabricating 300+300 PIN opto-packs for off-detector opto-receivers
  - equivalent to 21,600 channels

10 Gb/s VCSEL Array Driver

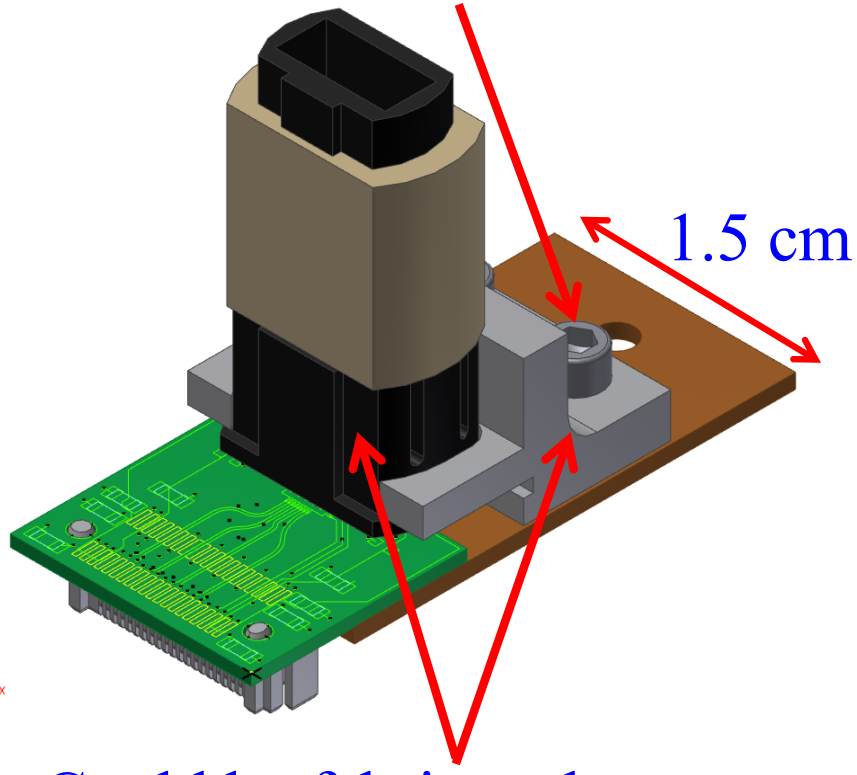
- R&D funded via CDRD program (FY13-15) of DOE (USA)
- Fabricated 4-channel test chips in 65 nm CMOS
- Uses only core transistors to achieve maximum radiation-hardness
- 8-bit DACs to set the VCSEL modulation and bias currents
  - DAC settings stored in SEU tolerant registers



ITK-Pixel Opto-Board



Connector secured to opto-board with screws instead of epoxy in current opto-board



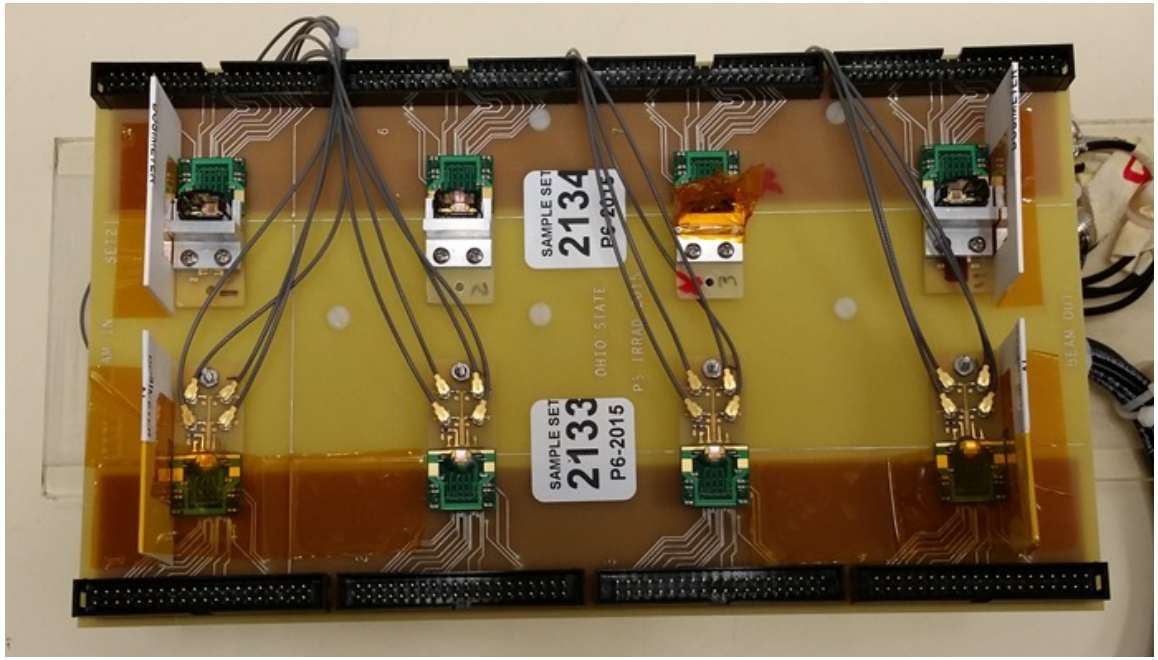
Could be fabricated as one piece with mold injection

Opto-Board Irradiation

- October 2015: irradiated 8 opto-boards with Rev. 1 array driver using 24 GeV protons at the CERN PS Irradiation facility
- 4 pcs. optical: driving Finisar VCSEL arrays (V850-2174-002)
  - dose: 13 Mrad
- 4 pcs. electrical: driving resistive load
  - dose: 111 Mrad

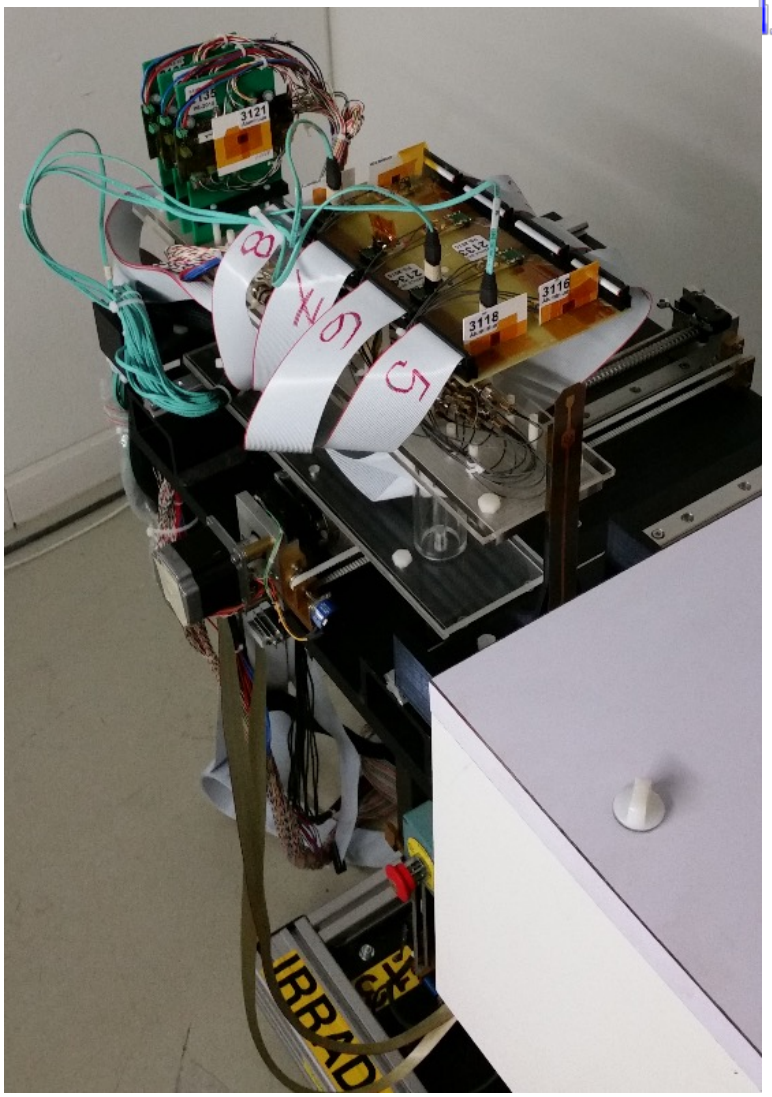
optical

electrical



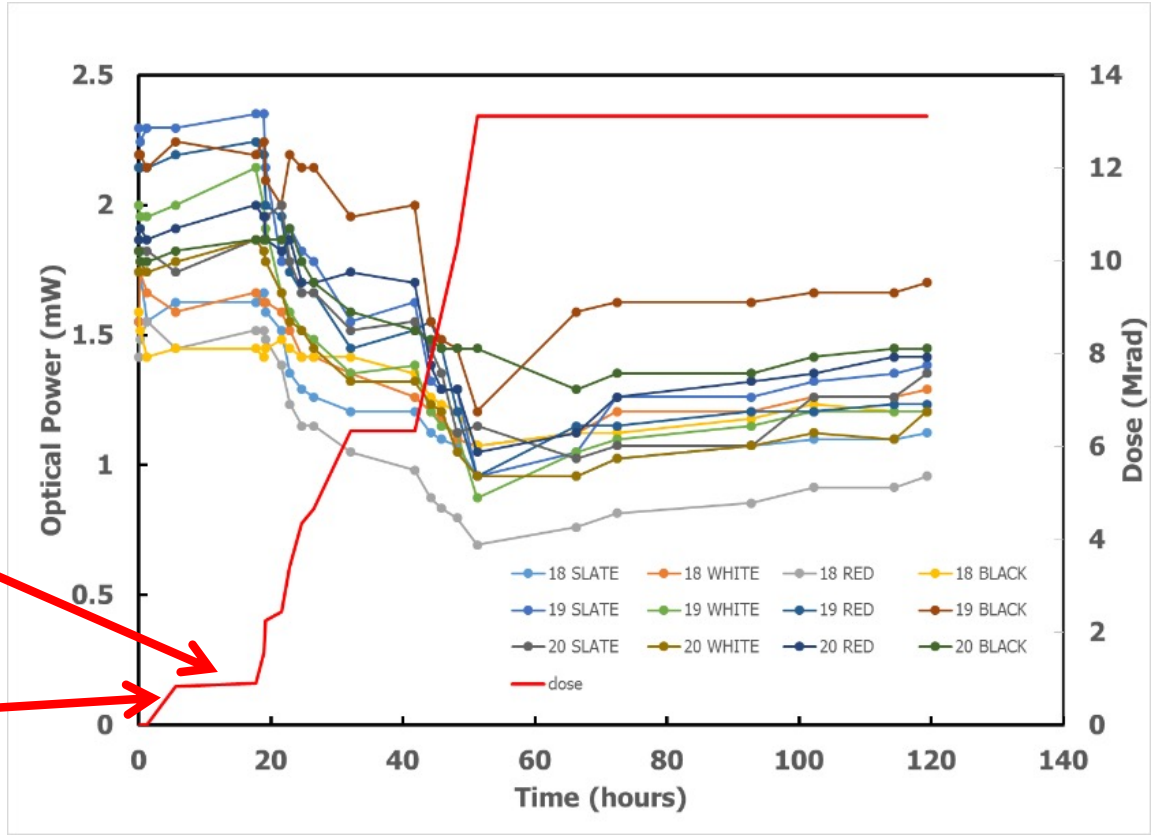
Opto-Board Irradiation

- Chips were powered and monitored during the irradiation at reduced speeds due to the irradiation facility cabling infrastructure
- All channels survived the irradiation and the cooled down chips have been returned to our lab for a study of their performance at high bit rates



VCSEL Optical Power vs. Dose

- Optical power of irradiated VCSELs decreased with dose as expected
- Annealing occurred (slowly) during times when the VCSELs were removed from the beam
- Monitored 12 out of the 16 VCSEL channels during irradiation due to limited number of fiber connections

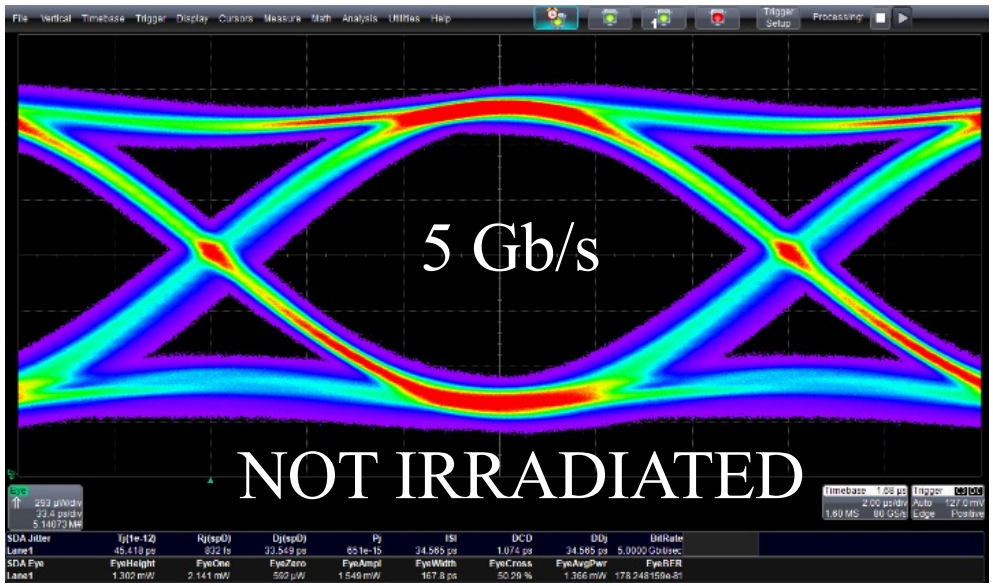


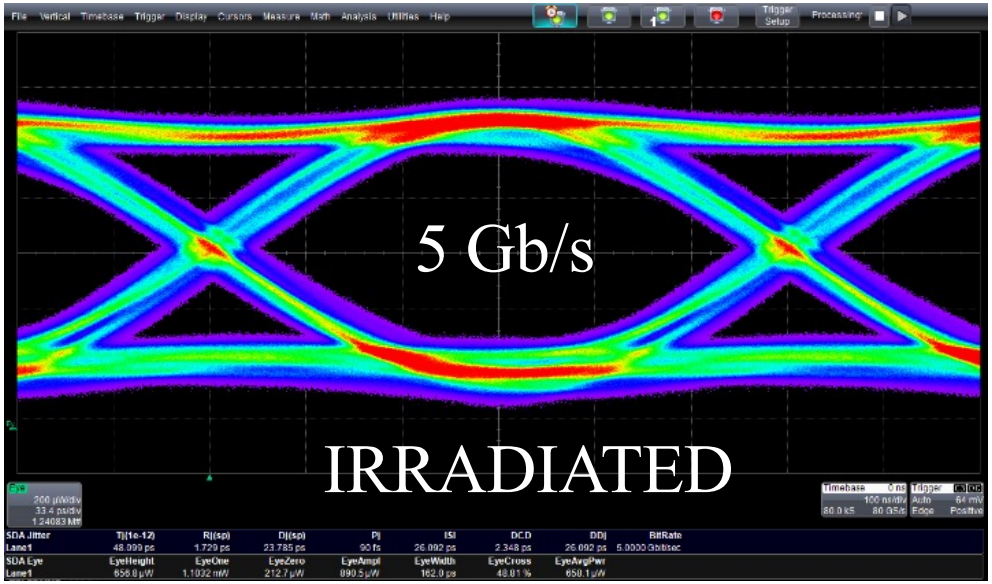
annealing

irradiation

Post Irradiation Results

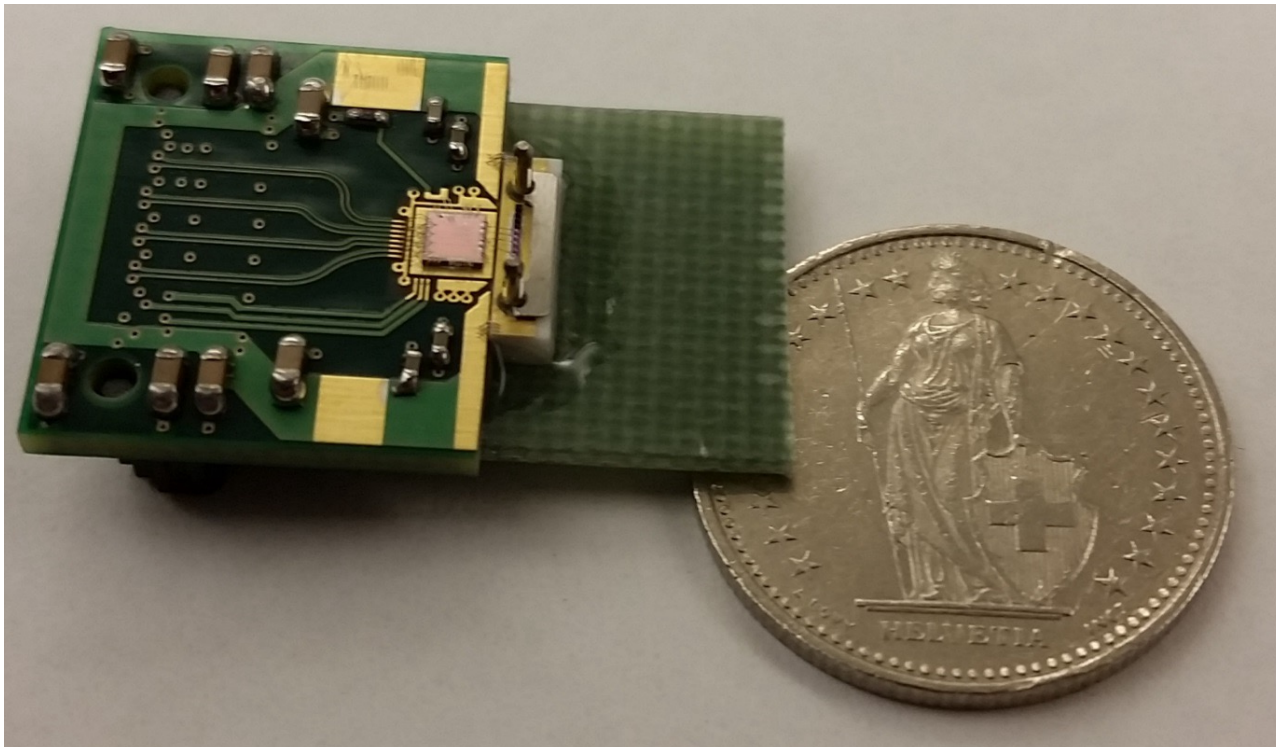
- All channels operational after irradiation
- Optical amplitude reduced from 2.07 mW to 1.19 mW
  - consistent with power loss seen during irradiation
- BER < 5×10^{-14} (run error free for more than 30 minutes)
- First demonstration of radiation hardness of an array driver/VCSEL combination at 10 Gb/s with a dose greater than 10 Mrads!





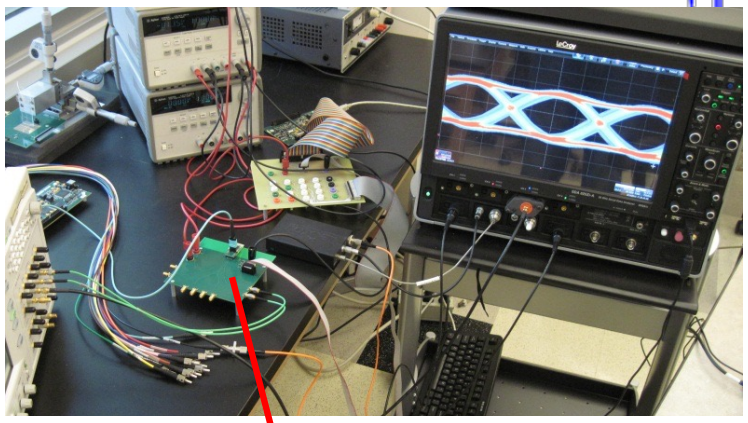
10 Gb/s Array Driver ASIC Rev. 2

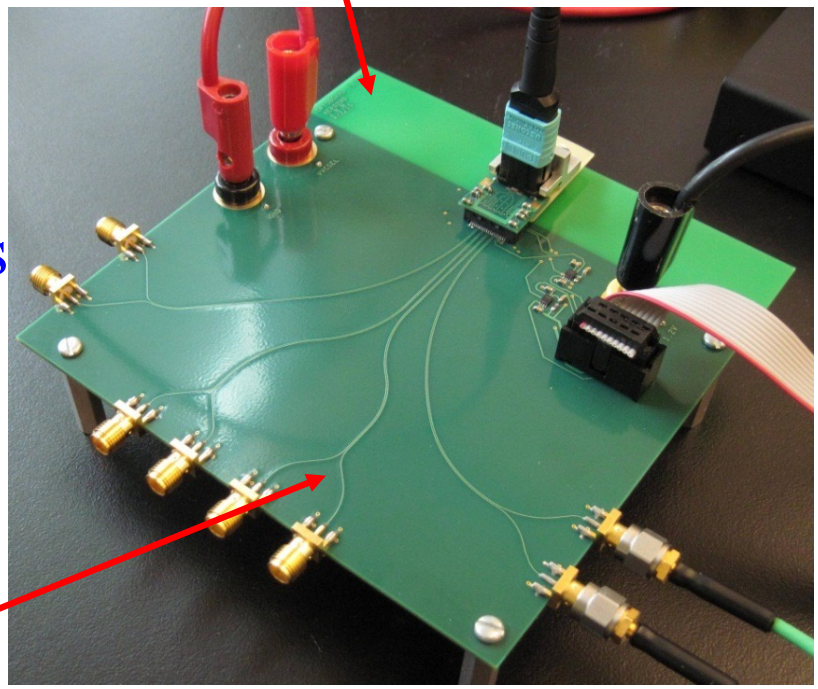
- Rev. 2 has improved architecture for the first three channels, including programmable pre-emphasis current and delay
- One channel was simply a copy of the old design to check for consistency between the versions
- Rev. 2 ASIC is much easier to tune for operation at 10 Gb/s



10 Gb/s Array Driver ASIC Rev. 2

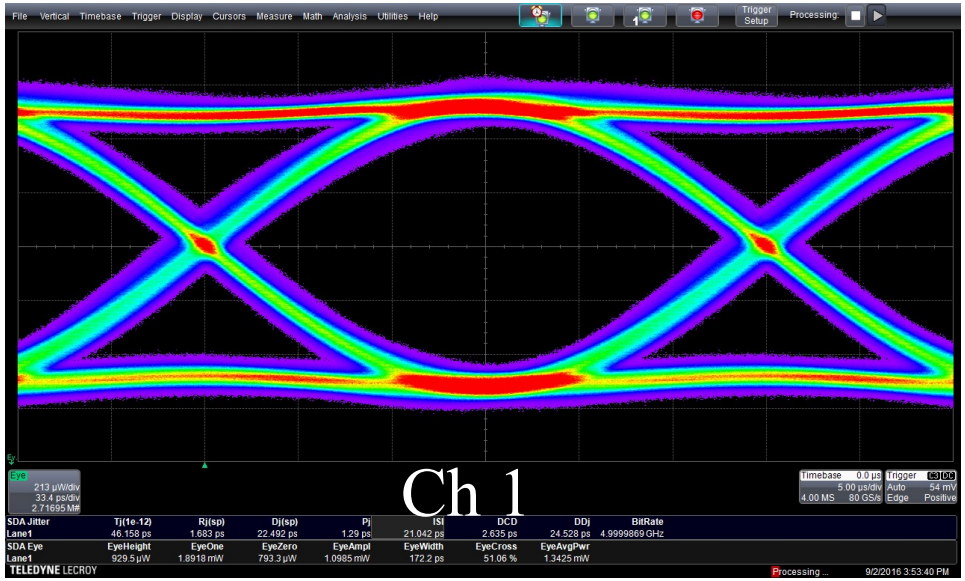
- runs at 1.2 V
  - consumes ~150 mA at 10 Gb/s with all four channels operating
- cathode set to -1.3 V to provide enough headroom to drive the VCSEL
- optical power > 2 mW on all channels
- BER < 5×10^{-14} on all channels at 10 Gb/s with every channel active

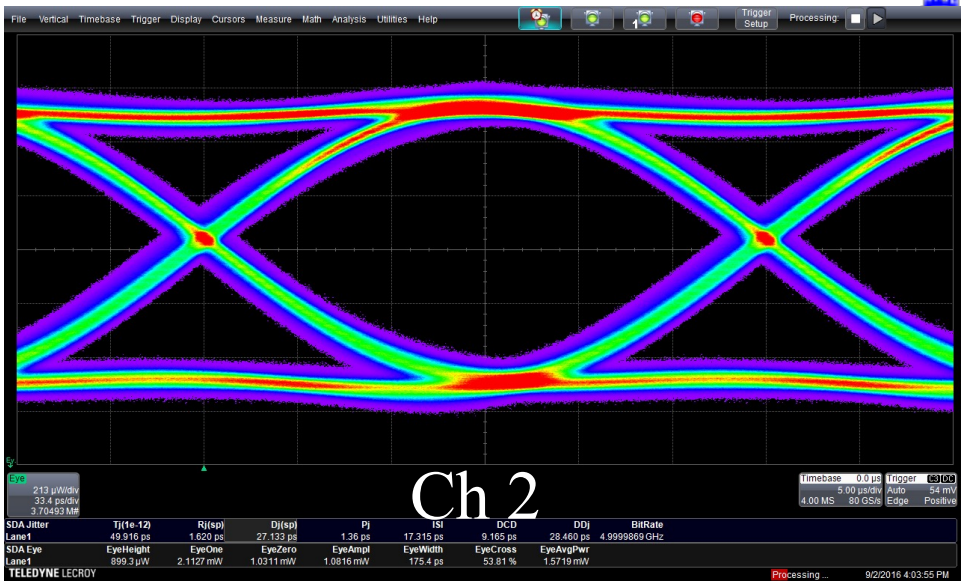


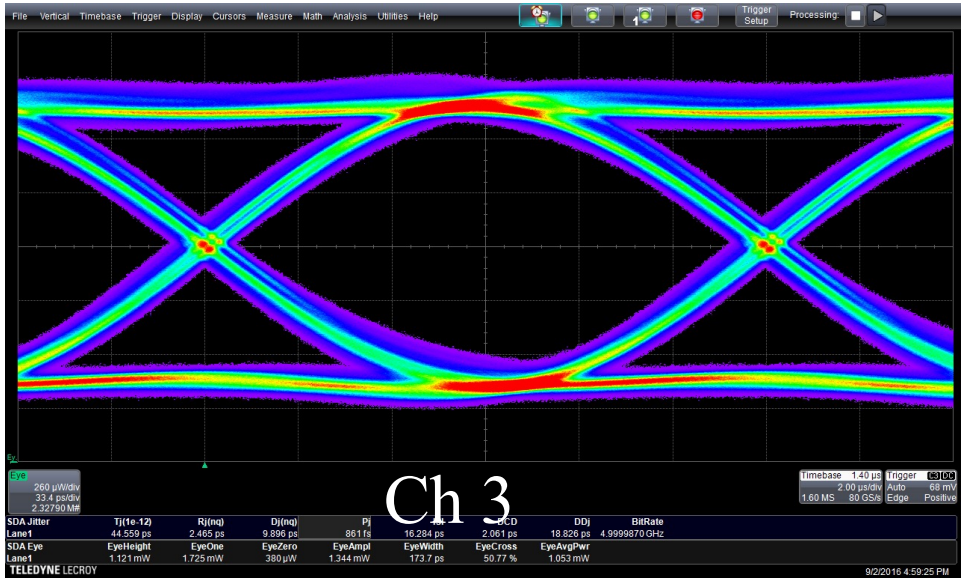


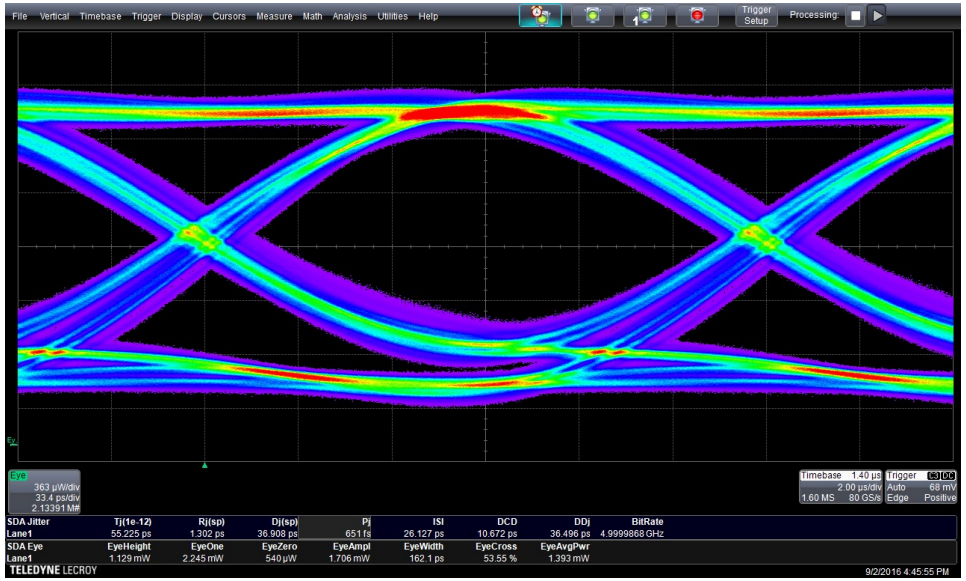
175 μm space/trace controlled impedance transmission lines

Array Driver ASIC Rev. 2: 5 Gb/s









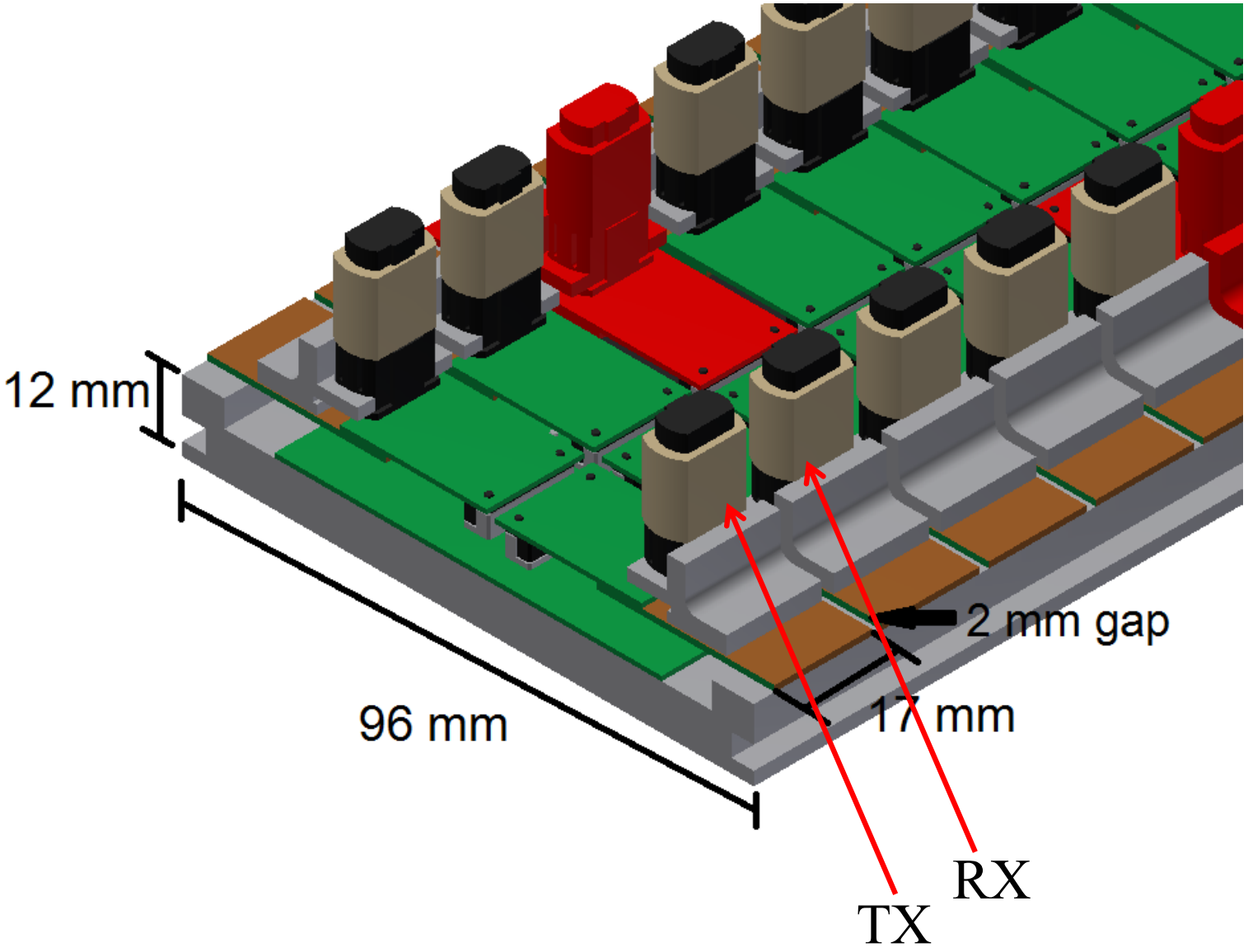
Plan for VCSEL Array Driver ASIC

- new array ASIC to incorporate an array of equalization circuits either from SMU or LBNL
  - will also incorporate any nice features from VL+
- current opto-boards available for data transmission test at cost
- future opto-boards (2018) will be available for free

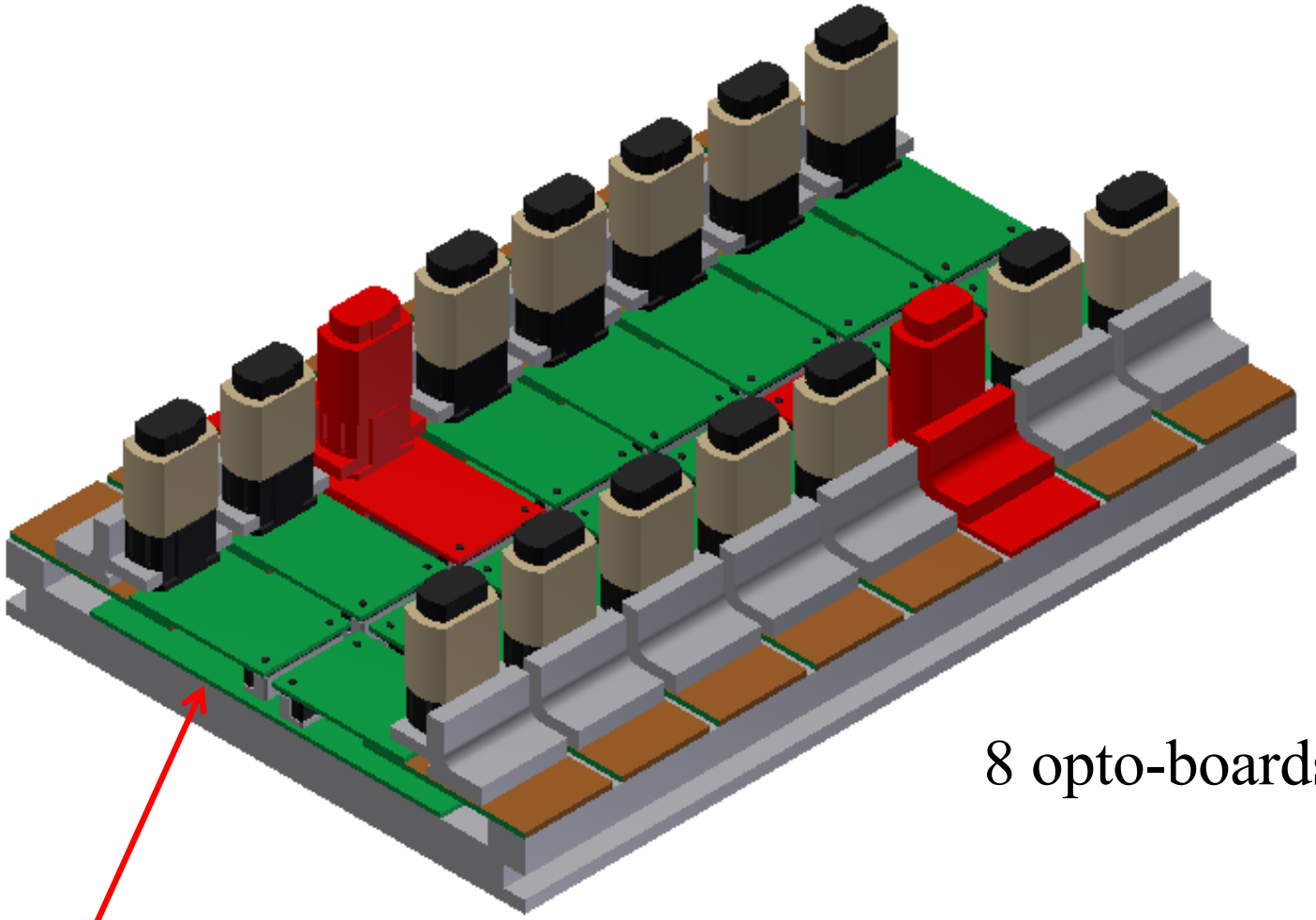
Plan for Receiver Opto-Board

- Basic assumptions:
  - up-links:
    - use 12-channel VCSEL array operating at 5 Gb/s
  - down-links:
    - layout lpGBT/VL receiver (2.5 Gb/s) in 12-channel array
    - use lpGBT to de-serialize signal from each channel into multiple 160 Mb/s signals for transmission to modules
    - locate lpGBT at opto-box to avoid disabling up to 64 modules in a single point failure
      - 160 Mb/s signals needed to control opto-boards
      - less material (ASIC/cooling/power) in central tracking region
      - radiation level at EOS for inner layers too high for lpGBT
  - one down-link opto-board for every seven up-link opto-boards

Opto-Box



Opto-Box



8 opto-boards per side

Back-plane for 2 x 8 lpGBT

Summary

- performance of transmitter opto-board is satisfactory
  - plan to incorporate equalization array into driver ASIC
- plan to layout lpGBT/VL receiver in 12-channel array for the receiver opto-board