Radiation-Hard ASICs for Optical Data Transmission in the First Phase of the LHC Upgrade

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Oct 27, 2011

Outline

- Introduction
- Results on 12-channel Opto-Receiver with Redundancy
- Design of 12-channel Opto-Driver with Redundancy
- Summary

Why Optical Data Links?

- Optical data transmission is now preferred over copper wire links:
  - lower mass
  - much higher data transmission rate over long distance (80 m)
  - break the ground loop between front and back-end electronics
- Optical transmitter: vertical cavity surface-emitting laser (VCSEL)
- Optical receiver: PIN diode
- Optical device can have 1, 4, or 12 channels

Array Optical Links: Today

- array solution has three major advantages:
  - compact: more channels in less space
  - robust: 12-fiber ribbon is stronger than an individual fiber
  - efficient: can reserve 1 in 12 channels for redundancy instead doubling the number of channels
- 120 Gb/s VCSEL/PIN array based links are now commercial standard
  - 12-fiber ribbon, 12 channel VCSEL/PIN array, 10 Gb/s each
- 12-channel array VCSEL and PIN are available from several vendors
  - enabled fabrication of only 272 array-based opto-modules instead of 1,744 single-link opto-modules for ATLAS Pixel detector

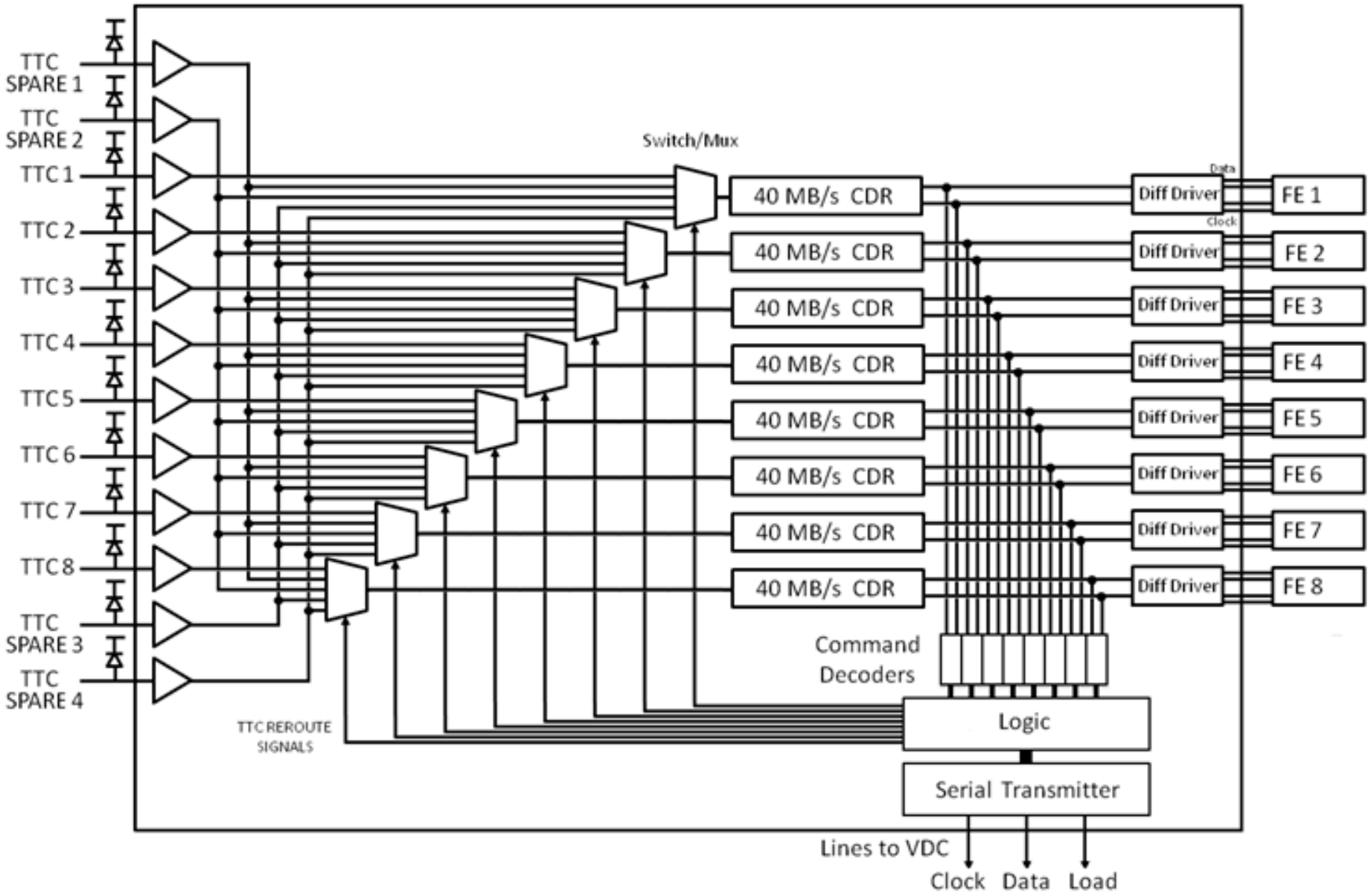
Driver/Receiver with Redundancy

- designed an updated version of VCSEL driver and PIN receiver of current ATLAS Pixel detector but with redundancy
  - possible applications include current ATLAS pixel detector and its upgrade, IBL (Insertable Barrel Layer), in 2013-4
  - experience gained from the development/testing of such new chips would help the development of on-detector array-based opto-links for HL-LHC
  - submission of 12-channel prototype chips (130 nm CMOS) in May

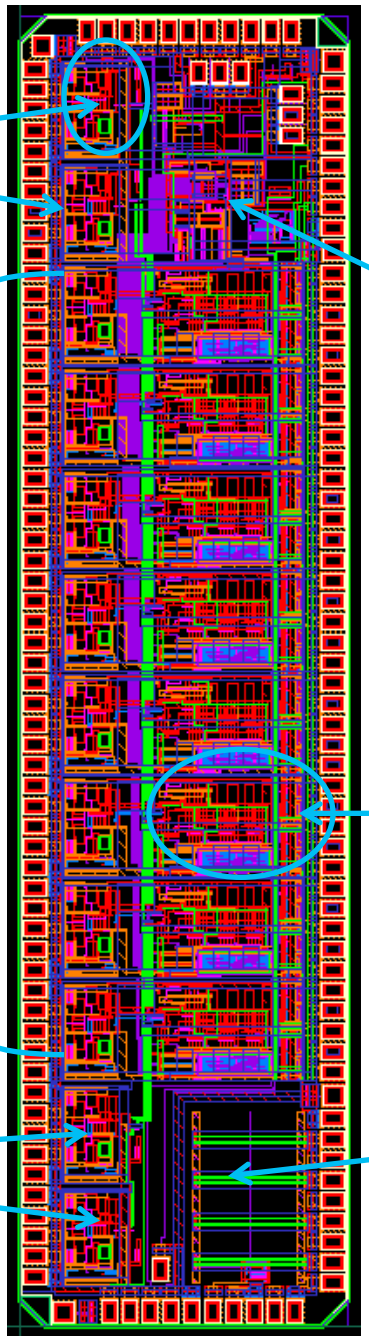
PIN Receiver/Decoder

- recover data and clock from 40 Mb/s bi-phase marked (BPM) signal
- 4 spare PIN receivers for redundancy
- 8 FE-I4 command decoders
  - allows remote control by processing commands received by the 8 command decoders
  - command processor acts if a valid command is received on any command decoder
  - allows working control if only 1 PIN channel is still alive
  - if one of the 8 inner PIN diodes fail
    - ⇨ signal from one of the 4 redundant channel amplifier outputs can be steered to the digital portion of the failed channel
  - power-on reset:
    - start chips in default state, no steering of redundant channels

PIN Receiver/Decoder



PIN Receiver/Decoder



Spare
PIN amplifiers

600 μm x 900 μm
voltage regulator
2.5 V ⇨1.5 V

8 X
DORIC

DLL + command decoder
+ LVDS driver

Spare
PIN amplifiers

600 μm x 900 μm
control logic

6.5 mm x 1.6 mm

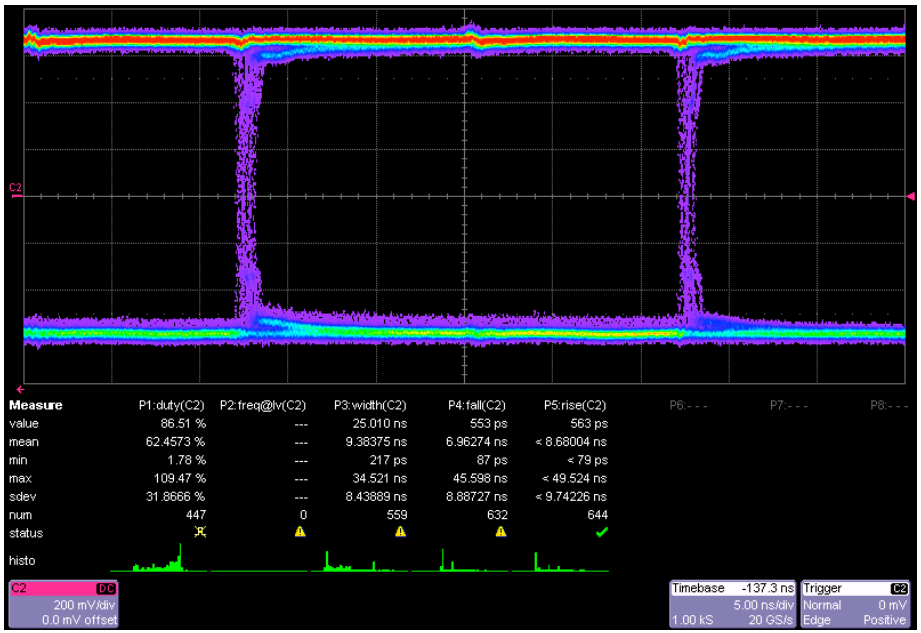
PIN Receiver/Decoder: Results so Far

- ✔ Power on reset circuit works:
  - channels not steered during power up
- ✔ Can steer from one (broken) channel to another (spare)
- ✔ New Bonn LVDS driver works well
  - can set LVDS output drive current
- ✔ Can generate proper serial streams for control of VDC

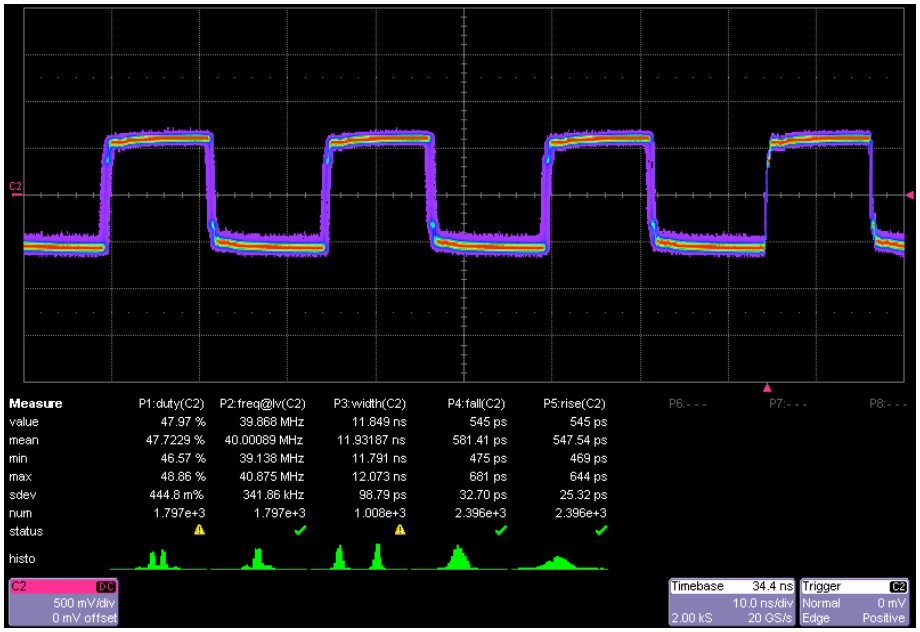
LVDS Driver

- Data eye shows rise/fall time ~0.5 ns

Data



Clock

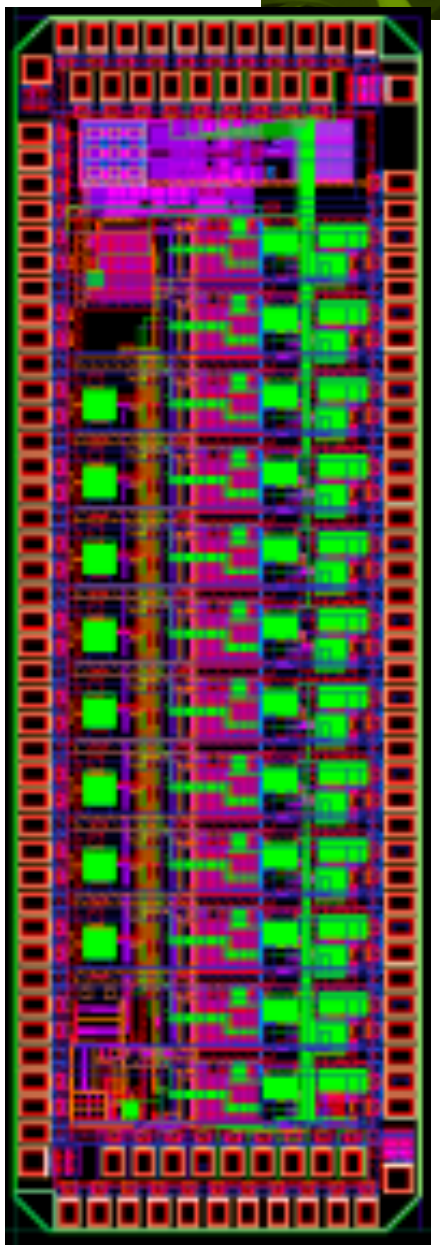


PIN Current Threshold for No BIT Errors

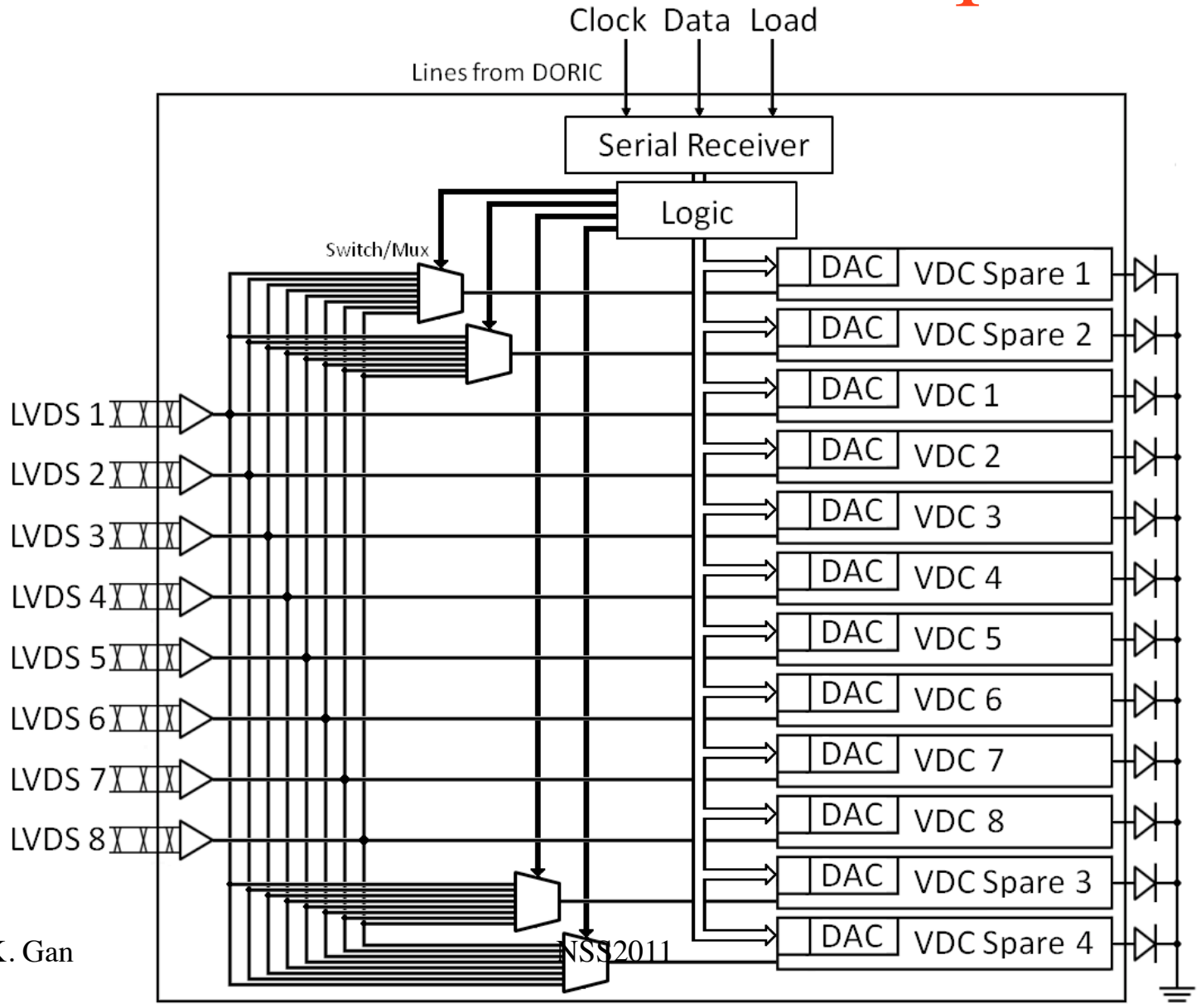
- Threshold (amplitude) for no bit errors:
  - expect to operate at 100 μA to minimize single event upset from traversing charged particle
  - < 20 μA for single channel active
  - 40-60 μA for all channels active with or without spares channels being steered over full length of chip
    - long lead connecting PIN diode?
    - problems with the supply routing/decoupling on the test card?

VCSEL Driver Chip

- Designed for 8 channel operation up to 5 Gb/s
- 4 spare VCSEL driver outputs
- Receives serial data from PIN receiver/decoder (command decoder) for configuration
- If one of the 8 inner VCSELs fail
  - ⇨ the data signal from the detector can be steered to any of the spare VCSELs
- 8-bit DAC for remote control of individual VCSEL bias and modulation current
- Power-on reset
  - sets VCSEL current to ~10 mA on power up
  - start chips in default state, no signal steering
- Submitted May 2011 – 1.5 mm x 4.5 mm



VCSEL Driver Chip



Voltage Regulator

- VCSEL driver needs 2.5 V but other 130 nm circuits need 1.5 V
  - ⇨ designed a PMOS LDO regulator for 2.5 to 1.5 V conversion
- Used enclosed layout transistors for radiation tolerance
- Output adjustable via an external resistor network
- Capable of delivering 750 mA @ 1.5 V
- Fabricated chip works as simulated
- Measured RMS noise on output: < 100 μV
- Low measured output resistance: 20 mΩ
- Runs at 85°C under full load (750 mA) with no cooling

VCSEL Driver Chip Status

- Delivery of VDC delayed 7 times in three-month period by foundry
  - irradiation of receiver/decoder postponed while waiting for VDC
  - need to wait until next IEEE/NSS to see the results on radiation hardness study of both ASICs

Summary

- 12-channel PIN receiver/decoder chip with redundancy and other improvements works well
- awaiting delivery of 12-channel VCSEL driver chip with redundancy
- Radiation hardness study postponed until next Spring