Prototype Opto Chip Results

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Outline

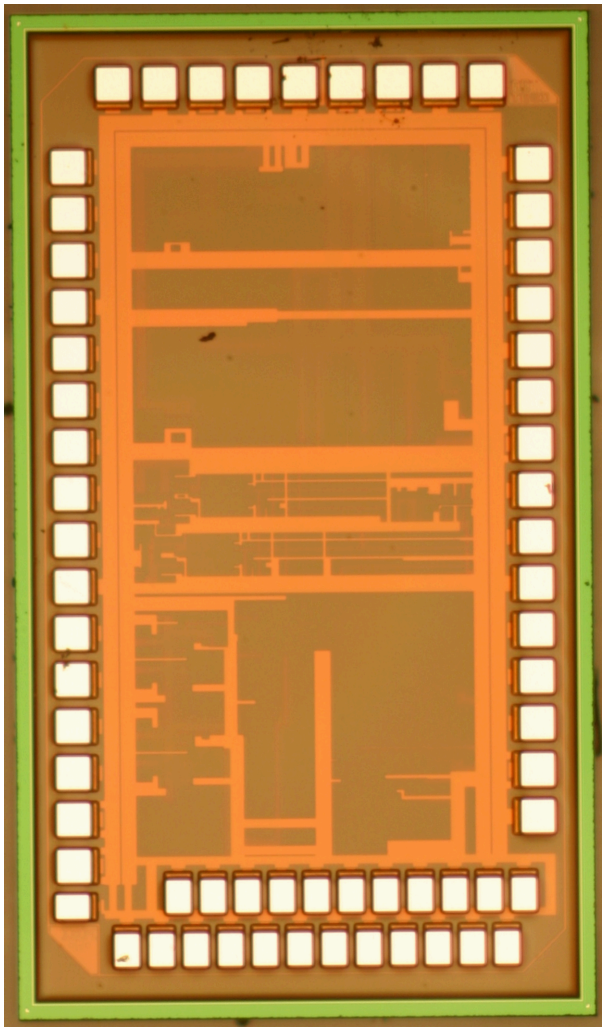
- Introduction
- VCSEL driver chip
- PIN receiver/decoder chip
- Clock multiplier
- Summary

Introduction

- Plan for the on-detector opto-link for the IBL:
  - add new functionalities to correct for deficiencies in current system
  - upgrade current optical chips to run at higher speed
  - some of the development could be of interest to SLHC upgrade
  - use IBM 130 nm CMOS 8RF process
  - prototype chips received/irradiated in July/August 2008
  - ⇨ results will be presented below

Opto-Chips

2.6 mm x 1.5 mm

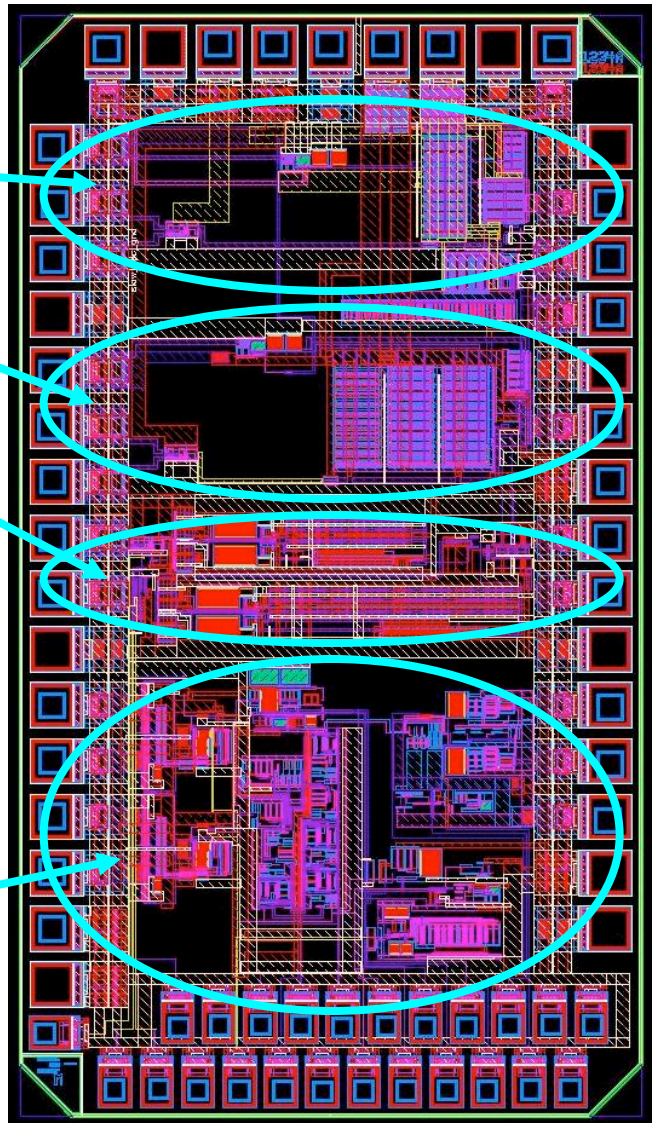


640 Mb/s VCSEL driver

3.2 Gb/s VCSEL driver

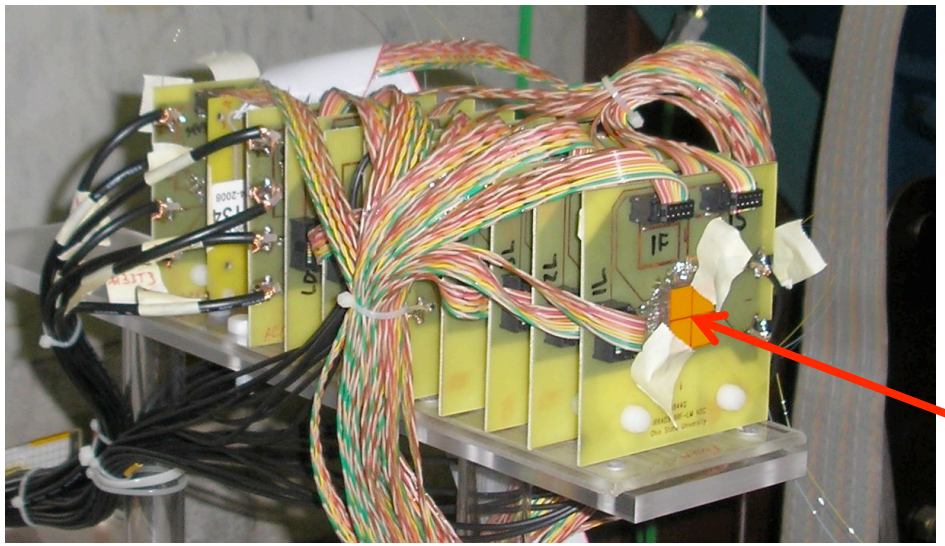
640 MHz clock multipliers
(4 x 160 and 16 x 40 MHz)

PIN receiver/decoder
(40, 160, 320 MHz)

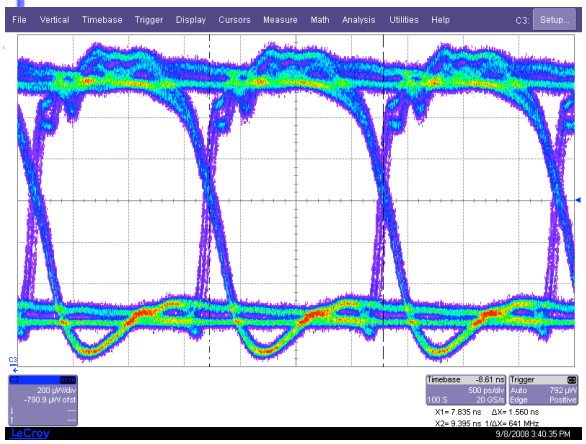


Testing the 130 nm Opto-Chips

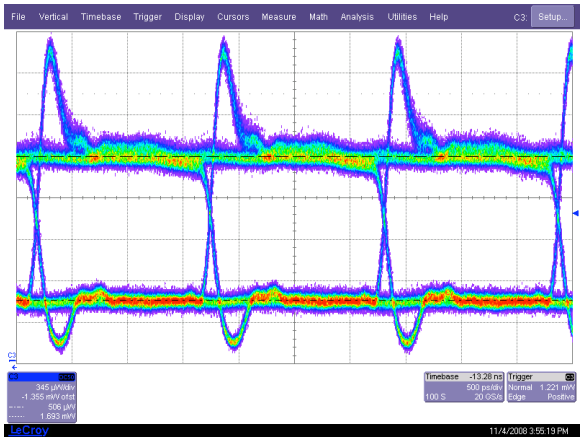
- chips were tested in the lab at Ohio State University
- chips were irradiated with 24 GeV protons to SLHC dose at CERN
  - 8 VCSEL drivers: 4 “slow” + 4 “fast”
  - 4 PIN receiver/decoder (purely electrical testing)
  - 4 PIN receiver/decoder coupled to PIN
  - 4 clock multiplier
  - long cables limited testing of driver/receiver to 40 Mb/s
  - special designed card allows testing of clock multiplier at 640 MHz



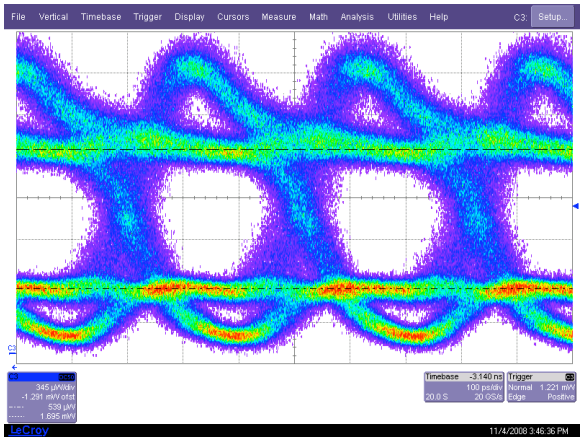
VCSEL Driver Chip



Slow VDC
640 Mb/s
~ 14 mA max



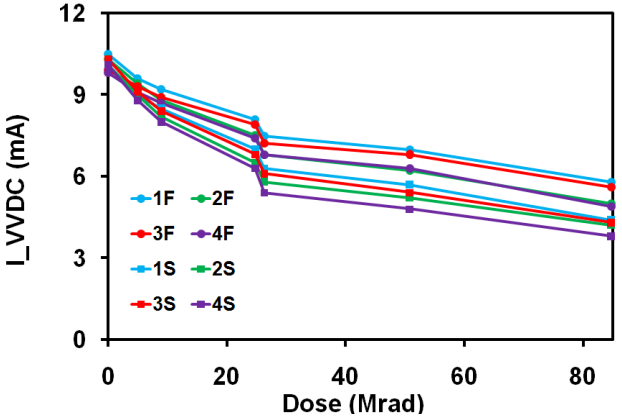
Fast VDC
640 Mb/s
~ 9 mA max

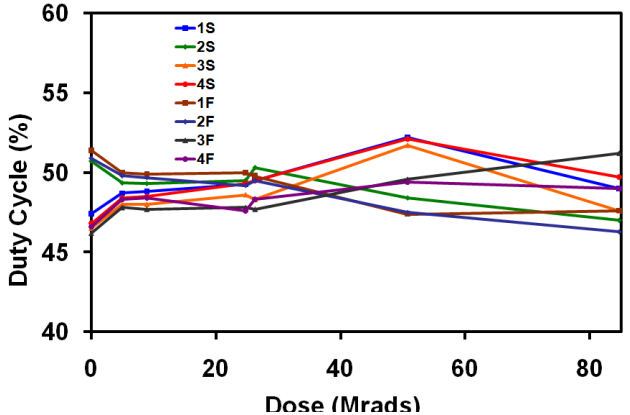


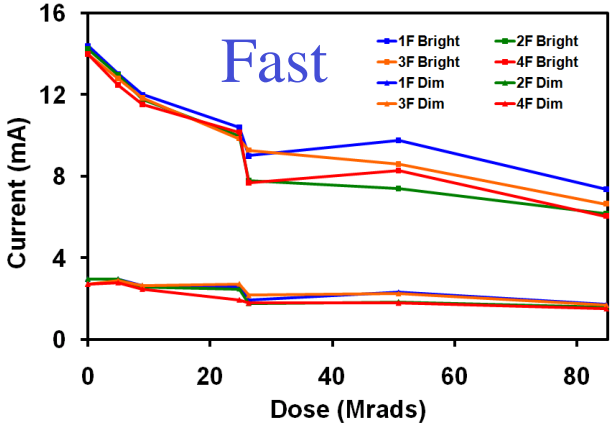
Fast VDC
3.2 Gb/s

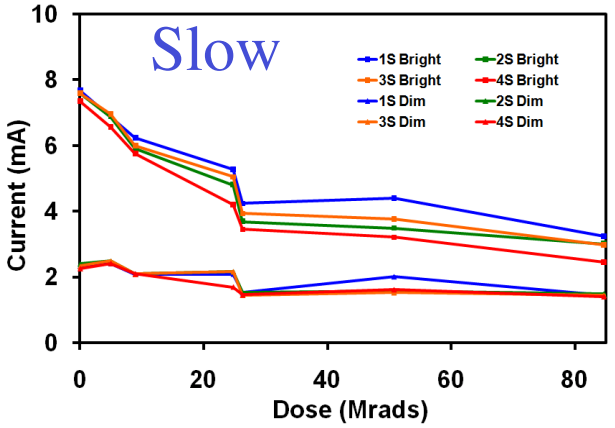
- both slow/fast chips are working
- LVDS receiver/VCSEL driver work at high speed
  - BER < 10^{-13} @ 4 Gb/s using 10 Gb/s AOC VCSEL
- detailed study in progress

VDC Irradiation





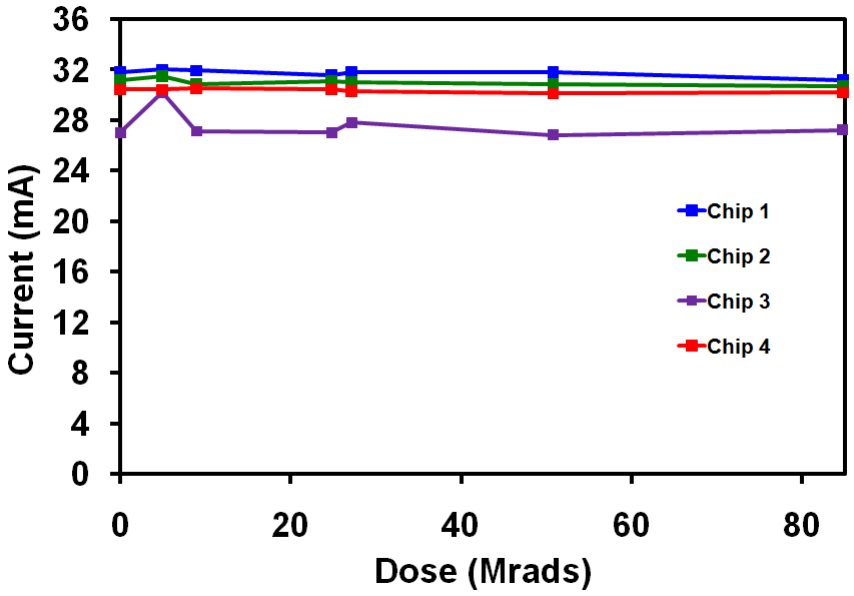




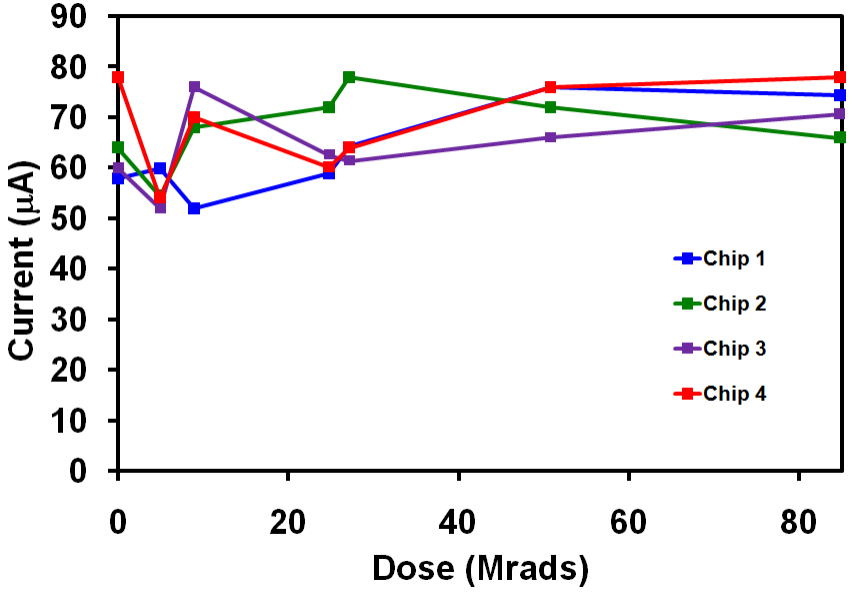
- VDC driving 25 Ω with constant Iset
- drive current decreases with radiation for constant ISET
  - driver circuit fabricated with thick oxide process
- need detailed study after cool down

Receiver/Decoder Chip

- Properly decode 40, 80, and 160 Mb/s BPM signals but the design is for 40, 160, and 320 Mb/s operation
  - LVDS-like output has proper amplitude and baseline
  - small clock jitter, e.g. < 50 ps (1%) @ 160 MHz
  - no significant degradation to SLHC dose

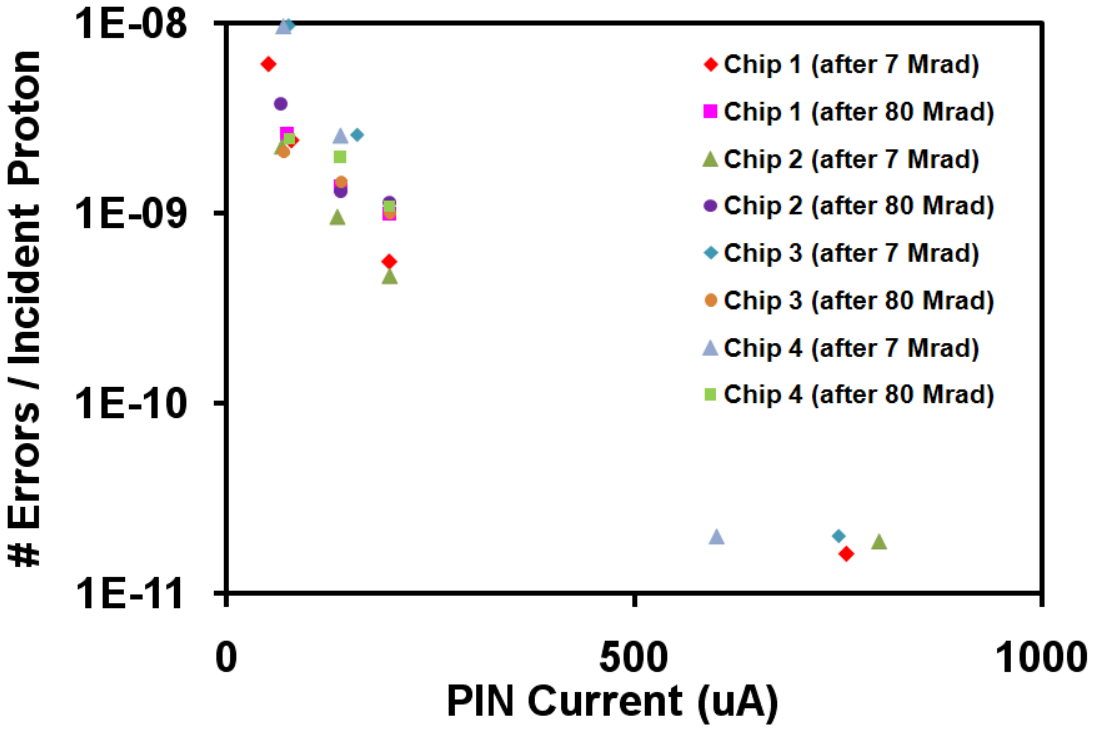


Threshold for 1 bit error/s



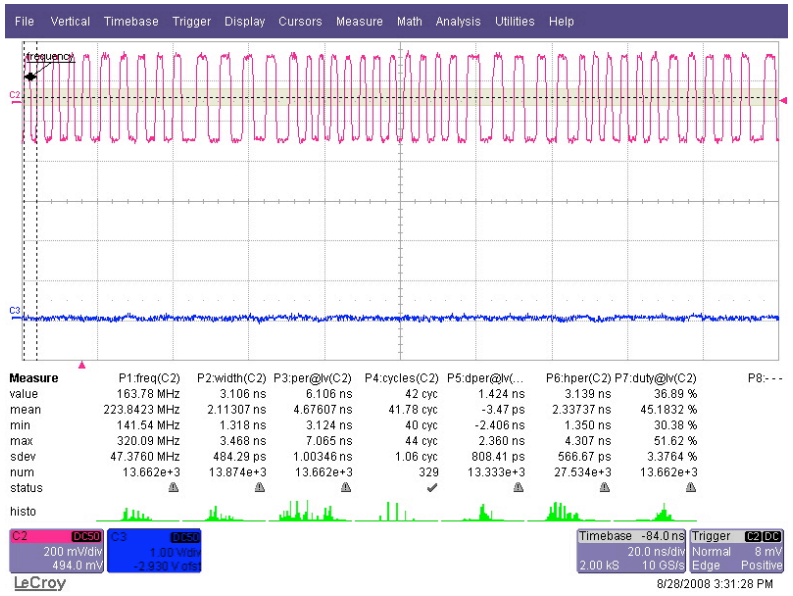
Single Event Upset

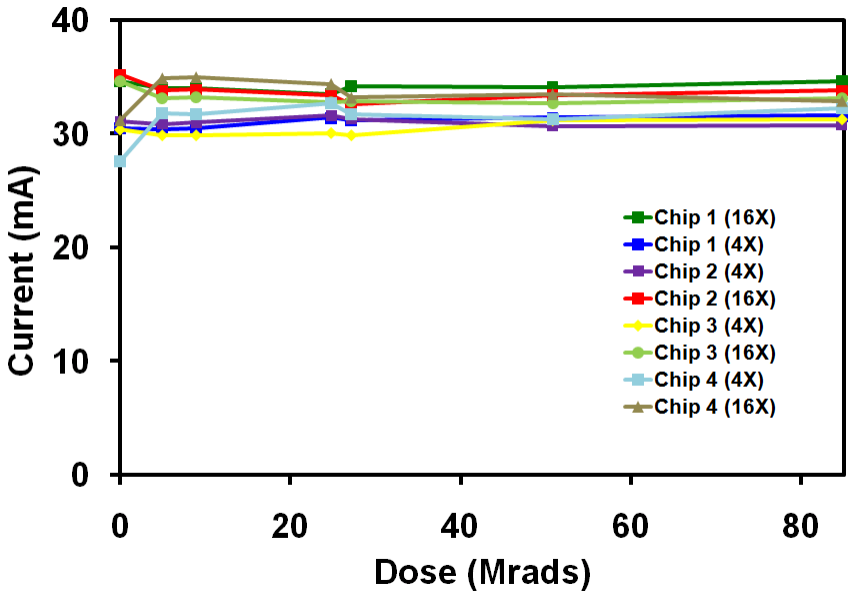
- Single event upset (SEU) measured with receiver/decoder coupled to a Taiwan PIN for 40 Mb/s operation
  - SEU rate much higher with PIN as expected
  - no significant degradation with radiation observed



Clock Multiplier

- clock multiplier needed to serialize high speed data
- Both 4 x 160 MHz and 16 x 40 MHz clock multipliers work
  - clock jitter < 8 ps (0.5%)
  - two of the four chips lost lock during irradiation
    - need power cycling to resume operation at 640 MHz
  - no change in current consumption



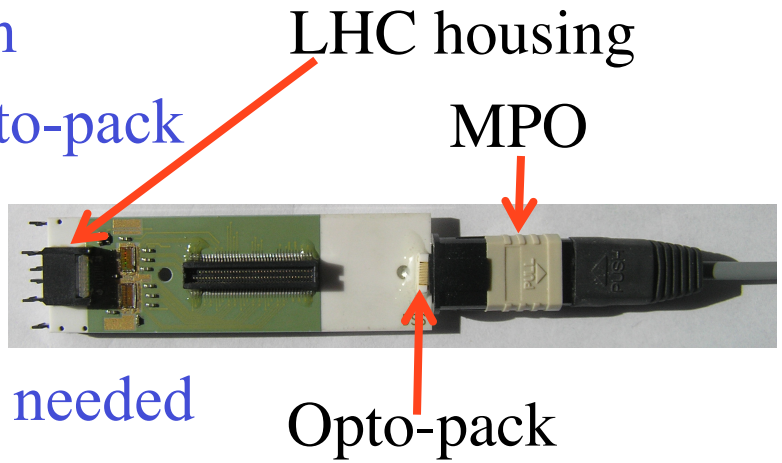


New Opto-Packs?

- Current Taiwan opto-pack has three deficiencies:
  - VCSEL array is mounted on FR4
    - ⇨ poor removal of heat
    - ⇨ poor control of VCSEL temperature
  - difficult soldering of micro leads (250 μm) to BeO board
  - difficult inspection of cold solder
- New BeO based opto-pack has been developed
  - efficient removal of heat
  - good control of VCSEL temperature
  - use wire bonds for connections
  - 55 VCSEL/16 PIN opto-packs have been built for 2006-8 irradiation

New Opto-Pack Housing?

- Current Taiwan opto-pack housing has three deficiencies:
  - two small ears prevent fiber ribbon from dislodging
    - use a needle to pry open the ears for ribbon insertion/removal
    - ears are fragile
    - ribbon is not pushed against the opto-pack
- Replace the housing with a modified MPO connector?
  - more robust commercial design
  - easy to insert and remove fiber ribbon
  - a spring pushes ribbon against the opto-pack
    - use non-magnetic spring
  - need to irradiate MPO connector
    - mold-injection with PEEK may be needed



New VCSEL Array?

- Some Truelight VCSEL arrays developed common serial resistance:
  - not enough voltage to drive a VCSEL array
    - ⇨ low or no optical power
    - problem not well understood
- Recommend using arrays evaluated for SLHC
  - AOC (5 or 10 Gb/s) or Optowell are leading candidates
    - will study later this month devices irradiated in August 2008
  - need long-term reliability study of ~20 irradiated arrays
    - planned in August 2009

New PIN Array?

- Taiwan PIN arrays have long fall time:
  - ⇨ limit operating region of off-detector RX
- Recommend using arrays evaluated for SLHC
  - Optowell and Hamamatsu GaAs arrays are leading candidates
  - Hamamatsu silicon PIN diode is also rad-hard
    - need custom fabrication of custom array if interested
  - will study later this month devices irradiated in August 2008
  - need long-term reliability study of ~20 irradiated devices
    - planned in August 2009

Summary

- First 130 nm submission mostly successful
  - full characterization of pre/post irradiation in progress
  - aim for next iteration in winter 2009 with new functionalities
    - individual control of VCSEL currents
    - redundancy: ability to bypass a bad VCSEL/PIN channel
- New opto-pack developed
- VCSEL/PIN characterized for SLHC are good candidates