Overview of Opto-Link R&D

W. Fernando, K.K. Gan, A. Law, H.P. Kagan, R.D. Kass, J. Moore, A. Rau, S. Smith
The Ohio State University

M.R.M. Lebbai, P.L. Skubic
University of Oklahoma

B. Abi, F. Rizatdinova
Oklahoma State University

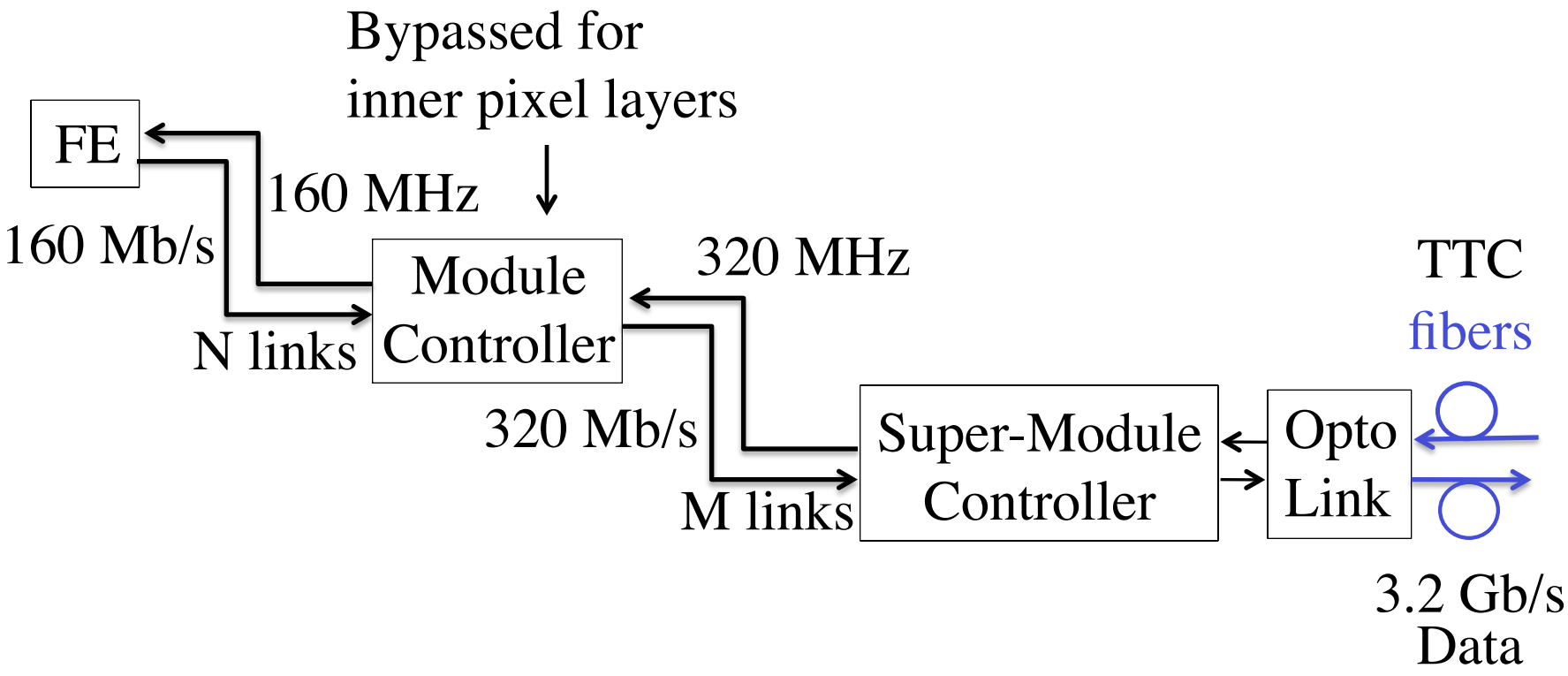
March 11, 2008

Outline

- Architecture
- Transmission on micro-cables
- Bandwidth of fiber
- Radiation hardness of PIN arrays
- Radiation hardness of VCSEL arrays
- Compact MT-style opto-pack
- Plan for opto-chips
- Summary

Read Out Architect

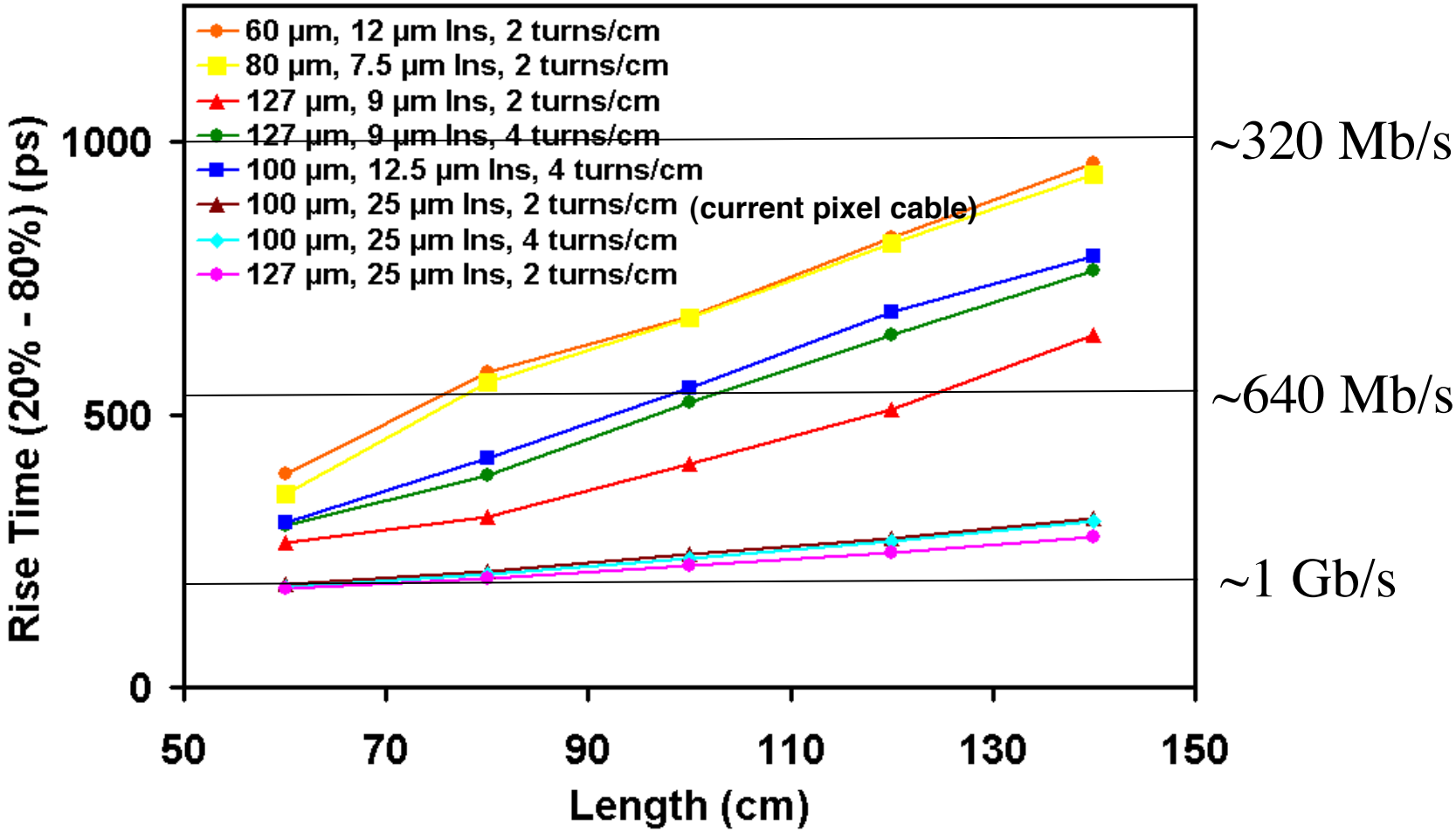
- G. Darbo, P. Farthouat, A. Grillo, ATL-P-EN-0001



Transmission on Micro-Cables

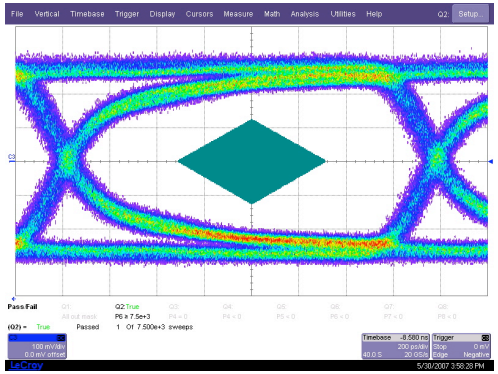
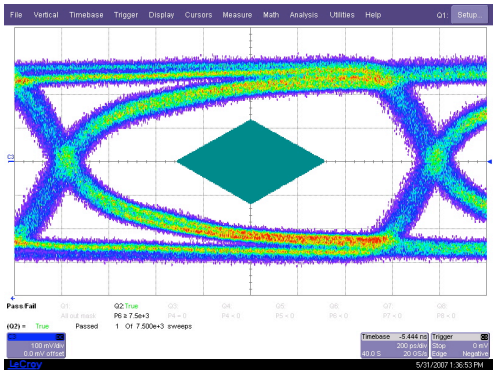
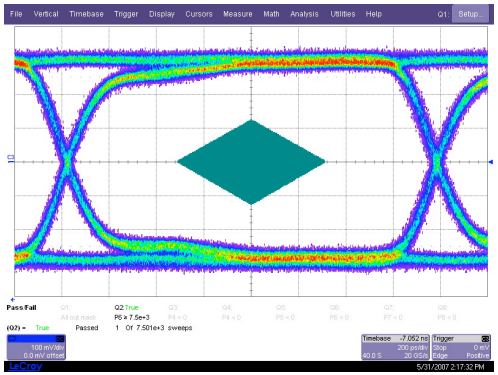
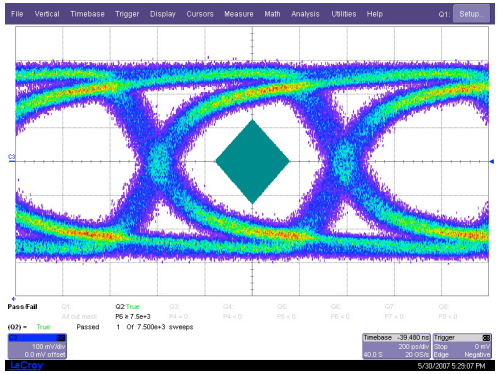
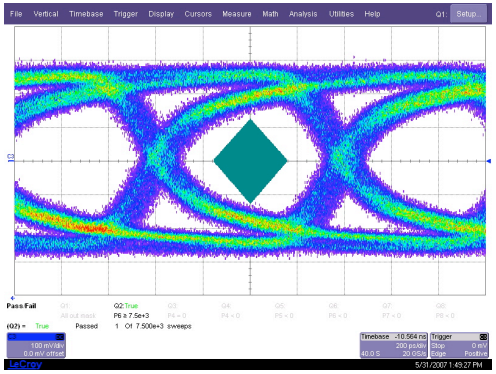
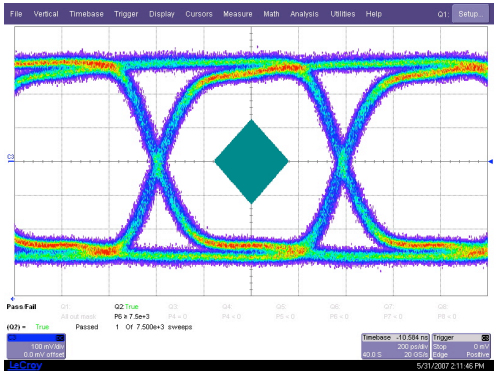
- optical link of current pixel detector is mounted on patch panels:
  - ⇨ much reduced radiation level
- use micro-twisted pairs for transmission between pixel and opto modules
  - ⇨ simplified the design/production of both types of modules
  - ⇨ what is the bandwidth of the micro cables?

Bandwidth of Micro Twisted Pairs



- current pixel cable with thick insulation is quite optimum!

Eye Diagrams

	127 μm cable 140 cm	100 μm current pixel cable 140 cm	100 μm current pixel cable 60 cm
640 Mb/s			
1280 Mb/s			

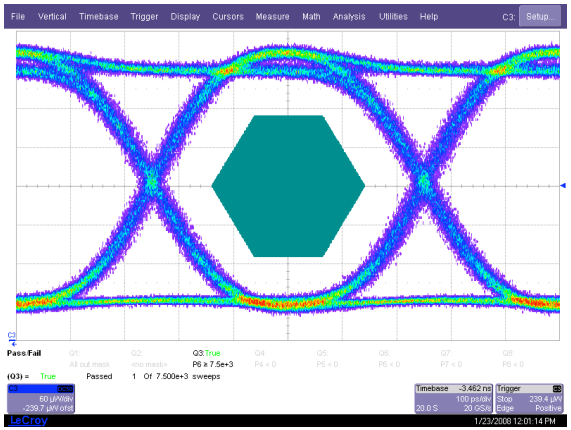
- transmission at 640 Mb/s is adequate
- 127 μm cable is slightly better
- will investigate the use of TRT cable for longer transmission

Bandwidth of Fiber

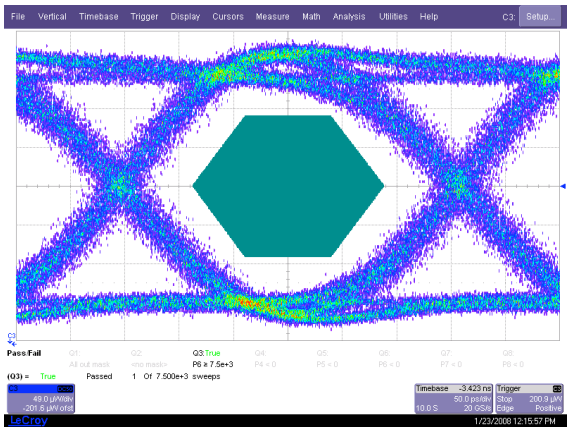
- optical links of current pixel detector use rad-hard/low-bandwidth SIMM fiber fusion spliced to rad-tolerant/medium-bandwidth GRIN fiber
  - ⇨ what is the limit of the bandwidth?

Bandwidth of Fiber

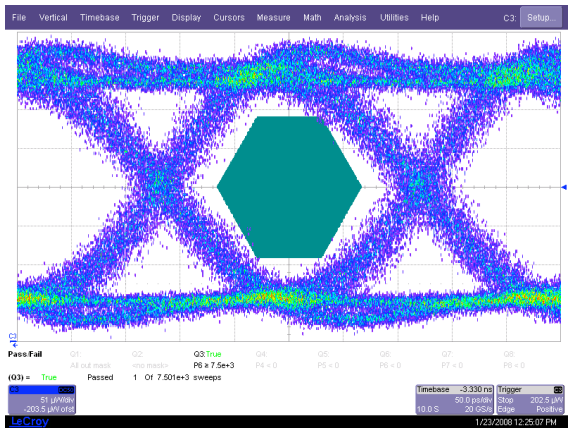
11 + 80 m spliced SIMM/GRIN fiber



2 Gb/s



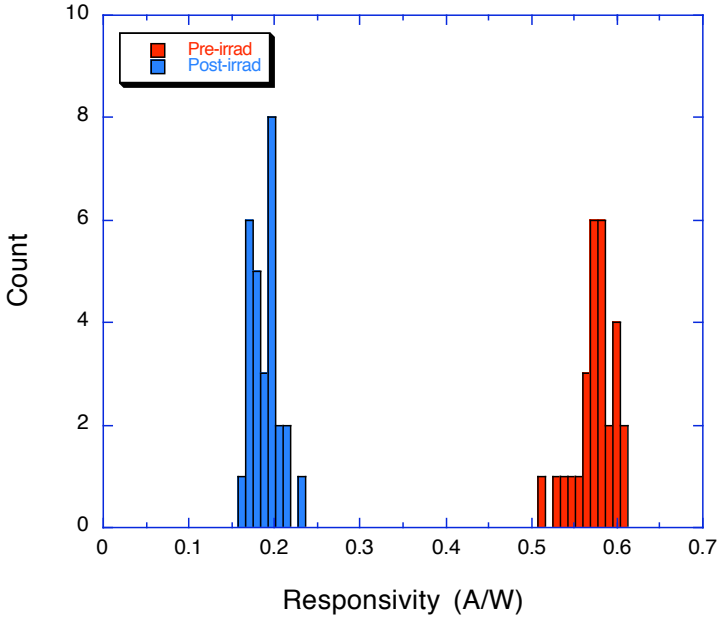
3.2 Gb/s

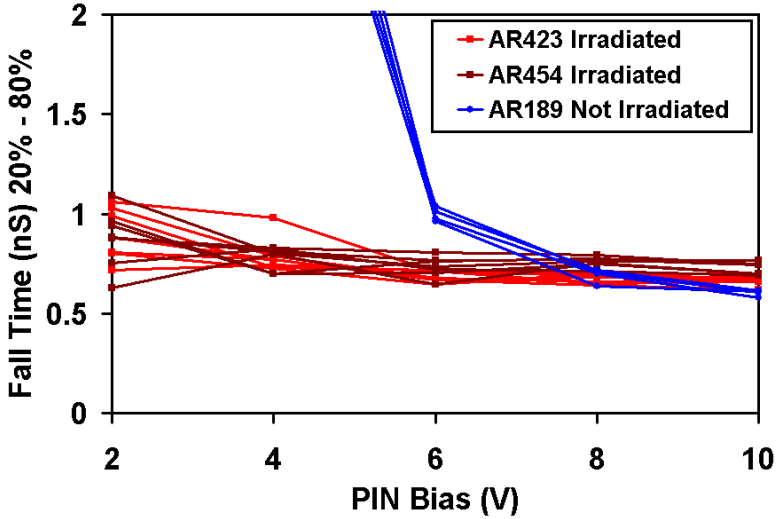


4.25 Gb/s

- transmission at 3.2 Gb/s is adequate
  - ✔ satisfy the requirement of B-layer upgrade
  - ■ current SLHC architecture calls for raw rate of 3.2 Gb/s plus 20% overhead for 8b/10b encoding
  - ⇨ more efficient encoding will improve margin of operation

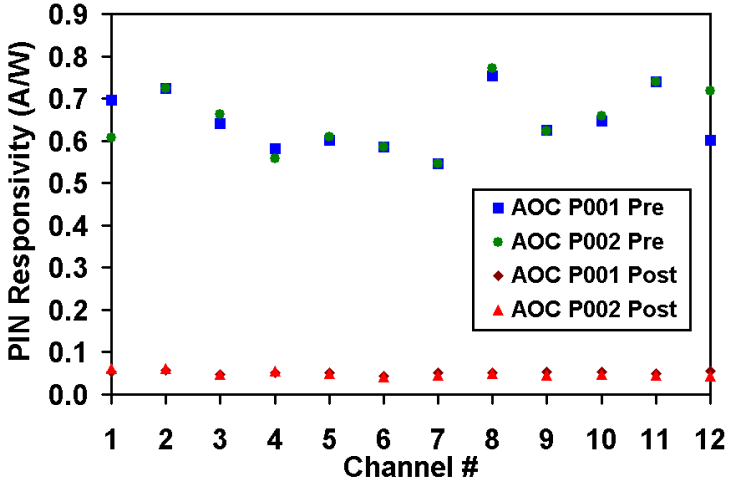
Radiation-Hardness of Silicon PIN

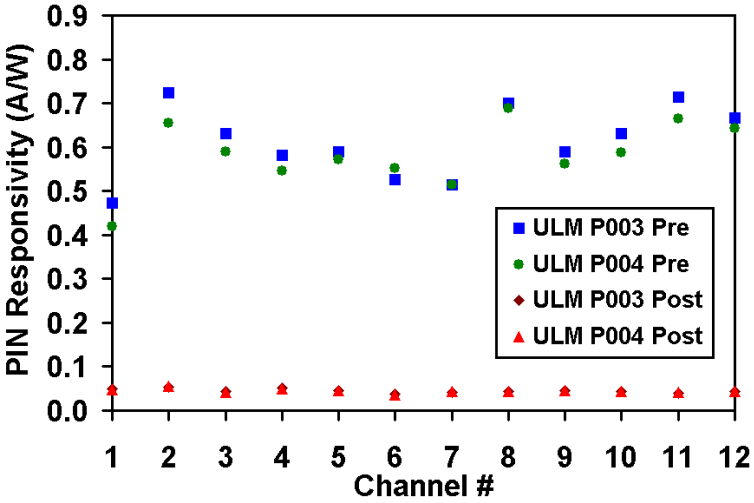


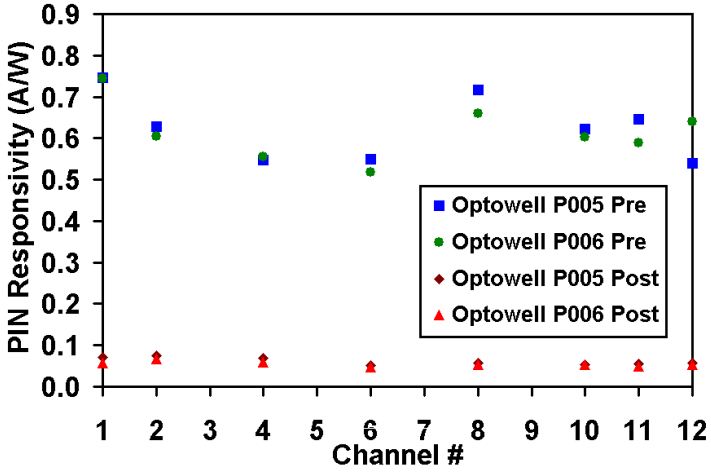


- irradiate PIN/VCSEL arrays with 24 GeV protons at CERN
- PIN responsivity decreases by 3x at 114 Mrad (SLHC: 69 Mrad)
- no degradation of rise/fall time
  - ✔ operation at 160 MHz is OK

Radiation-Hardness of GaAs PIN

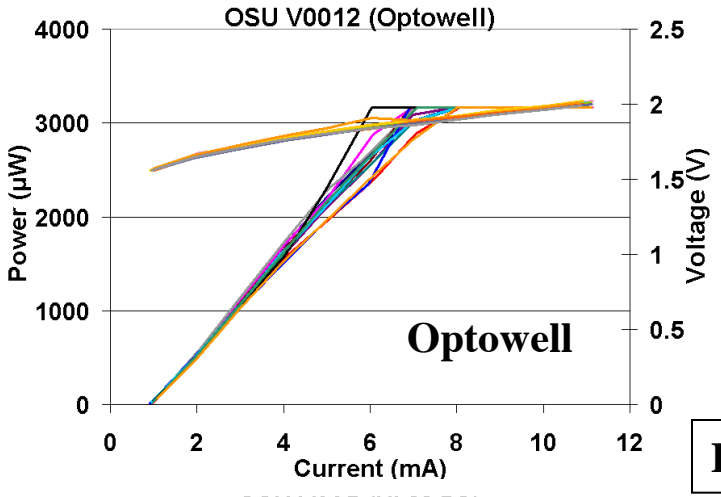




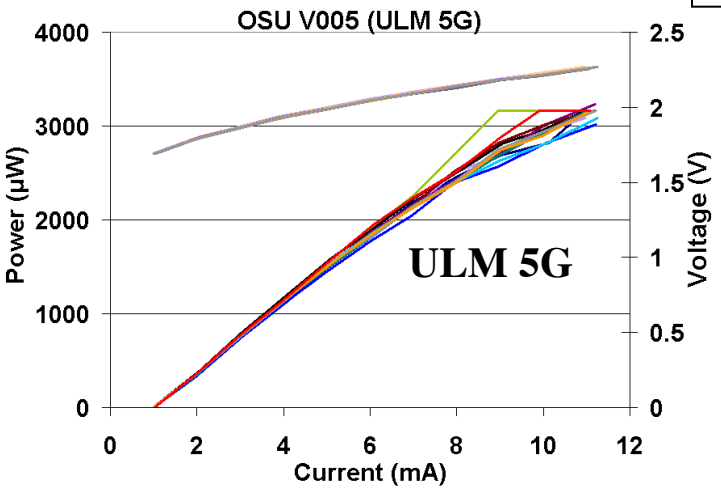


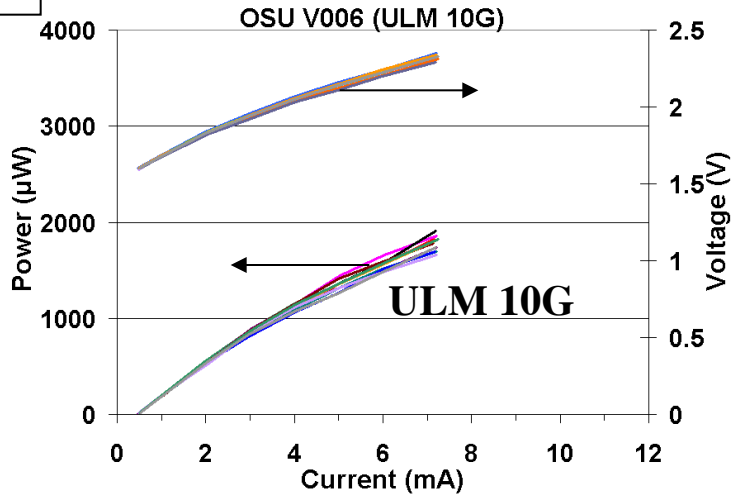
- all arrays are front side illuminated
- PIN responsivities decrease by ~10x at 53 Mrad
- should repeat irradiation to SLHC dosage of 34 Mrad

VCSEL LIV Characteristics



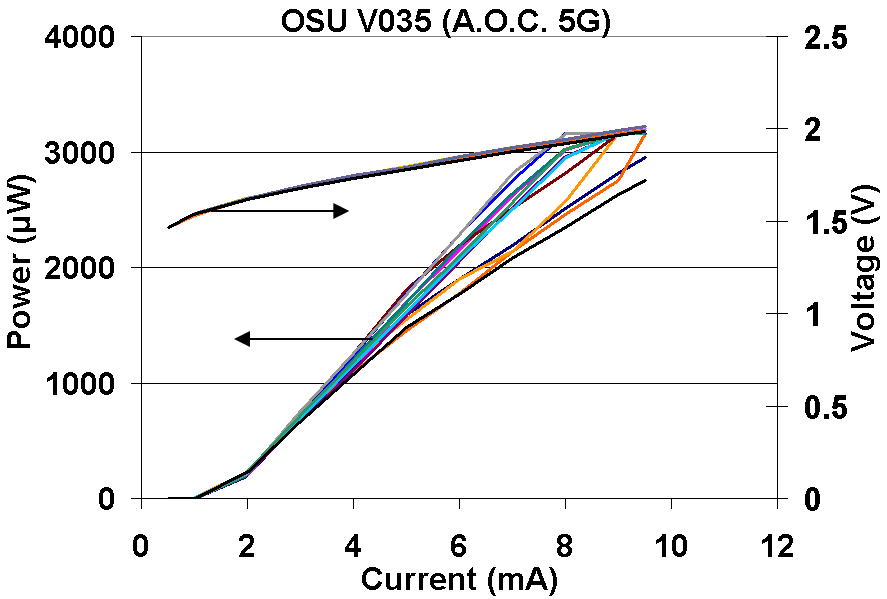
Pre-irrad

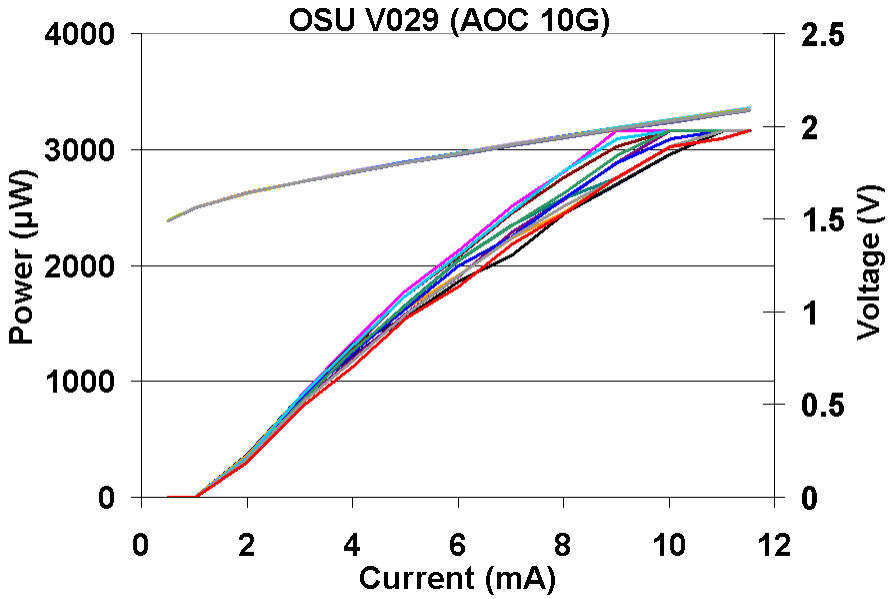




- ☹ ULM requires higher voltage to operate
- ● all arrays have very good optical power

VCSEL LIV Characteristics

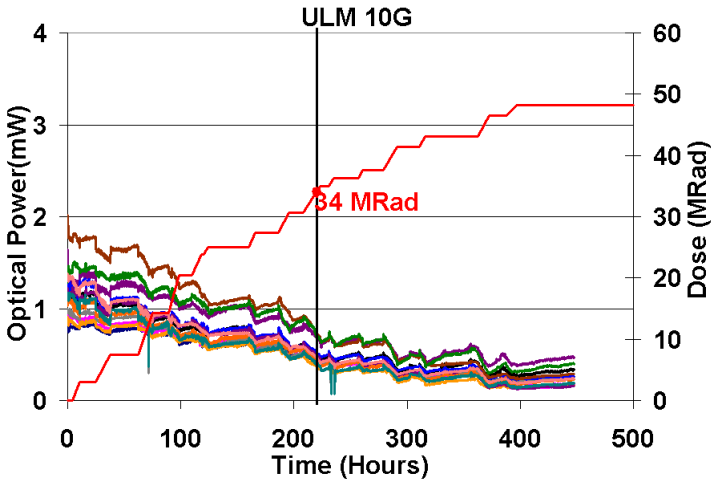


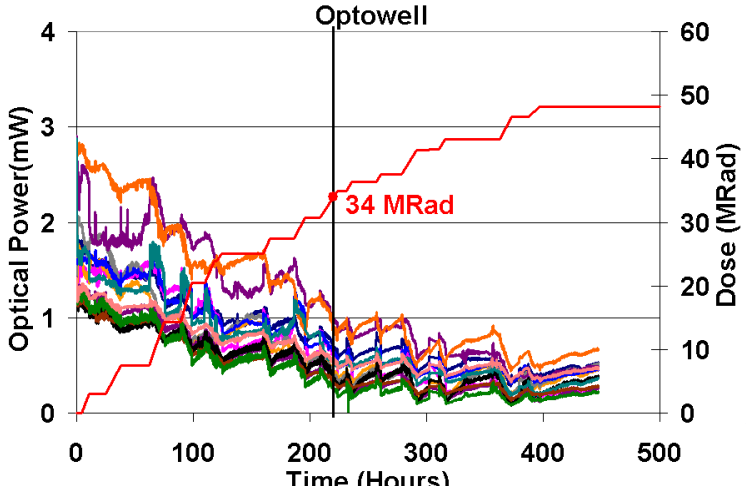


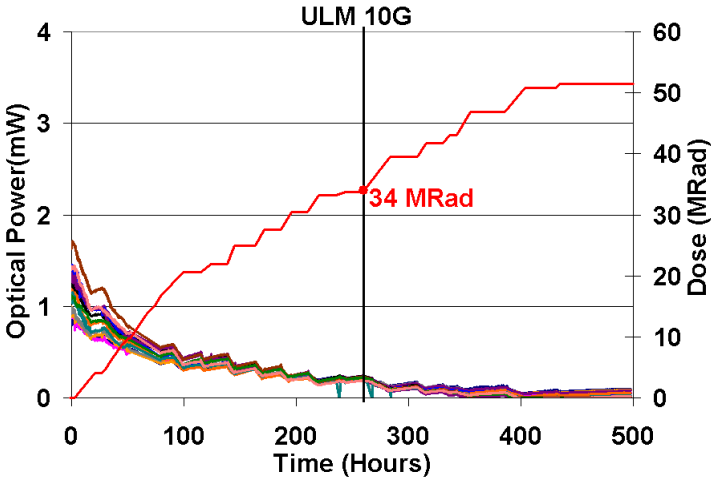
Pre-irrad

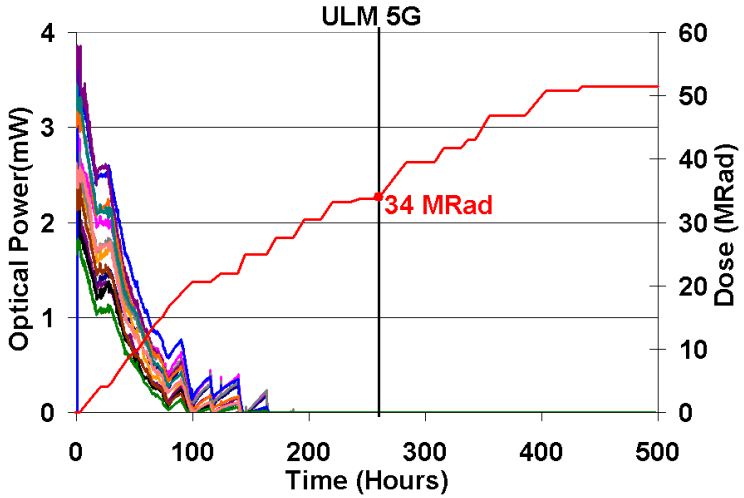
- both arrays have very good optical power

VCSEL Power vs Dosage









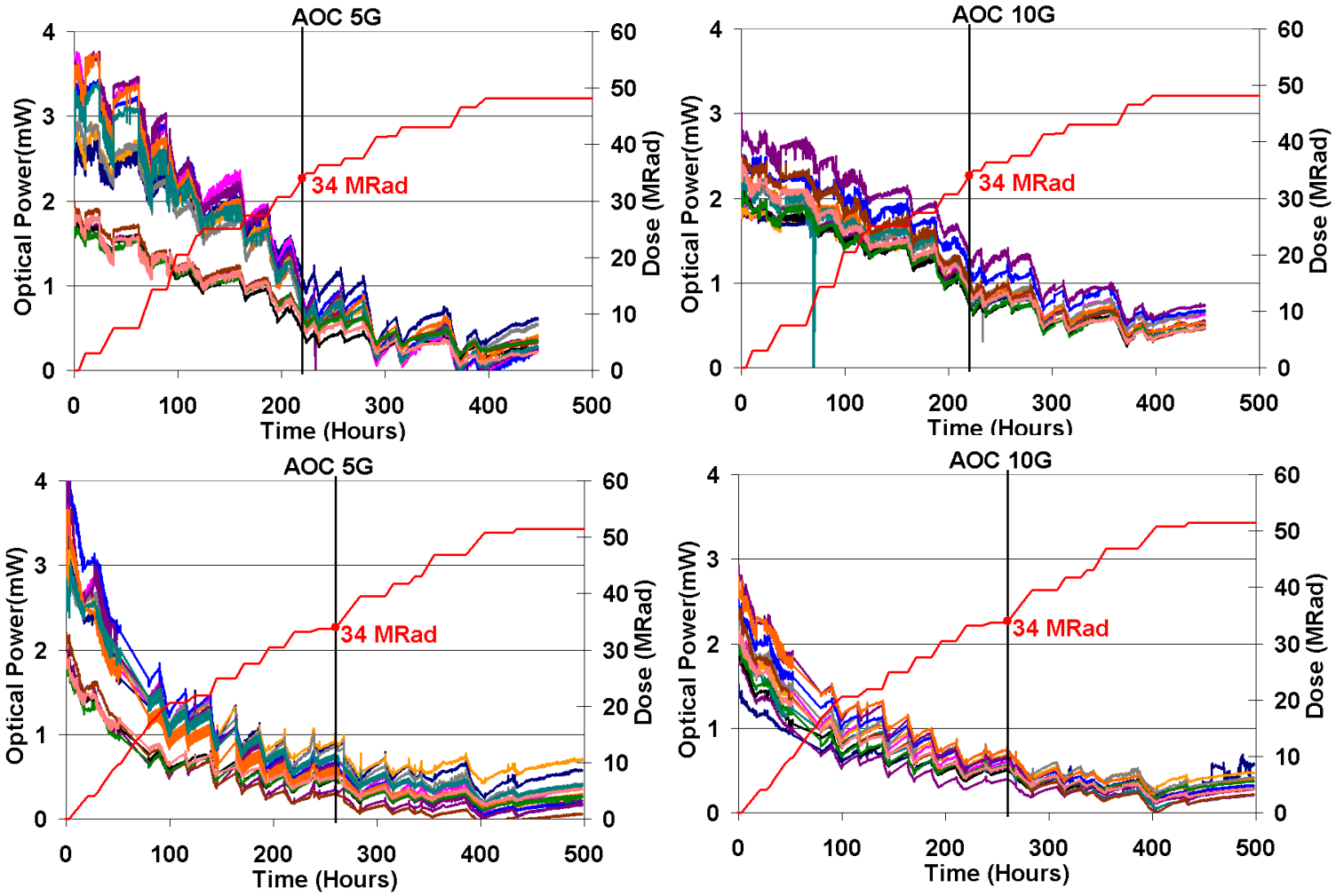
1st irradiation period

2007: Two arrays each (2 x 7 channels)

2nd irradiation period

- Optowell & ULM (10 Gb/s) survive to SLHC dosage

VCSEL Power vs Dosage



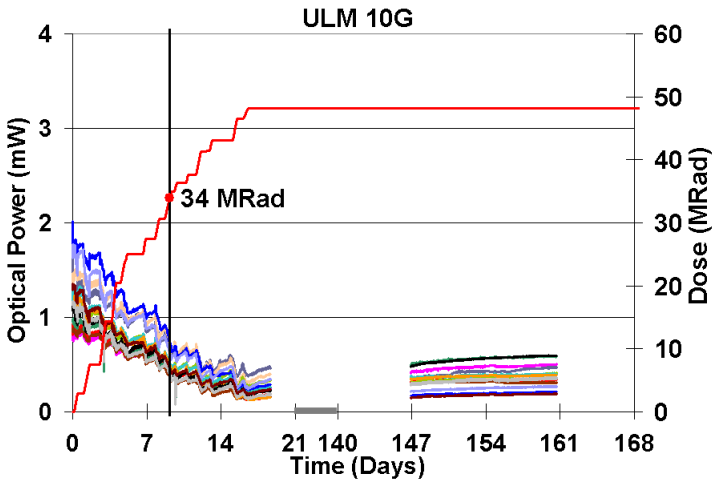
1st irradiation period

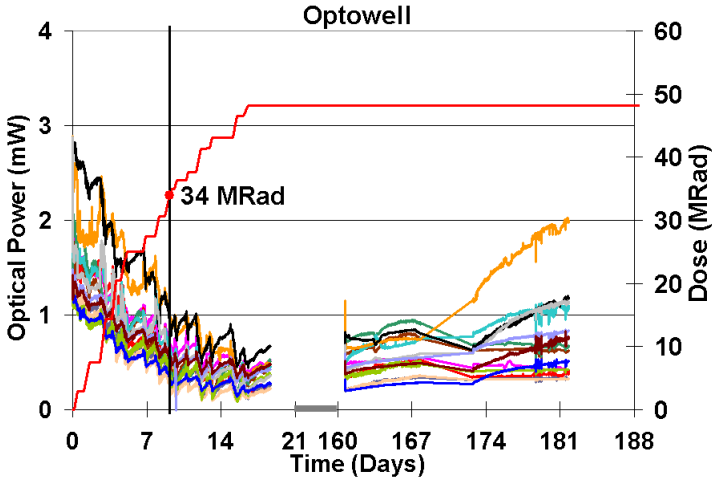
2007: Two arrays each (2 x 7 channels)

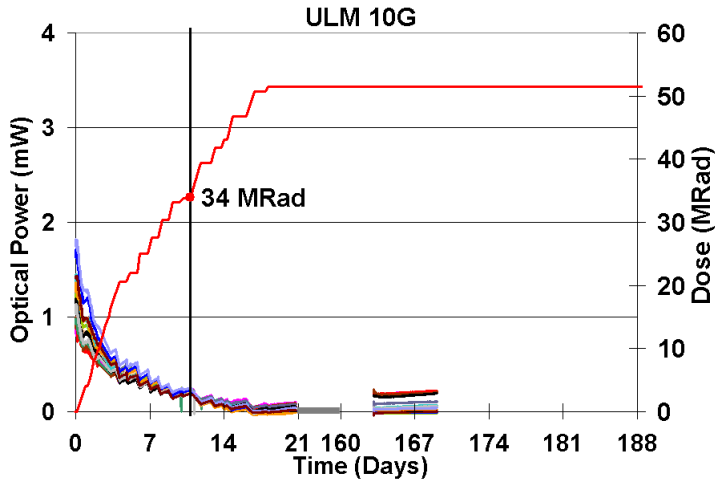
2nd irradiation period

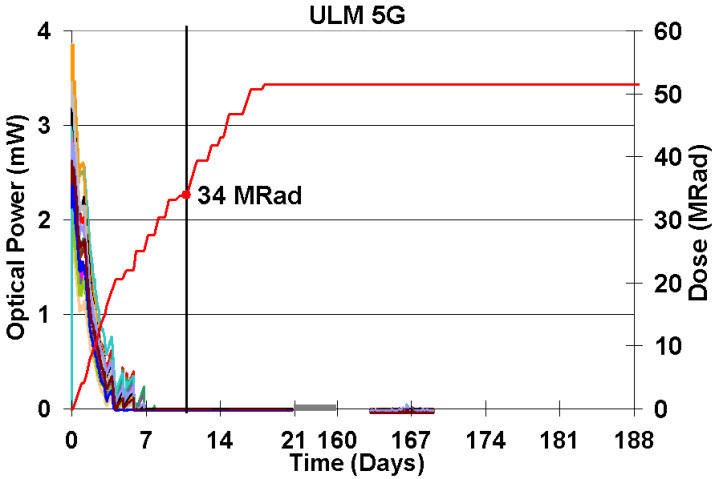
- AOC (5 & 10 Gb/s) survive to SLHC dosage

Annealing of VCSEL Arrays



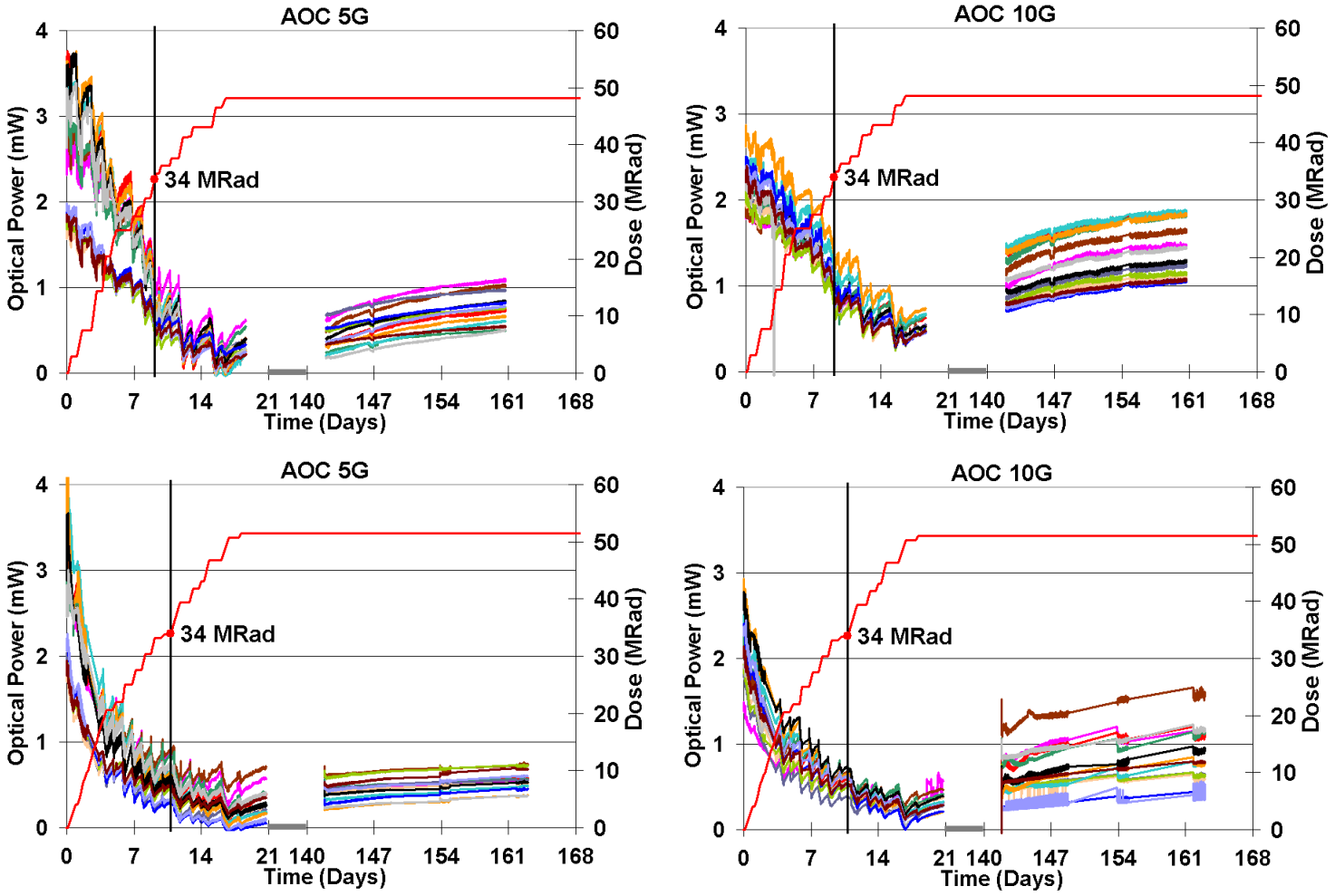






- recovery is slow
- Optowell has the highest annealed power

Annealing of VCSEL Arrays

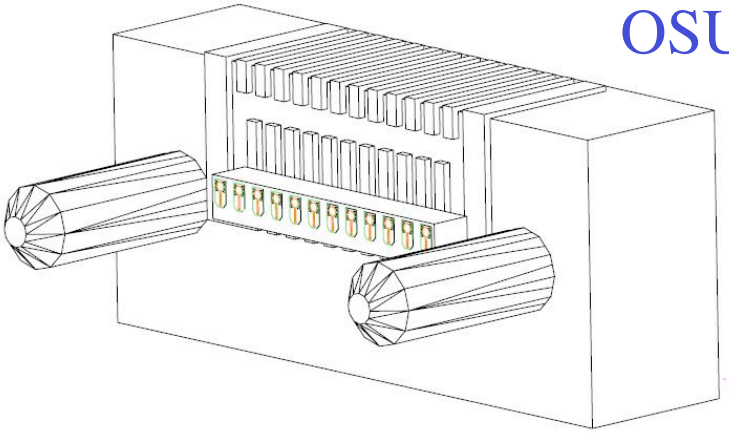


- recovery is slow but adequate annealed power

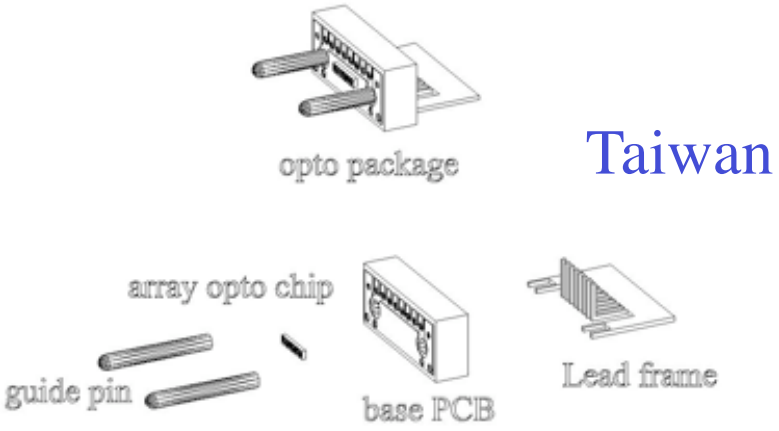
Opto-Pack Development

- current pixel detector uses Taiwan optical packages
  - ☹ VCSEL mounted on PCB with poor heat conduction
  - ☹ micro soldering of 250 μm leads is difficult
- Ohio State develops new opto-pack for SLHC
  - uses BeO base with 3D traces for efficient heat removal
  - wire bond to driver/receiver chip

OSU

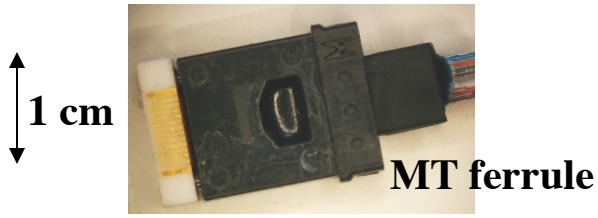


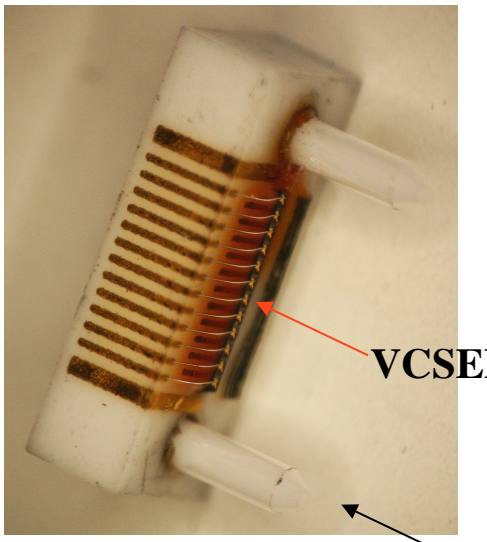
Taiwan

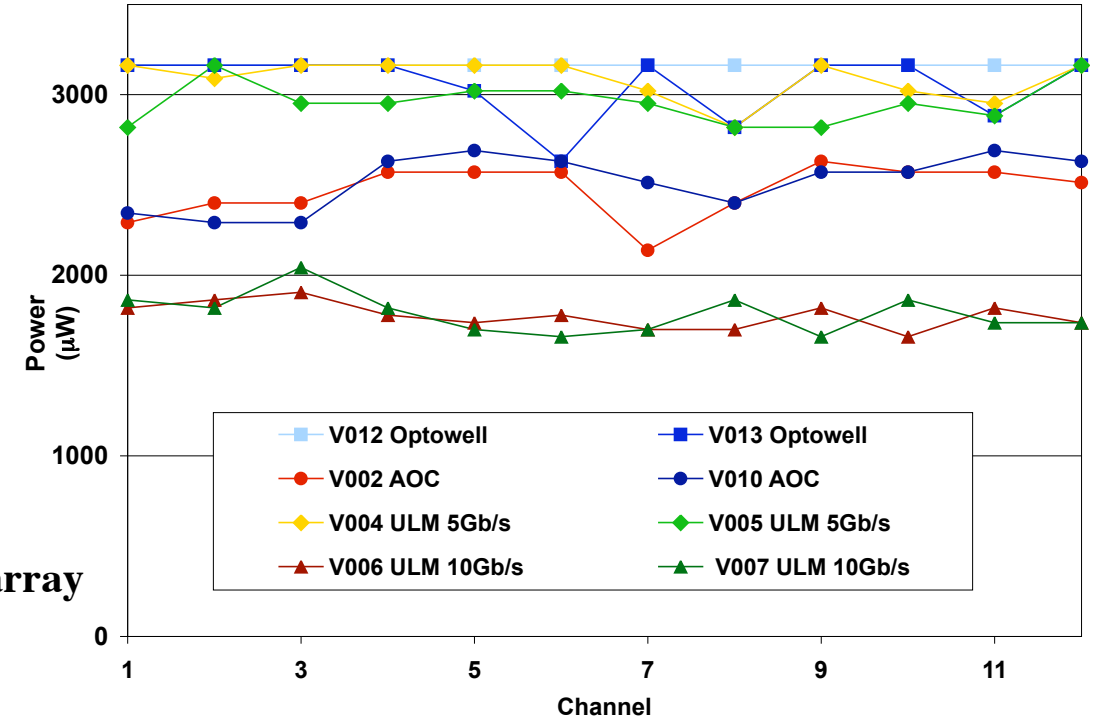


Results on Opto-Packs

- 35 VCSEL & 6 PIN opto-packs have been fabricated
  - all VCSEL opto-packs except one have good coupled power
- ⇨ principle of new opto-pack has been demonstrated







Opto-Chips

- Proposal is to submit 4 mm^2 prototype chips:
  - receiver/decoder operating at 40, 160 and 320 MHz
    - use bi-phase marked encoding due to the low speed
  - VCSEL driver operating at 640 Mb/s and 3.2 Gb/s
  - both designs take advantage of LHC experience
  - SMC block: 3.2 GHz serialization clock
- Goal:
  - gain experience with IBM 130 nm technology
  - find out problems/limitations of design
  - test radiation-hardness/SEU in summer 2008
  - submission date: Monday, March 24
  - cost: $18K

Relation to GBT/Versatile Link

- GBT: driver/receiver operating at several Gb/s are being designed:
  - operate with single mode laser (1310 nm)
    - ATLAS SCT/Pixel use multi-mode laser (850 nm)
  - ⇨ no duplication of effort
- Versatile Link:
  - proposal has been submitted to ATLAS/CMS to develop opto-links with single channel devices
  - Versatile Link group is fully aware of the R&D effort here via the ATLAS/CMS Joint Opto-Link Working Group

Summary

- much progress in last three years on R&D of various components:
  - micro cables
  - fusion spliced SIMM/GRIN fibers
  - Si and GaAs PIN arrays
  - VCSEL arrays
  - array packaging
- ✔ these components can be used for the upgrades and bandwidth and radiation-hardness limitations have been measured
- Questions for the Review Committee:
  - Is it time to fabricate prototype opto-chips to learn the limitations?
  - Will the design be ready for March 24th submission?
  - What changes should be implemented before/after submission?