ASICs: Will We Reach 10 G Arrays?

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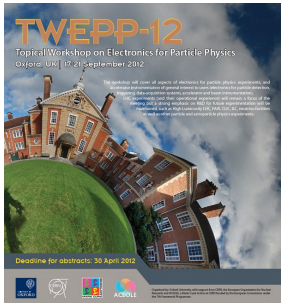
VCSEL Arrays



- Arrays with suitable bandwidth are available from our preferred vendors
- 10 Gb/s arrays from ULM and AOC have been tested to HL-LHC dose
  - optical power degradation is acceptable
  - bandwidth has not been verified
- Awaiting receipt of irradiated array driver ASIC and VCSEL to test operation at 5 Gb/s

10 Gb/s Array Driver

- From literatures and commercial products
  - ⇨ we know that a 10 Gb/s VCSEL driver is possible using:
    - 180 nm CMOS
    - 130 nm BiCMOS
    - 130 nm CMOS
    - 90 nm CMOS…
- From our preliminary work
  - ⇨ it seems that we can achieve 10 Gb/s in 130 nm CMOS

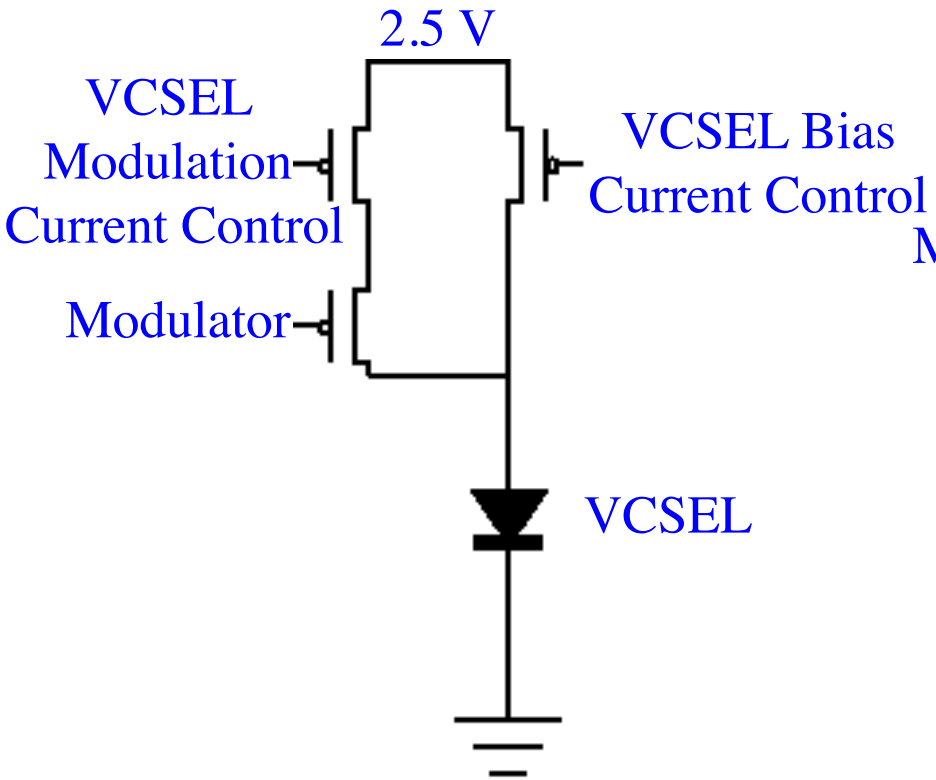
10 Gb/s Driver in 130 nm CMOS?

- If we can achieve this
  - ⇨ low cost compared to BiCMOS or 65 nm
- Need different architecture than our present 5 Gb/s array driver ASIC:
  - Differential receiver:
    - Use CML/LVPECL/ECL like receiver
    - LVDS or LVDS like above 4 Gb/s is not commercially available
    - Working on receiver design now
  - VCSEL driver:
    - Switch to using negative cathode bias
    - No thick oxide transistors
    - Preliminary results on extracted layout simulations look promising

Improved 130 nm VCSEL Array Driver

Existing design

(thick oxide FETs)



New preliminary design

(thin oxide FETs)