Update on Opto-Link R&D

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Outline

- Transmission on micro-cables
- Bandwidth of fiber
- Radiation hardness of PIN arrays
- Radiation hardness of VCSEL arrays
- Status of driver/receiver chips design
- Plan for new TX/RX modules
- Summary

Transmission on Micro-Cables

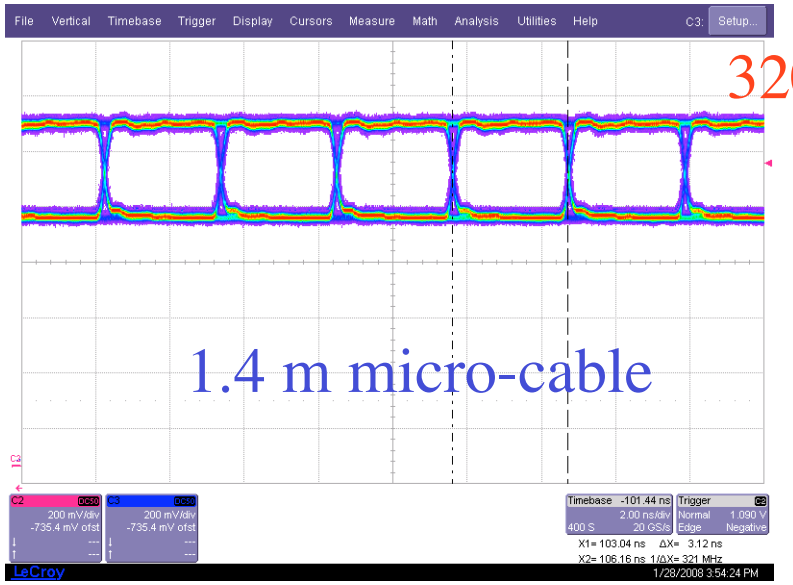
- optical links of current pixel detector use micro-twisted pairs for transmission between pixel and opto modules
  - transmission at 640 Mb/s up to 1.4 m is adequate
  - ✔ satisfy the requirements of B-layer and SLHC upgrades
- new pixel electronics without MCC requires many more micro-cables to distribute clock and data to each FE
  - can these signal be shared?
  - ⇨ test with commercial LVDS driver/receivers…

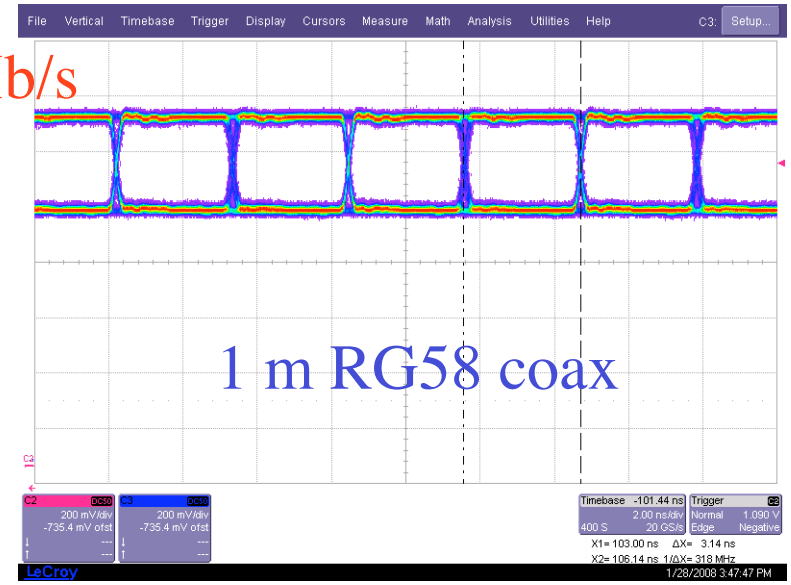
Test Setup of Shared LVDS

- mock up a stave with 4 commercial LVDS receivers (FEs)
  - space between receivers: 20 mm
  - use 2-layer PCB with ground plane and match length pairs
    - no special impedance control
  - all 4 inputs tied to a common pair of PCB traces
  - PCB trace pair driven by 1.4 m of micro-cable
  - one 100 Ω termination

Quality of Shared LVDS

- common input trace driven by different cable:





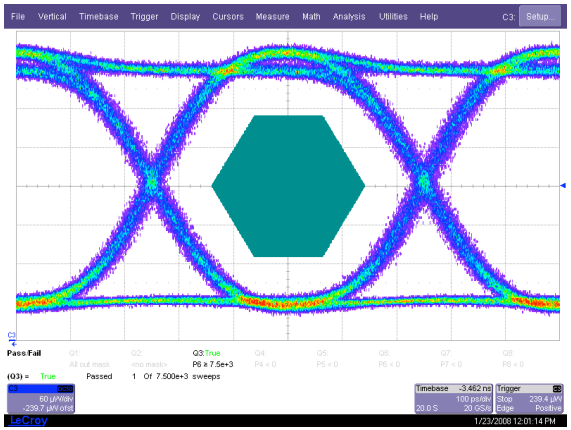
- signal driven by micro-cable is only slightly worse
- good signal on all 4 channels regardless of termination locations
  - ⇨ 4 x reduction in TTC cables?
  - ⇨ should repeat test with custom driver/receivers

Bandwidth of Fiber

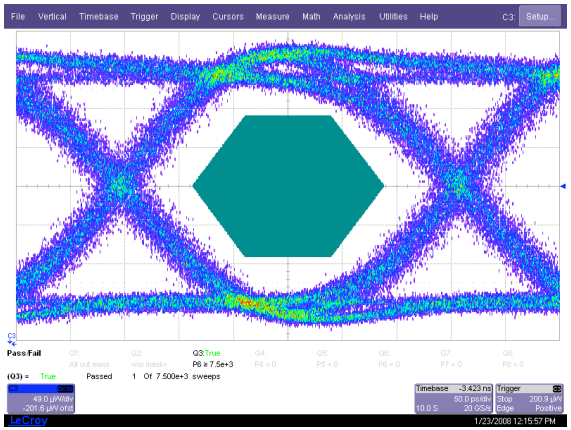
- optical links of current pixel detector use rad-hard/low-bandwidth SIMM fiber fusion spliced to rad-tolerant/medium-bandwidth GRIN fiber
  - can transmit up to at least 2 Gb/s
  - ⇨ what is the limit of the bandwidth?

Bandwidth of Fiber

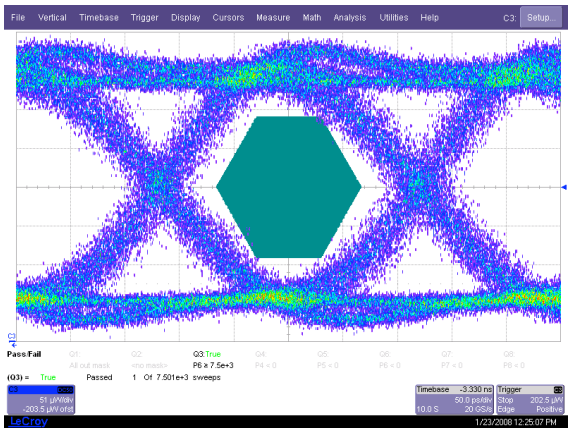
11 + 80 m spliced SIMM/GRIN fiber



2 Gb/s



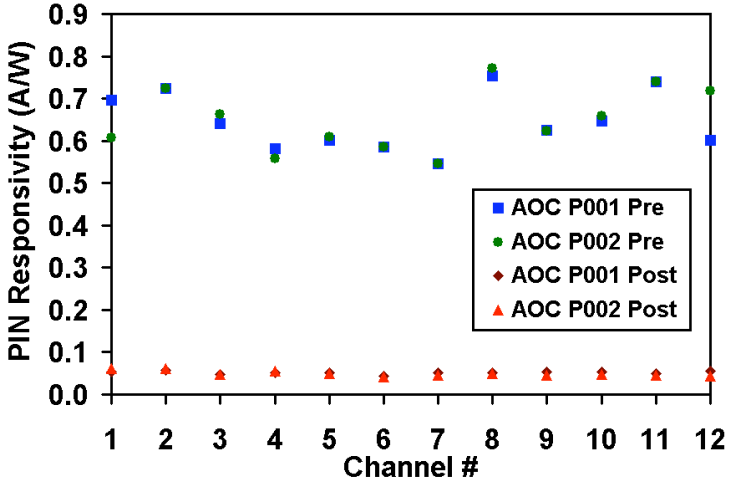
3.2 Gb/s

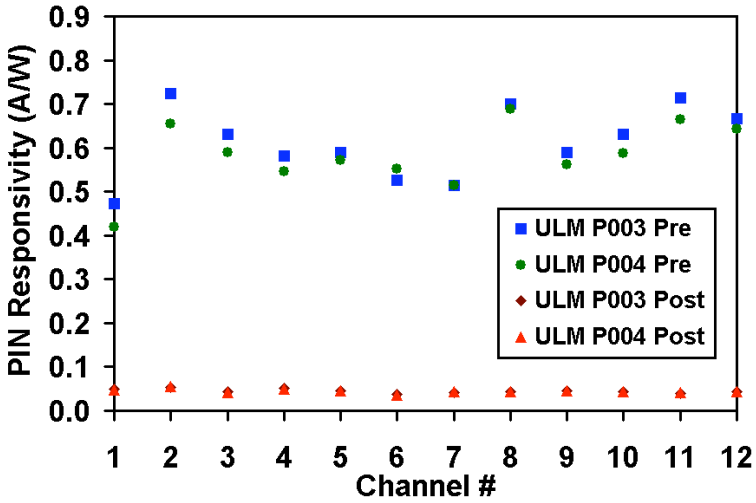


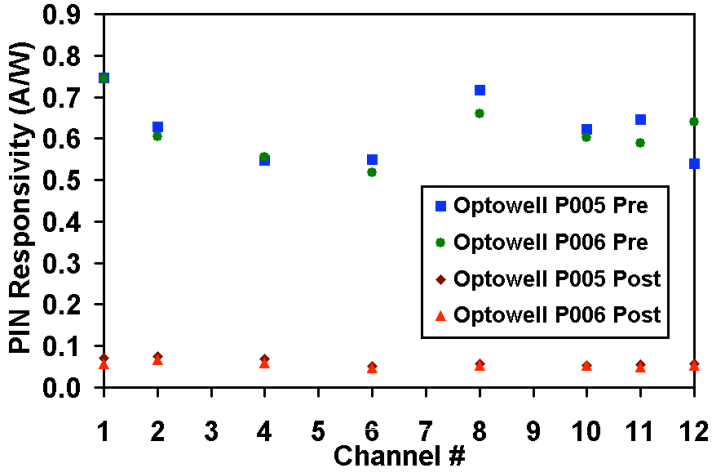
4.25 Gb/s

- transmission at 3.2 Gb/s is adequate
  - ✔ satisfy the requirement of B-layer upgrade
  - ■ current SLHC architecture calls for raw rate of 3.2 Gb/s plus 20% overhead for 8b/10b encoding
  - ⇨ more efficient encoding will improve margin of operation

Radiation-Hardness of GaAs PIN

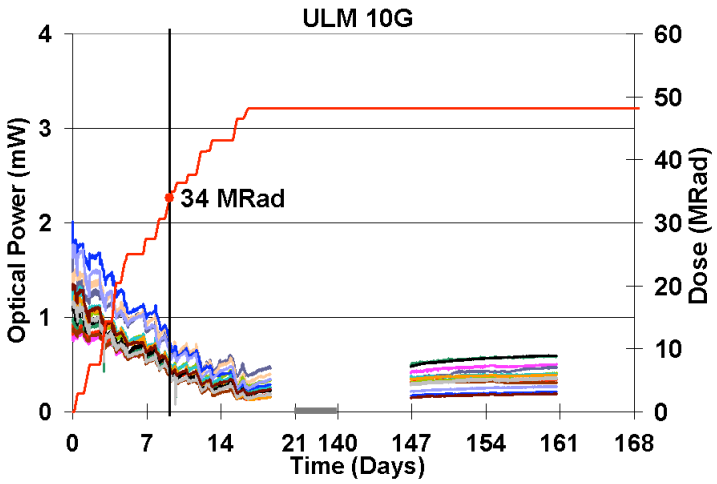


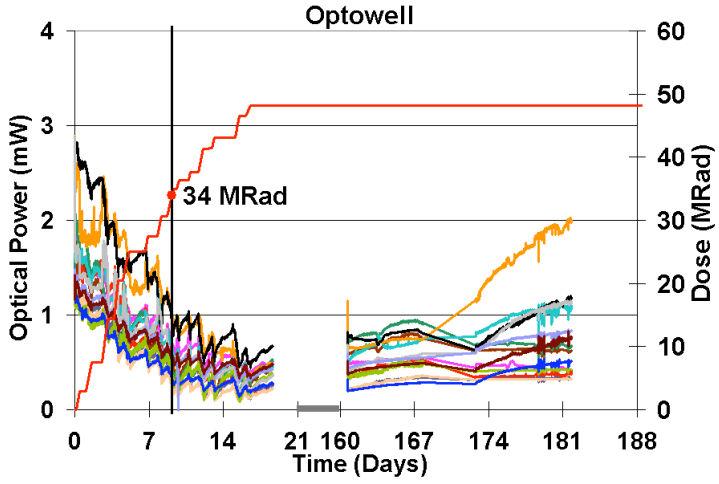


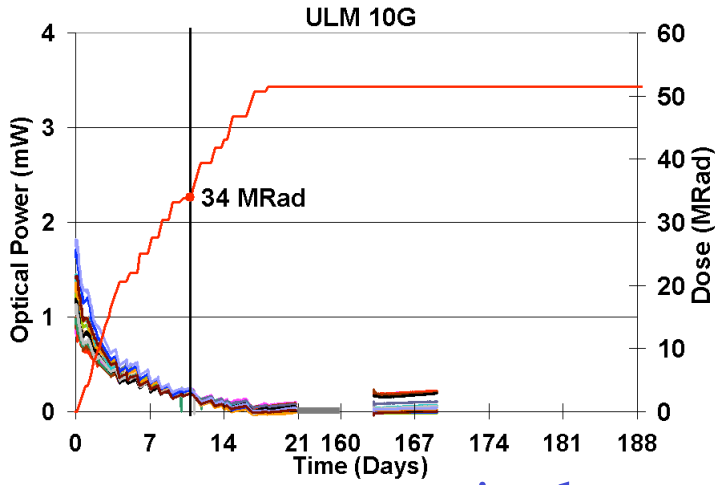


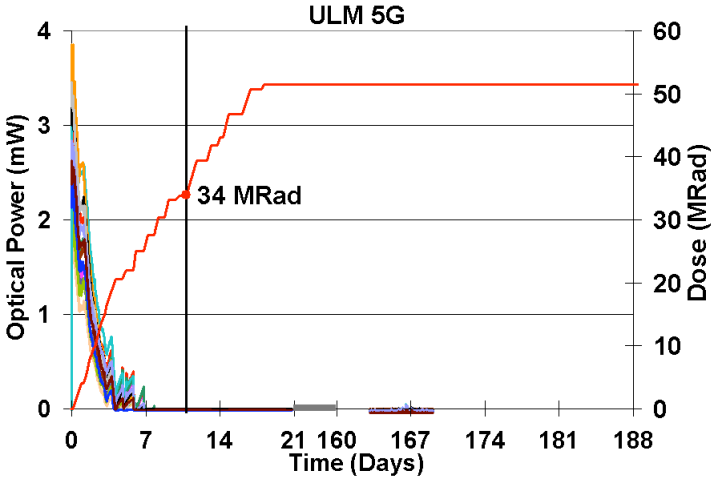
- all arrays are front side illuminated
- PIN responsivities decrease by ~10x at 53 Mrad
- should repeat irradiation to SLHC dosage of 34 Mrad
- Si PIN can operate up to at least 160 MHz at SLHC dosage

Annealing of VCSEL Arrays



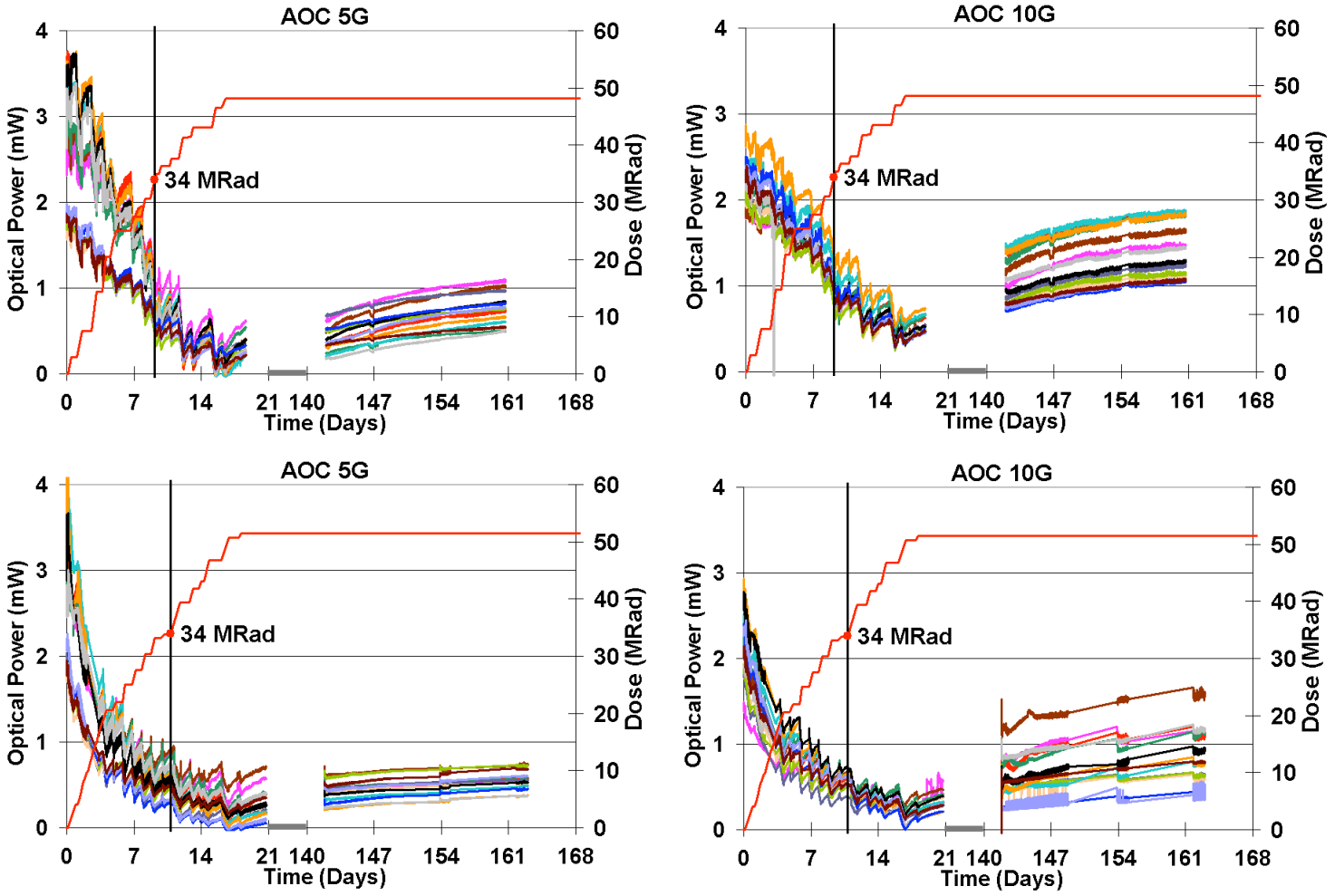






- recovery is slow
- Optowell has the highest annealed power

Annealing of VCSEL Arrays



- recovery is slow but adequate annealed power

Status of VDC

- works well up to 2 Gb/s at
  - 5 fixed process corners
  - supply voltage: 1.2 & 1.5 V
  - -15, 25, & 50 C
- layout completed and simulated from extraction with parasitics, including pads/wire bonds
- will push the bandwidth to 3.2 Gb/s
- plan to submit both low and high speed versions

Status of DORIC

- trans-impedance + limiting amplifiers work up to 1 Gb/s:
  - wide dynamic rang: 50 - 1000 μA
  - corner simulation in progress
- near complete design of decoder of 160 MHz clock and data
  - based on BPM input data as in present pixel TTC
- plan to also produce a version with twice the speed

Status of SMC

- working on building blocks at schematic level:
  - serializer
  - clock multiplier: generate high speed serializer clock from TTC
  - programmable delay
  - FIFO
- work in collaboration with MC designers
- plan to have a few test circuits ready…

Chips Submission Plan

- submit a 2 x 2 mm^2 chip to MOSIS via CERN:
  - VDC
  - DORIC
  - SMC “very lite”
- submission: March 24
  - review: March 11
  - PS irradiation: summer
    - will compare SEU at 40, 160, and 320 Mb/s

Design of New TX/RX Modules

- use 12-channel TX/RX dice from Helix Semiconductor
  - can operate up to 4.25 Gb/s
  - TX: DAC for setting current in each VCSEL
  - RX: limiting-amp with large dynamic range
    - no need for threshold DAC
  - sample dice on order
- use 12-channel VCSEL/PIN from AOC or Optowell
  - use opto-package designed by OSU
- use FPGA to generate BPM signal at 320 MHz
  - no need for custom BPM chip
- 1st prototype: ~ May 08

Summary

- ✔ TTC signal could be shared by 4 FEs
- ✔ fusion spliced SIMM/GRIN fiber can transmit up to 3.2 Gb/s
- ✘ responsivity of GaAs PIN decreases by 10 x at SLHC dosage
- ✔ VCSELs from two vendors survive to SLHC dosage
- ● small chip submission planned in March
- ● prototyping of RX/TX in May