

#### Status of Opto-Board Production

#### B. Cote, K.K. Gan, H. Kagan, Z. Pollock, S. Smith, H. Lawson, B. Tar, A. Woyshville The Ohio State University

Nov 6, 2019

Pixel Week



#### Outline

- Introduction
- Opto-pack bases
- VCSEL/PIN arrays
- Opto-pack burn-in
- ASIC probing
- Opto-board PCB
- Opto-board QA
- Summary



#### Opto-Board

- needed: 272 boards
- goal: 400 boards





## Status of Opto-Pack Bases

- traces on opto-pack bases in 2018 order were over etched
- vendor claims to understand the problem
- blistering in gold during cleaning process
  - vendor in contact with BeO supplier
  - will try high temp clean air fire at 1500 C



## Status of VCSEL/PIN Delivery

- 300 VCSEL arrays from II-VI delivered
  ULM can't give a delivery date due to yield problem
- 700 additional VCSEL arrays ordered
- PIN arrays ship date: Nov 7<sup>th</sup>



## Opto-Pack Burn-In

- use II-IV VCSEL array in optical package
- II-IV statement: there is a need for a burn-in
- recommend 24 hours of burn-in at 100 C at 10 mA
  - will burn-in for 69 hours at 80 C at 10 mA
- recommended acceptable changes:
  - optical power: -15 to +5% at 6 mA
  - threshold current: -5 to +10%
  - forward voltage increase: < 40 mV at 6 mA

# Test of Opto-Pack Burn-In Concept

challenge: electrical contact with fine traces of 250 µm spacing
jig successfully tested using a broken probe card used in opto-pack QA



 PCB has 4 slightly oversize holes
 springs underneath PCB to ensure probe tips are slightly above traces during alignment K.K. Gan Pixel Week





- VCSEL power coupled to a fiber will fluctuate between measurements due to mode hopping and slightly different coupling
  - standard procedure is to use large area PIN diode
  - test consistency of measurements with repeated remounting to avoid development of setup for large area PIN diode
  - 2 out 130 measurements just above threshold
  - present QA system acceptable for burn-in test K.K. Gan





No failure in 130 measurements
present QA system acceptable for burn-in test



# Opto-Pack Burn-In To-Do List

- design PCB to supply 10 mA to all VCSELs
- 24 VCSEL opto-packs needed per week
  - order 36 probe cards
  - machine 36 aluminum jigs
  - design/machine a rack to hold 36 jigs
- pushing to get everything done in 3 weeks



# **DORIC/VDC** Probing

- two wafers diced
  - PO for dicing two more wafers placed
  - will have two spare un-diced wafers
- use automatic probe station with pattern recognition instead of manual probe station used previously
- new VDC probe card ordered
- VDC probe card PCB designed/ordered
- old DORIC probe card sent for repair
- new probe station controller PC power supply ordered



## Status of Opto-Board PCB

- 150 PCBs were delivered but some traces were over etched
- Cirexx claims that the etching script has been fixed
- expect replacement batch next week
- order for passive components mounting has been placed
- might have PCBs with passive components mounted in 2 weeks



# Opto-Board QA

- need two QA systems to have enough through-put as in 2013/14 production
- one environmental chamber (refrigerator/oven) has broken refrigeration
   service call has been placed
- one QA system is working but needs some software update
- need to get the other QA system working



### Conclusion

- VCSEL procurement problem solved
- new problem in production of opto-pack bases at vendor
- VCSEL opto-pack burn-in is feasible
- significant amount of work remains to launch production on Dec 1<sup>st</sup>