Radiation-Hard ASICs for Optical Data Transmission in the ATLAS Pixel Detector

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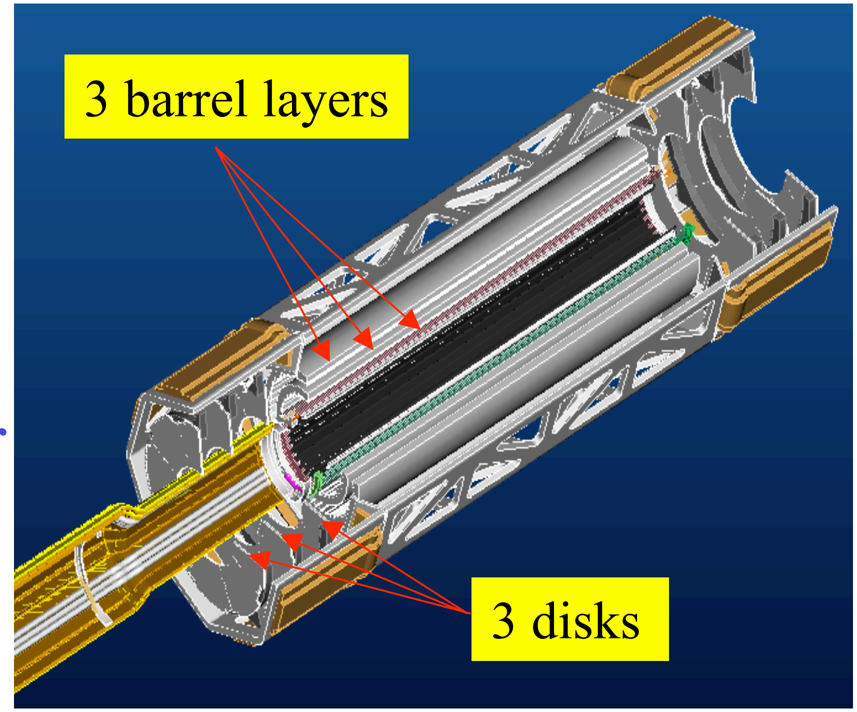
Outline

- Introduction
- Results on IBM 0.25 μm Prototype Chips
- Results on Proton Irradiations
- Summary

ATLAS Pixel Detector

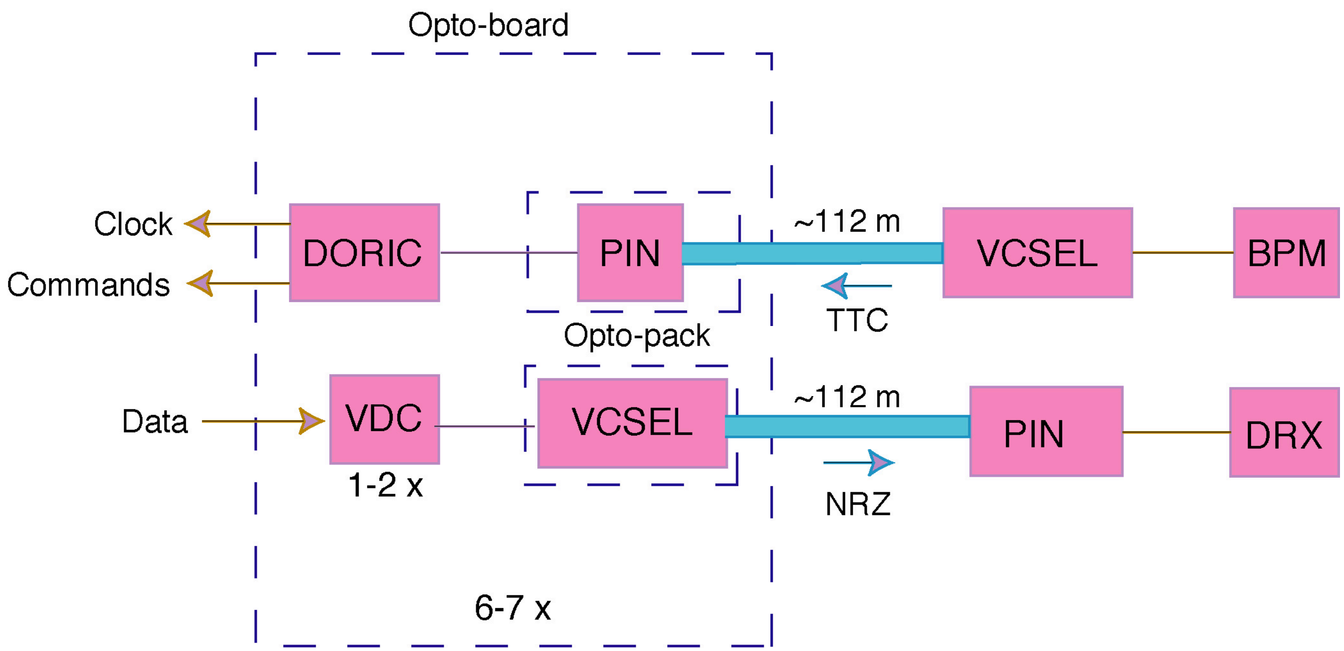


- Inner most tracking detector
- Pixel size: 50 μm x 400 μm
- ~ 100 million channels
- Barrel layers at r = 5.1, 9.9, 12.3 cm
- Disks at z = 50, 58, 65 cm
- Dosage after 10 years:

  middle barrel layer: 50 Mrad or 10^{15} 1-MeV n_{eq}/cm^2

  optical link: 30 Mrad

ATLAS Pixel Opto-link



VCSEL: Vertical Cavity Surface Emitting Laser diode

VDC: VCSEL Driver Circuit

PIN: PiN diode

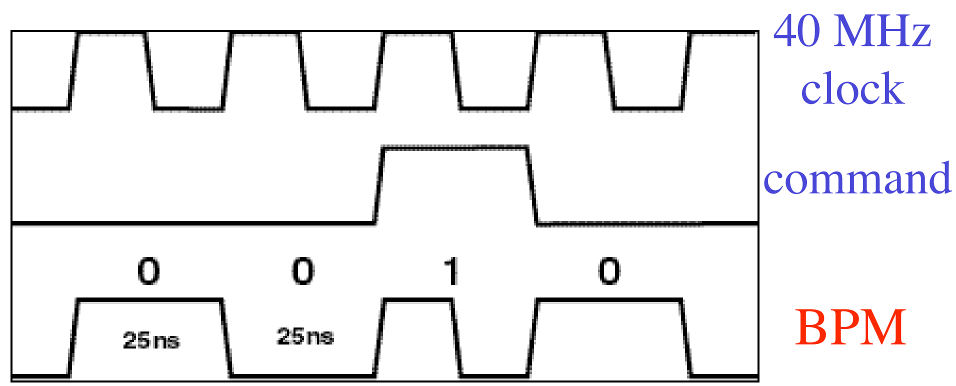
DORIC: Digital Optical Receiver Integrated Circuit

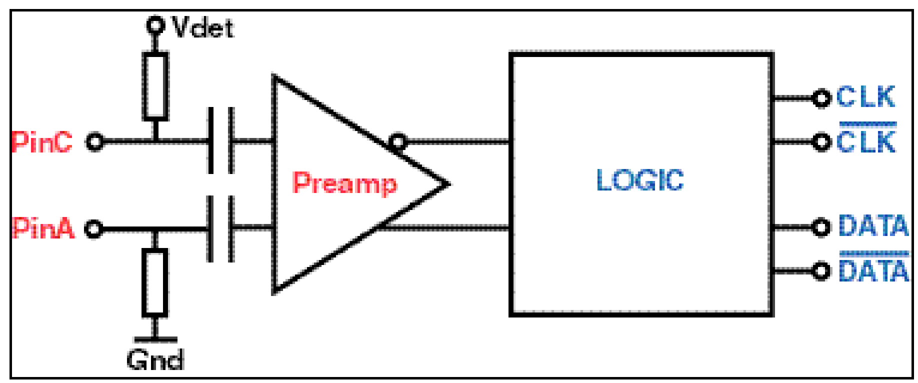
VCSEL Driver Circuit Specs

- Convert LVDS input signal into single-ended signal appropriate to drive VCSEL diode
- Output (bright) current: 0 to 20 mA, controlled by external voltage
- Standing (dim) current: ~ 1 mA to improve switching speed
- Rise & fall times: 1 ns nominal (80 MHz signals)
- Duty cycle: (50 +/- 4)%
- "On" voltage of VCSEL: up to 2.3 V at 20 mA for 2.5 V supply
- Constant current consumption!

Digital Optical Receiver IC Specs

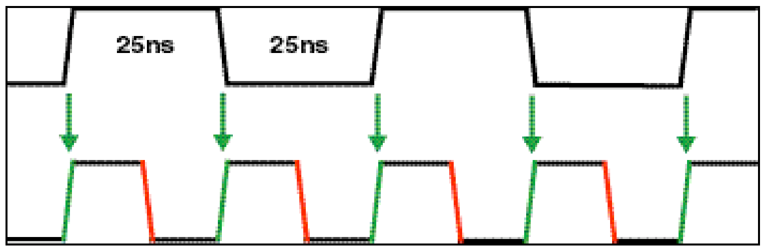
- Decode Bi-Phase Mark encoded (BPM) clock and command signals from PIN diode
- Input signal: 40-600 μA
- Extract: 40 MHz clock
- Duty cycle: (50 +/- 4)%
- Total timing error: < 1 ns
- Bit Error Rate (BER): < 10^{-11} at end of life





DORIC Logic

- Training period: ~25 μs of 20 MHz clock (BPM with no data)



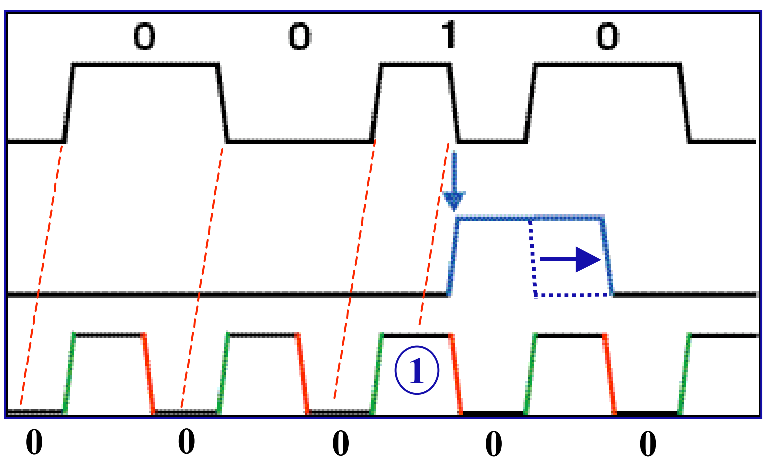
Input transitions ⇨ leading edges

Internal delays ⇨ trailing edges

Delay of Trailing Edges → 40 MHz Recovered Clock

Delay Locked Loop:
Duty Cycle = 50%?

⇨ Ready for data:



BPM

Recovered Data

Recovered 40 MHz Clock

VDC & DORIC Design History

- Original design for ATLAS SemiConductor Tracker (SCT)
  - AMS 0.8 μm BiPolar in radiation tolerant process (4 V)

- DMILL #1-3: Summer 1999 - May 2001
  - 0.8 μm CMOS rad-hard process (3.2 V)
  - VDC & DORIC #3: meet specs
  - severe degradation of circuit performance in April 2001 proton irradiation
  - ⇨ migrate to IBM 0.25 μm (2.5 V) in Summer 2001
  - ⇨ enclosed layout transistors and guard rings for improved radiation hardness

VDC & DORIC Designs in 0.25μm

- **IBM #1-2: June - October 2001**

  VDC: decouple adjustment of bright & dim currents
  more constant current consumption

  DORIC: optimized differential preamp circuit

  ⇨ both circuits meet specs

- **IBM #3: November 2001**

  VDC: further improvements in current consumption

  DORIC: single-ended preamp keeps 10 V PIN bias off chip
  improved delay control circuit…

  ⇨ single-ended preamp matches prior performance

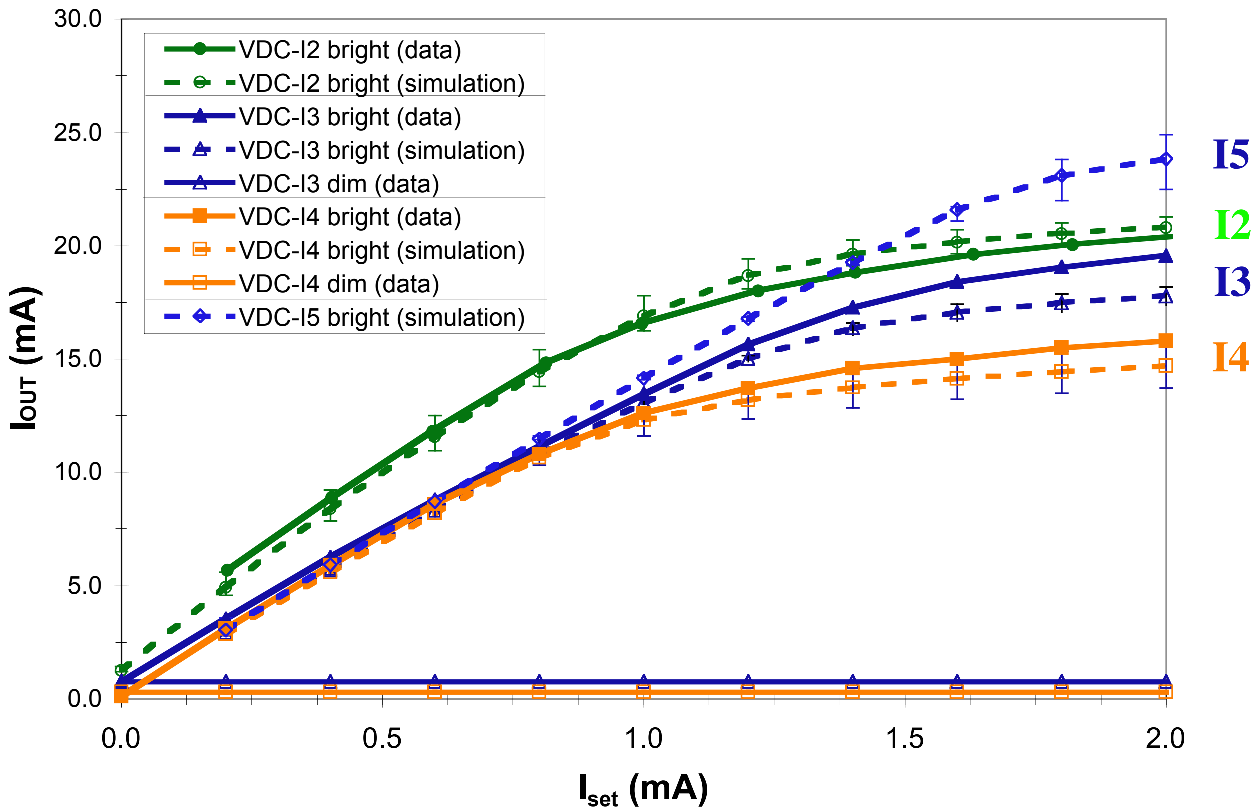
- **IBM #4: April 2002**

  VDC: compatible with common cathode VCSEL arrays, 4-channel chip

  DORIC: preamp optimized for common anode PIN arrays
  improved delay control circuit: centers clock at 50% duty cycle
  reset added for slow and controlled recovery…4-channel chip

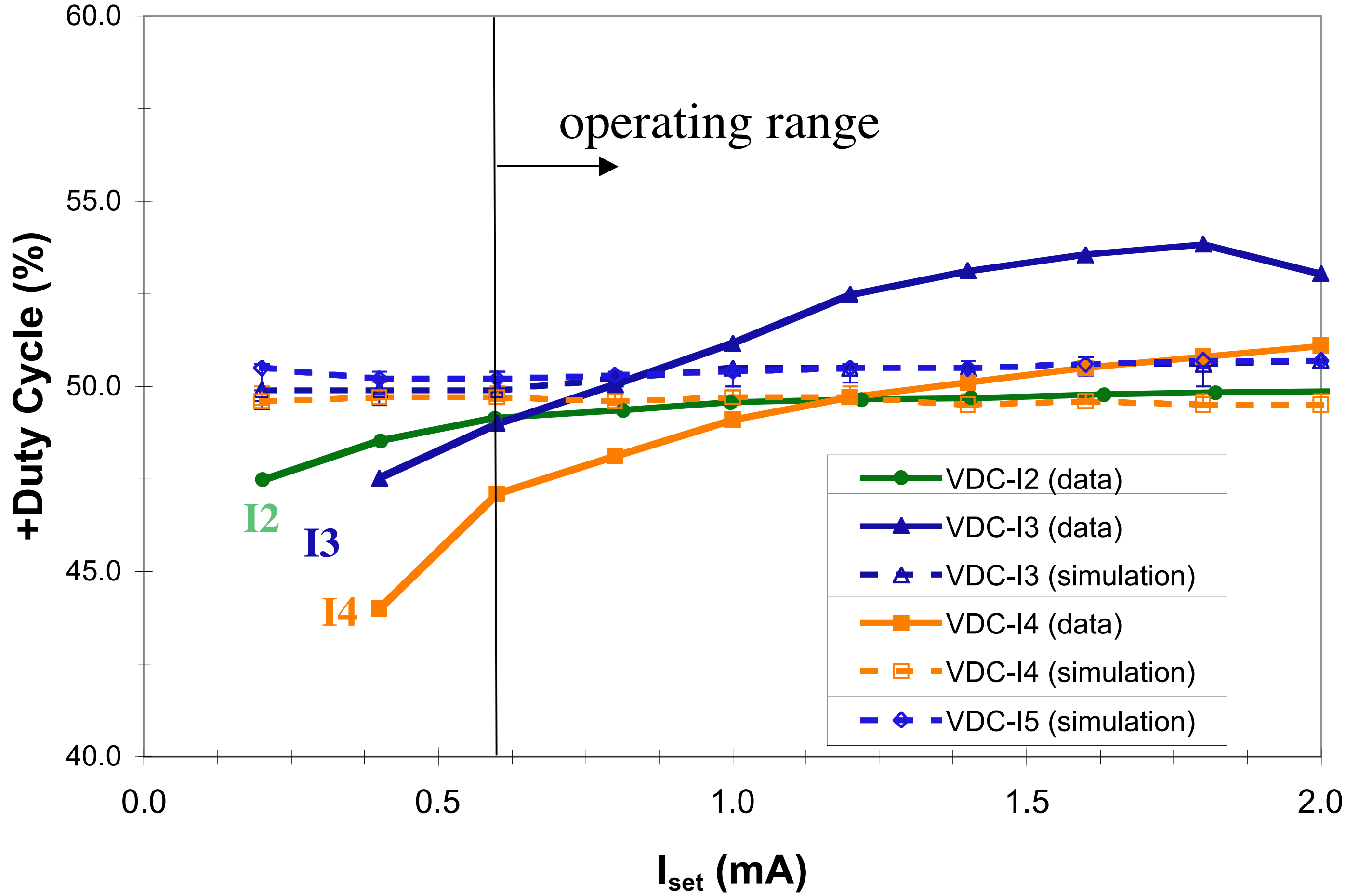
  ⇨ improved performance over #3

VDC-I4: VCSEL Drive Currents vs I_{set}



- turning over at high I_{set} is due to 10 Ω in series used in measurement
- dependence of bright current vs I_{set} is as expected
- need to increase bright (VDC-I3 reached 20 mA) and dim (1 mA) currents
- VDC-I5 is predicted to produce more currents

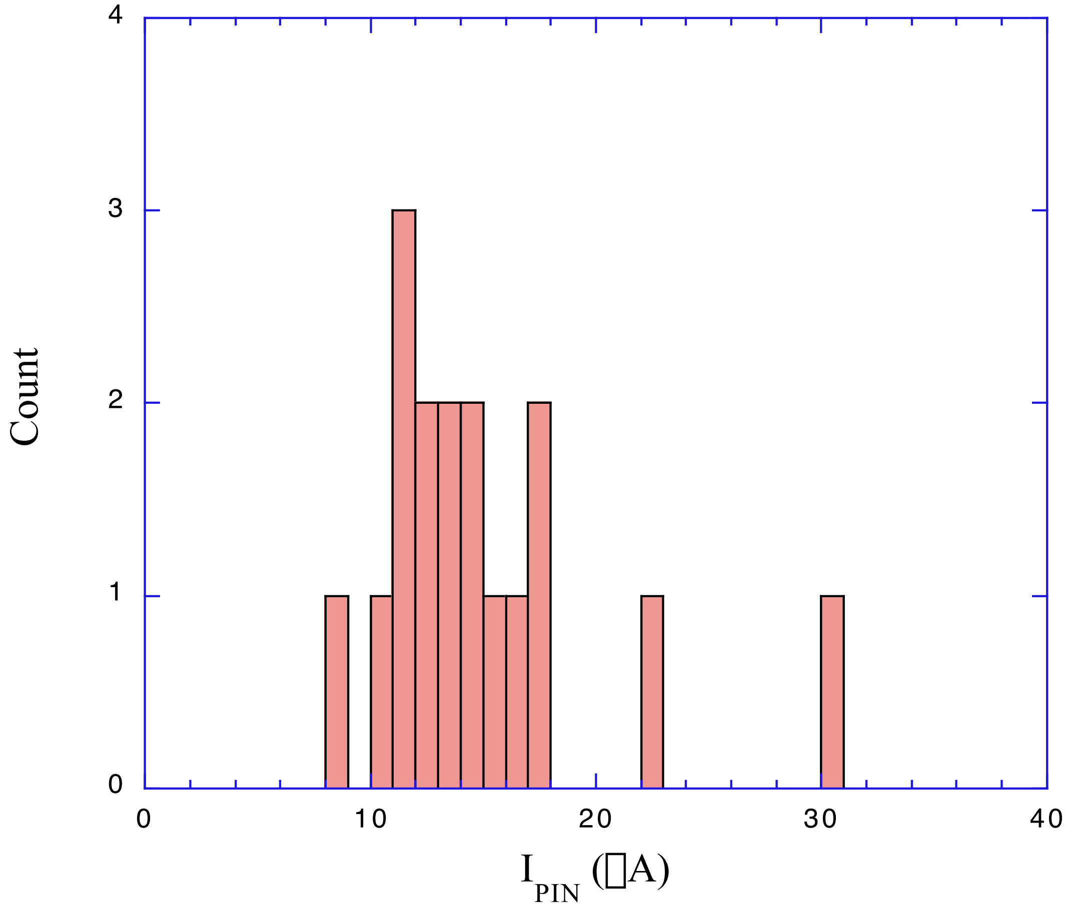
Duty Cycle vs I_{set} for 40 MHz Clock



- clock duty cycle close to 50%
- rise & fall times: 1.0-1.5 ns over operating range

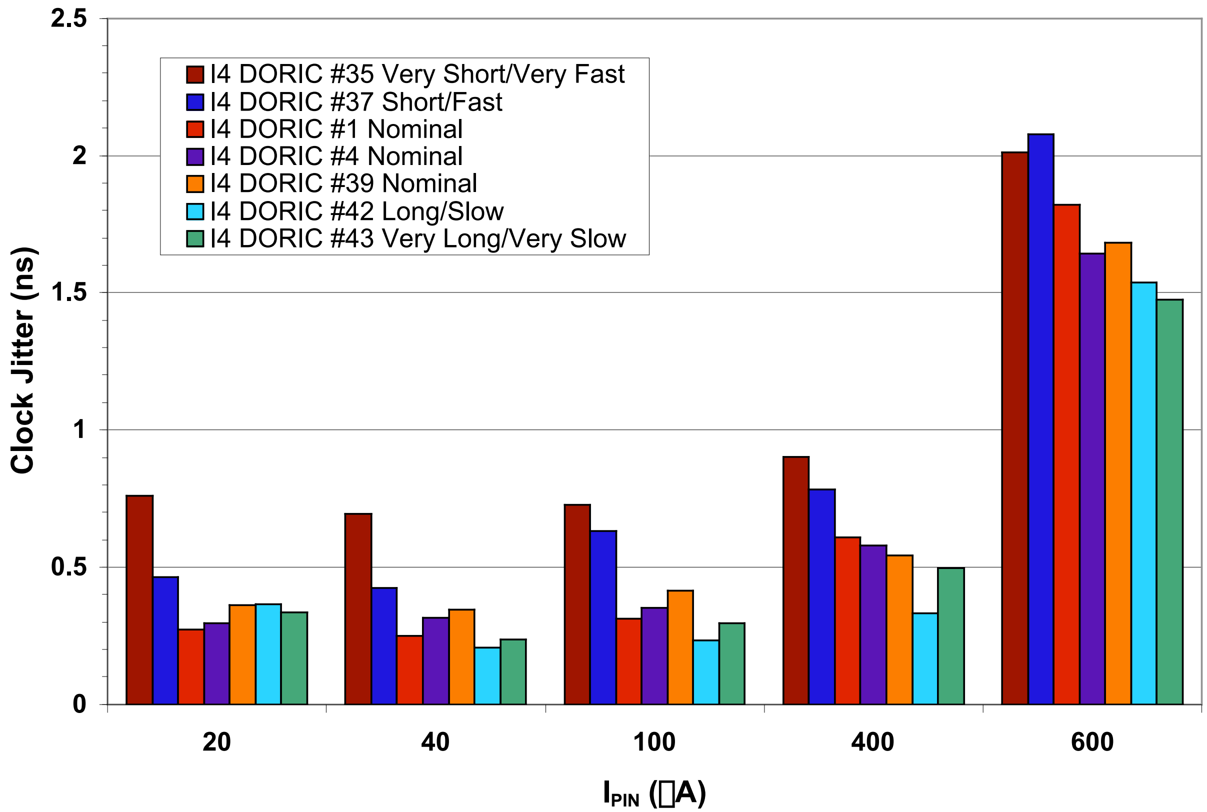
⇨ improve speed of pFETs used to drive common cathode VCSEL

PIN Current Thresholds in DORIC-I4



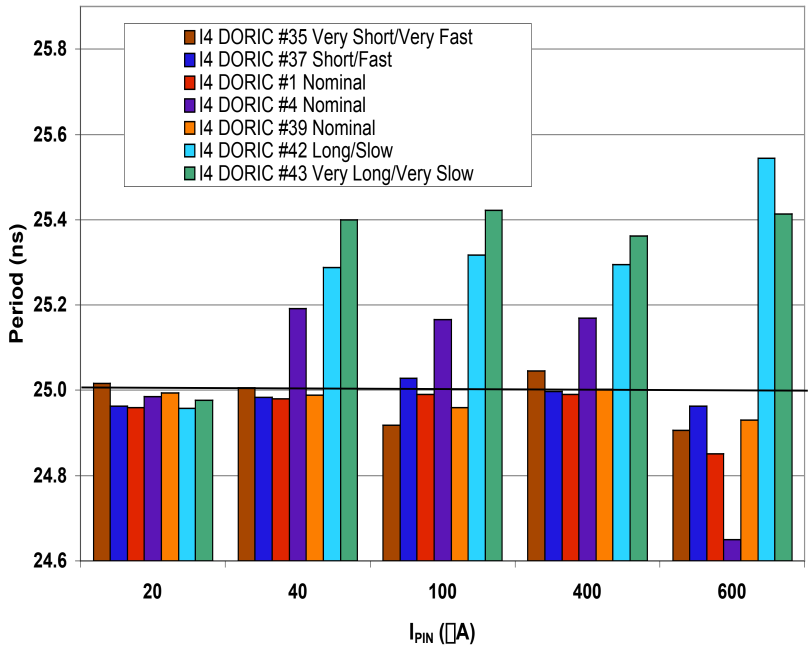
- PIN current thresholds for no bit error are low: ~ 15 μA

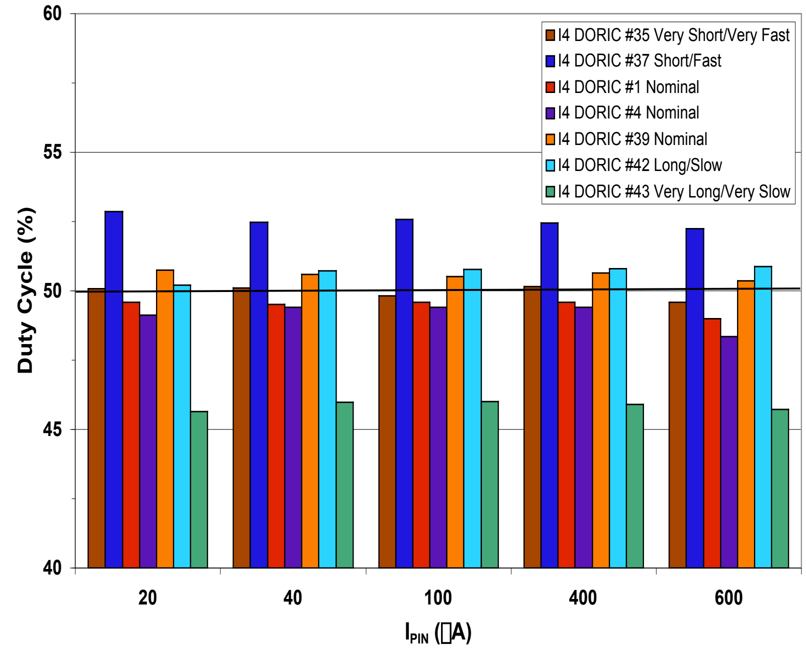
Jitter of Recovered Clock in DORIC-I4



- jitter is low for low PIN current
- jitter is large for high PIN current due to kludge used in getting DORIC to work with common cathode PIN

Period/Duty Cycle of Recovered Clock in DORIC-I4

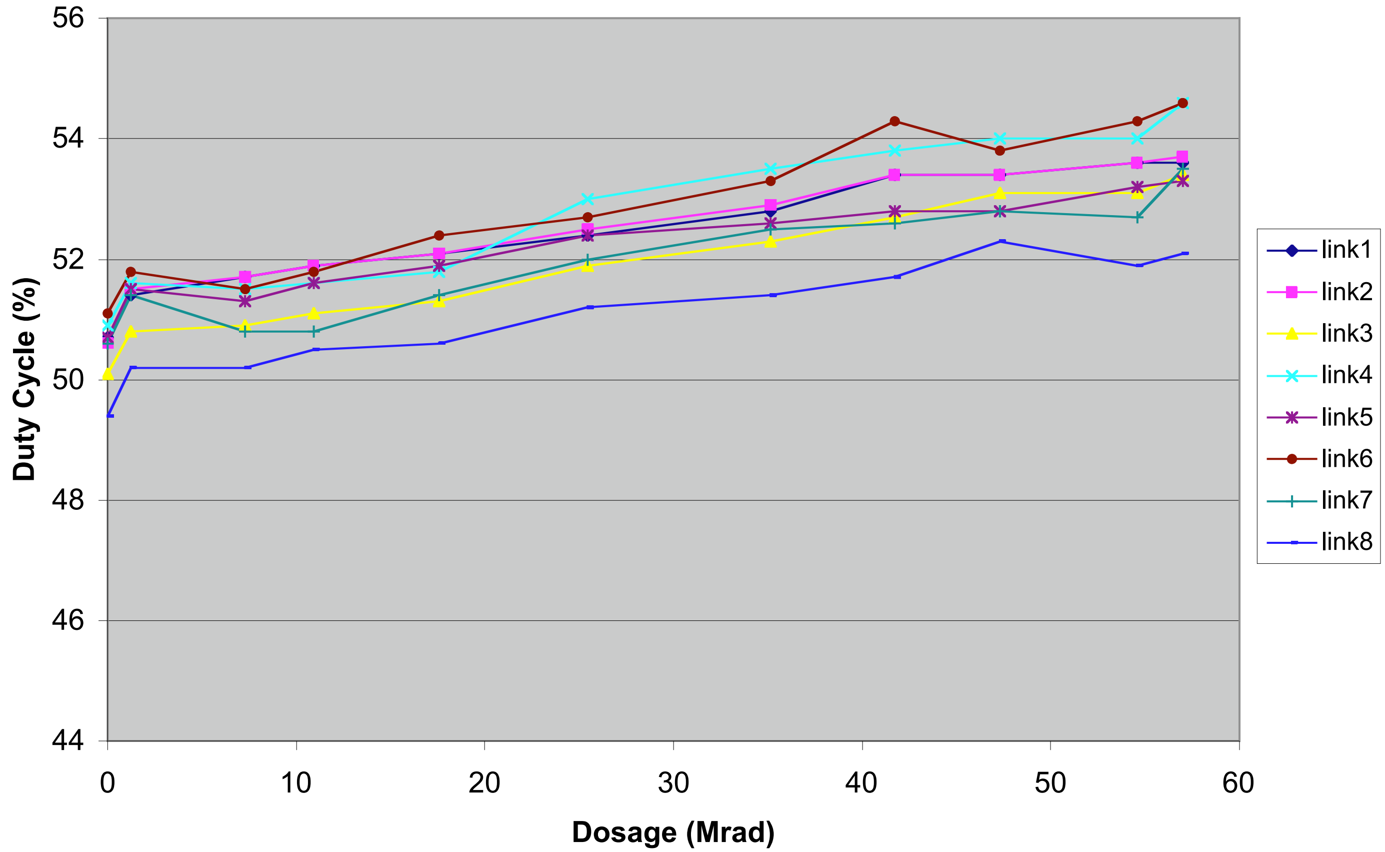




- clock period is close to 25 ns
- clock duty cycle is close to 50%

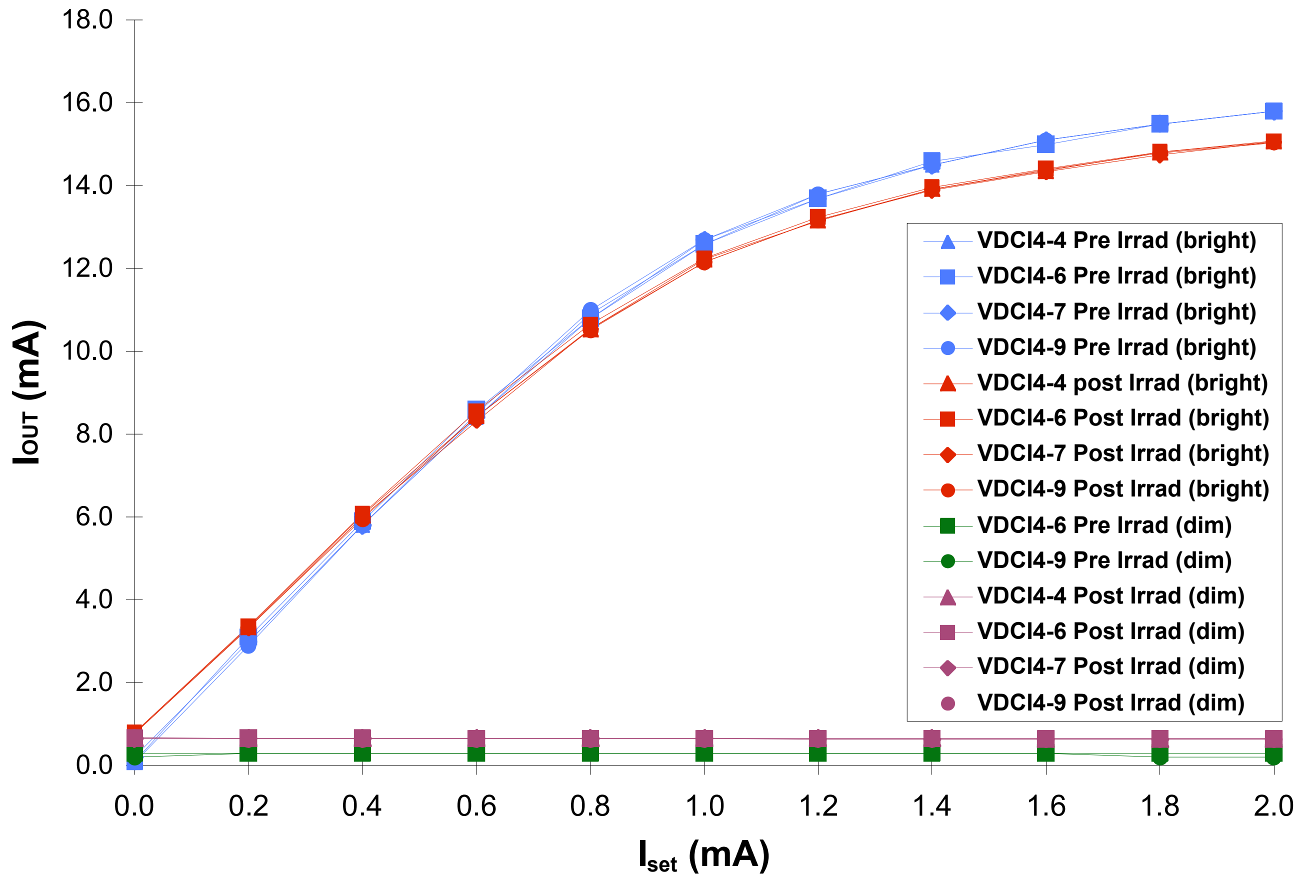
VDC-I4: Clock Duty Cycle vs. Dosage

- irradiated opto-electronics with 24 GeV protons at CERN



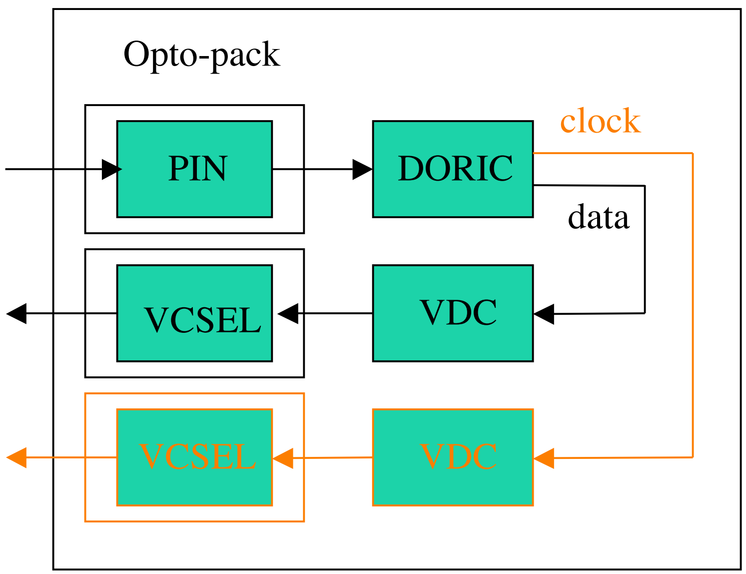
- duty cycle increases by ~ 2% after 58 Mrad

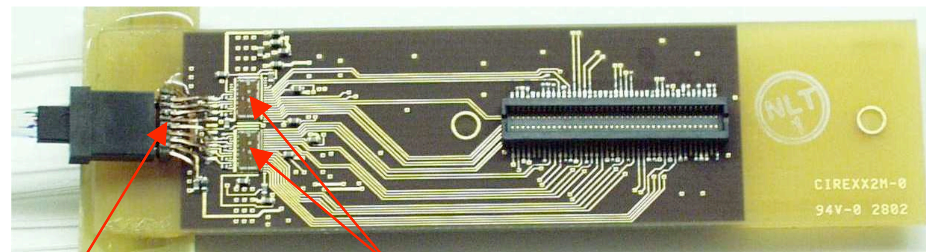
VCSEL Drive Current of Irradiated VDC-I4



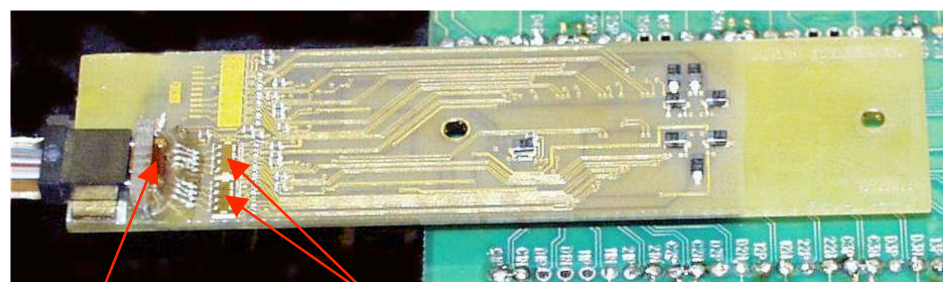
- no degradation from irradiation
- similar result for irradiated VDC-I3

Opto-Board for Irradiation Study



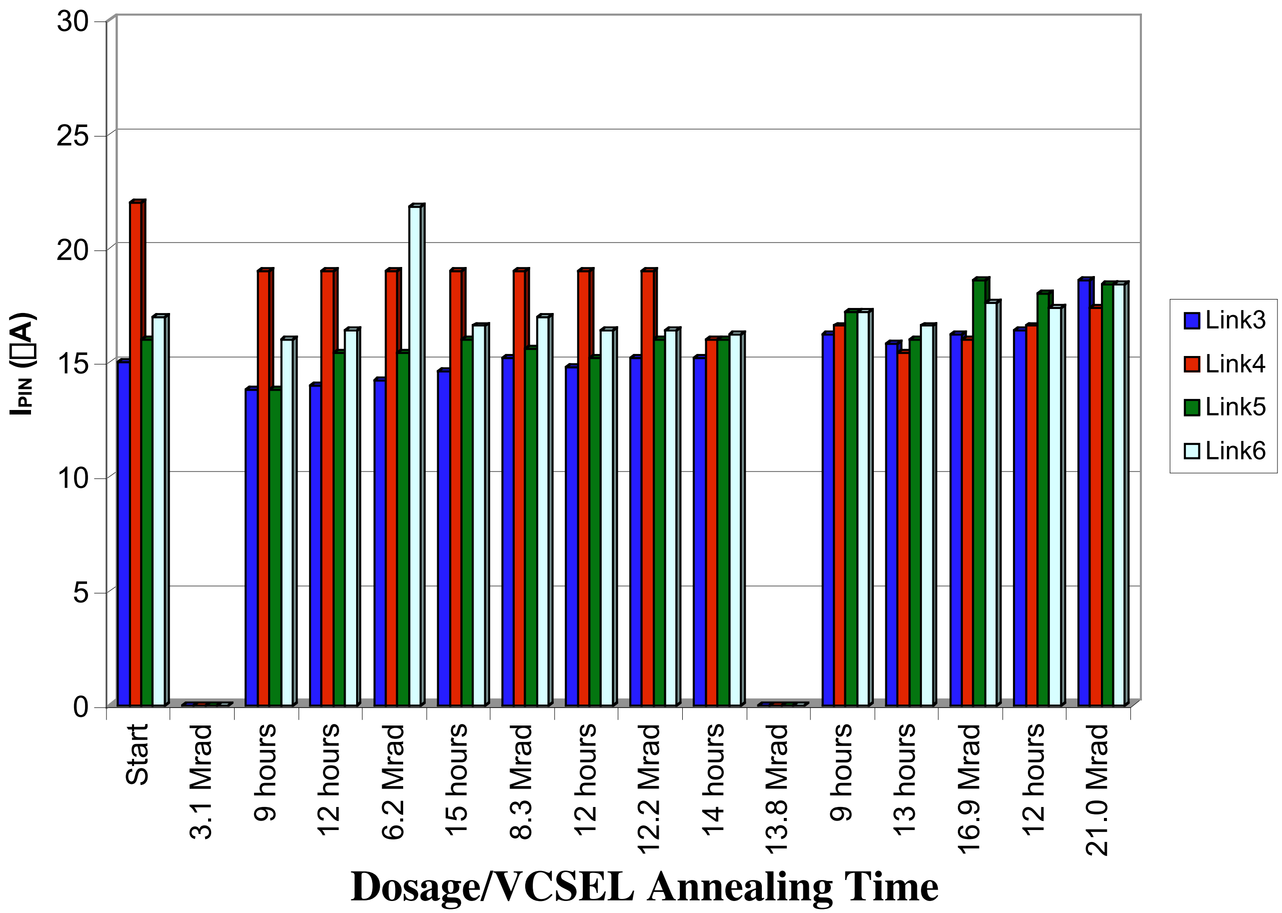


PIN array 4-channel DORIC-I4



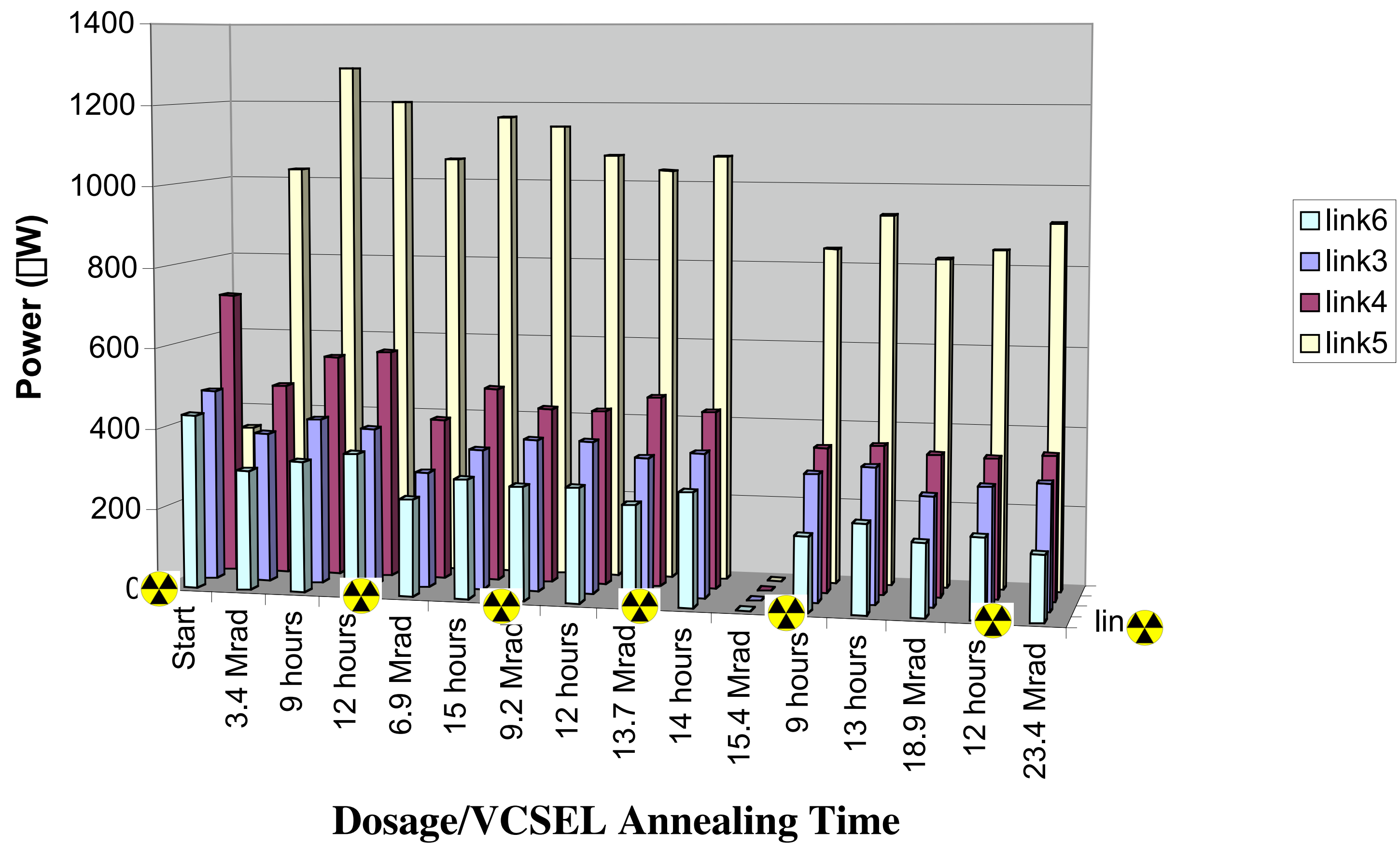
VCSEL array 4-channel VDC-I4

Opto-Board Bit Error Threshold vs. Dosage



- VCSELs annealed with 20 mA during indicated periods
- bit error thresholds remain constant up to 21 Mrad

Opto-Board Optical Power vs. Dosage



- optical power above ATLAS pixel specs

Summary

- VDC-I4 & DORIC-I4 (IBM 0.25 μm) meet ATLAS pixel specs
- opto-link passes ATLAS pixel radiation hardness specs
  ⇨ continue to perform well after 20-58 Mrad!
- next submission: Dec. 2002
  - improve speed & amplitude of common cathode VDC
  - implement common cathode preamp in DORIC