Radiation-Hard Optical Link in the ATLAS Pixel Detector

K.K. Gan The Ohio State University

May 24, 2004

K.E. Arms, K.K. Gan, M. Johnson, H. Kagan, R. Kass, A. Rahimi, C. Rush, S. Smith, R. Ter-Antonian, M.M. Zoeller The Ohio State University

> A. Ciliox, M. Holder, S. Nderitu, M. Ziolkowski <u>Universitaet Siegen, Germany</u>

Outline

Introduction

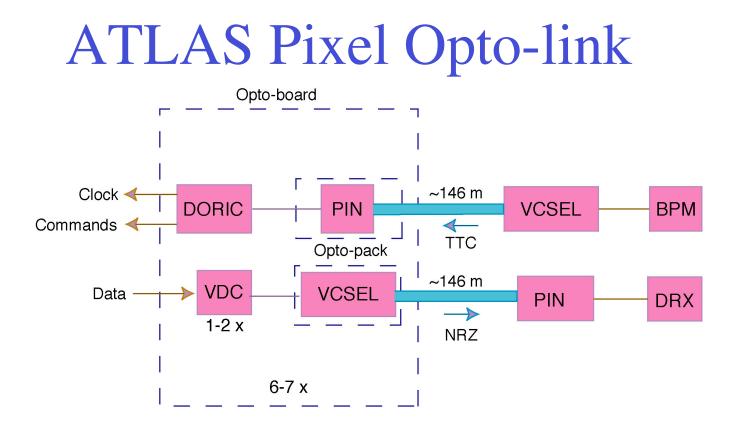
• Results on IBM 0.25 µm Chips

• Results on Proton Irradiations

• Summary

ATLAS Pixel Detector

- Inner most tracking detector
- Pixel size: 50 μm x 400 μm
- 100 million channels
- Barrel layers at r = 5.1, 12.3 cm
- Disks at z = 50, 65 cm
- Dosage after 10 years:
 - optical link: 30 Mrad or 6 x 10¹⁴ 1-MeV n_{eq}/cm^2

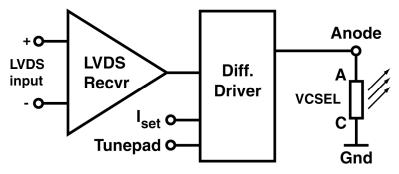


- **VCSEL: Vertical Cavity Surface Emitting Laser diode**
- **VDC: VCSEL Driver Circuit**
- PIN: PiN diode
- **DORIC: Digital Optical Receiver Integrated Circuit**

Siena04

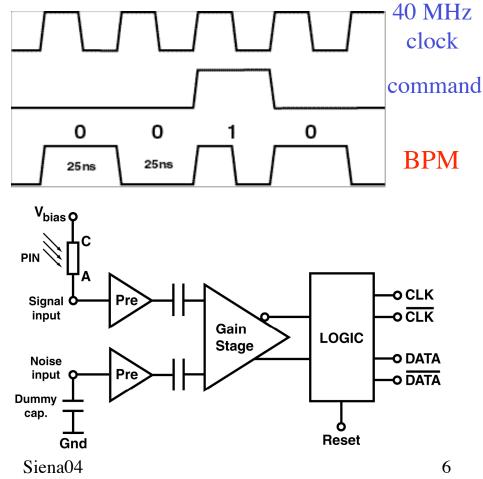
VDC: VCSEL Driver Circuit

- Convert LVDS input signal into single-ended signal appropriate to drive VCSEL diode
- Output (bright) current: 0 to 20 mA
 controlled by external current I_{set}
- Standing (dim) current: ~ 1 mA
 improve switching speed
- Rise & fall times: 1 ns nominal for 80 MHz signals
- "On" voltage of VCSEL: up to 2.3 V at 20 mA for 2.5 V supply
- Constant current consumption!
- use Truelight high-power oxide common cathode VCSEL array



DORIC: Digital Optical Receiver IC

- Decode Bi-Phase Mark encoded (BPM) clock and command signals from PIN diode
- Input signal: 40-600 μA
- Extract: 40 MHz clock
- Duty cycle: $(50 \pm 4)\%$
- Total timing error: < 1 ns
- Bit Error Rate (BER):
 < 10⁻¹¹ at end of life
- use Truelight common cathode PIN array

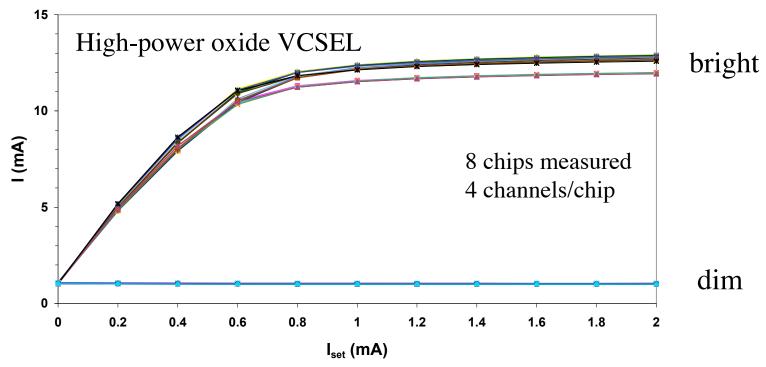


Status of VDC & DORIC

- Original design for ATLAS SemiConductor Tracker (SCT)
 AMS 0.8 µm BiPolar in radiation tolerant process (4 V)
- DMILL #1-3: Summer 1999 May 2001
 - □ 0.8 µm CMOS rad-hard process (3.2 V)
 - □ VDC & DORIC #3: meet specs
 - severe degradation of circuit performance in April 2001 proton irradiation
- IBM #1-5: Summer 2001 Dec 2002
 - \Box 0.25 µm CMOS rad-hard process (2.5 V)
 - □ enclosed layout transistors and guard rings for improved radiation hardness
- IBM 5e: April 2003 engineering run
 - convert 3-layer to 5-layer layout for submission with pixel Module Control Chip (MCC) for cost saving
 - this is the production run since chips meet specs and sufficient quantity of chips were produced

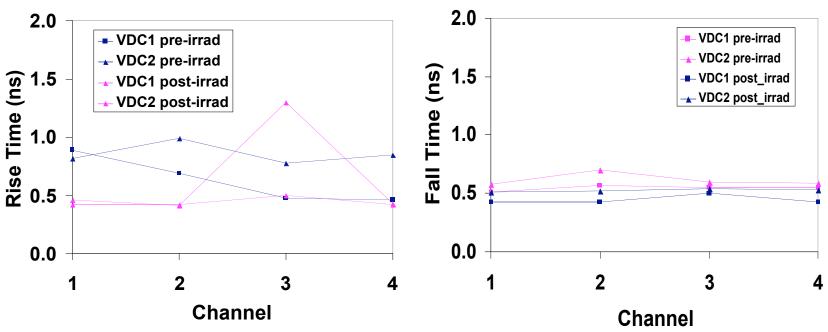
K.K. Gan

VDC-I5e: Bright and Dim Currents vs. I_{set}



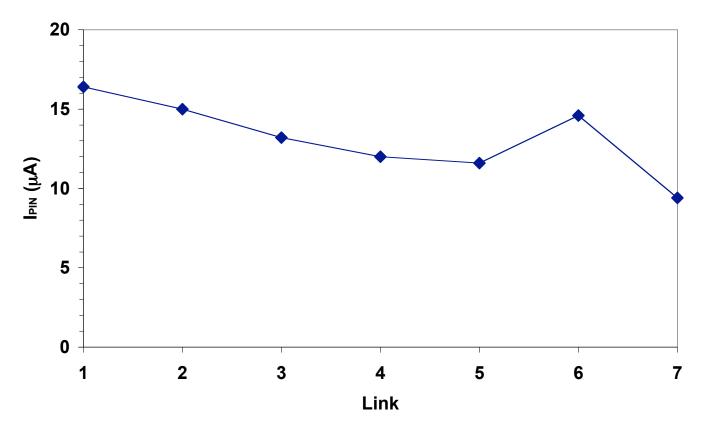
- dim current is ~ 1 mA as expected
- bright current measured with 1 Ω in series
- maximum bright current is ~ 13 mA
 - oxide VCSEL has larger effective resistance than p⁺ implanted VCSEL
 - target is 20 mA but 13 mA is adequate for annealing from irradiation damage

VDC-I5e: Clock Rise/Fall Time



- ✓ fall time < 1 ns
- \times rise time > 1 ns
 - measured with 44-pin package
 - ♦ faster rise time on opto-board
- ✓ no degradation up to 62 M....d

DORIC: PIN Current Thresholds with No Bit Errors

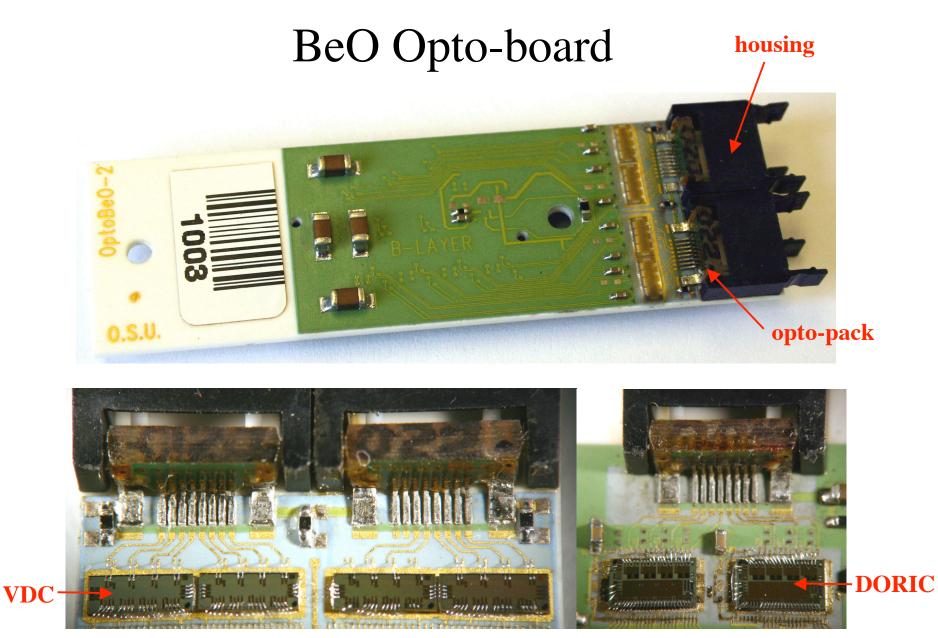


• thresholds significantly better than spec: 40 μ A

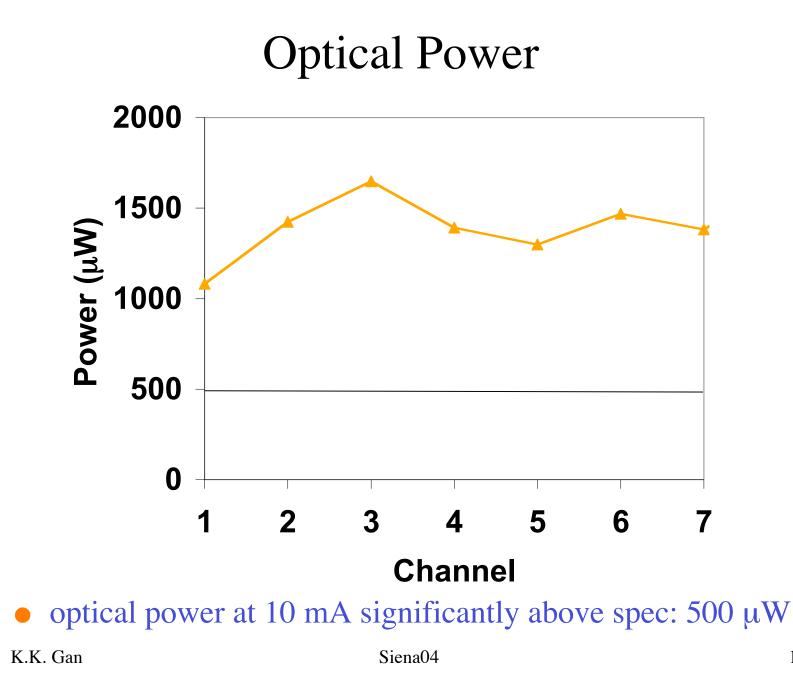
Siena04

Status of BeO Opto-board

- converts: optical signal \leftrightarrow electrical signal
- contains 7 optical links
- use BeO for heat management but prototype initially in FR-4 for fast turnaround and cost saving
- 1st BeO prototype:
 - many open vias due to insufficient gold filling
 - ✓ opto-links works after via repairs!
- 2nd BeO prototype:
 - recycled BeO boards
 - many shorts due to over filling
 - ➡ use more experienced/expensive vendor
 - ➡ produced opto-boards of high quality

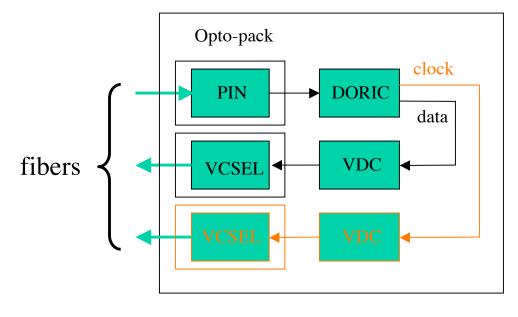






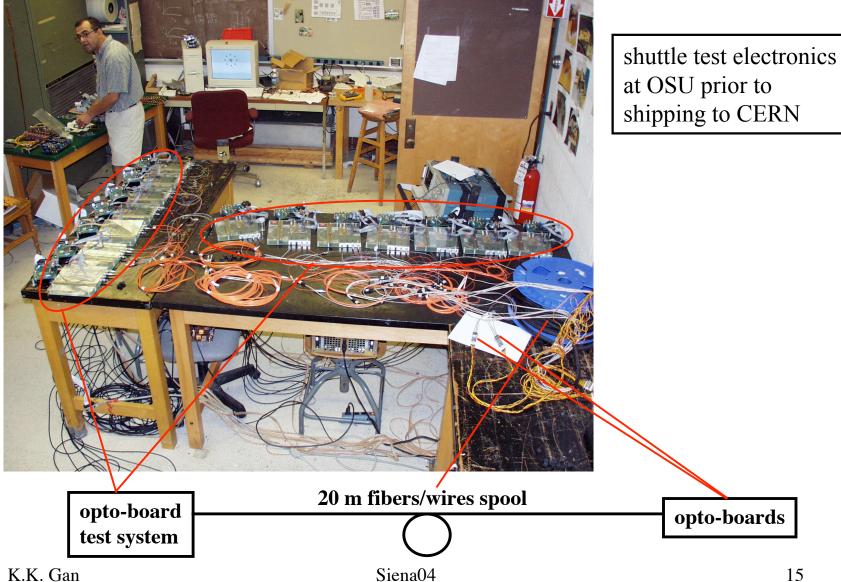
Proton Irradiation at CERN

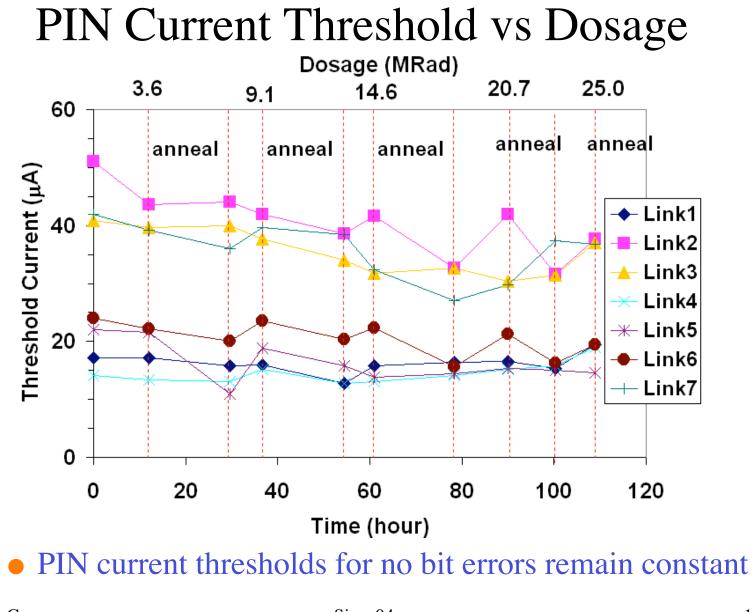
- use 24 GeV protons at T7 to verify radiation hardness of opto-links
- monitor performance of opto-links in real time
- cold box: irradiate 4 VDC-I5e and 4 DORIC-I5e with no optical components
- shuttle: irradiate 4 opto-boards
 - opto-boards can be moved in and out of beam remotely for VCSEL annealing



Siena04

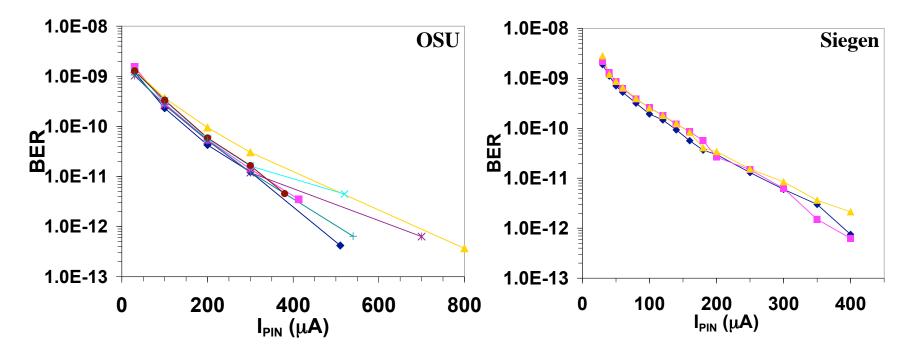
Shuttle Test System





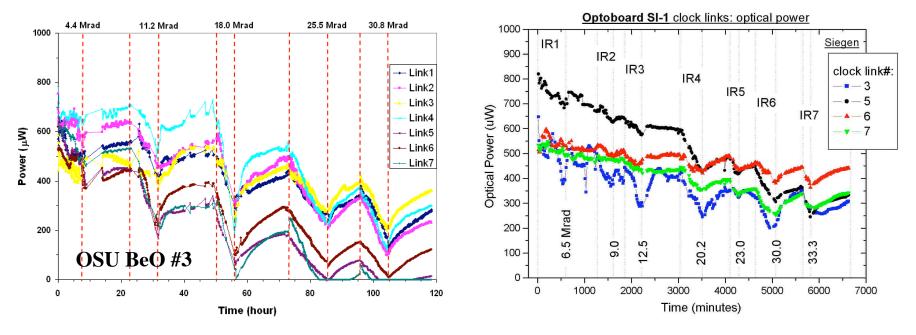
Proton Induced Bit Errors in PIN

• convert observed bit errors into bit error rate at opto-link location:



- bit error rate decreases with increasing PIN current as expected
- bit error rate ~ 3 x 10⁻¹⁰ at 100 µA (1.4 errors/minute)
 DORIC spec: 10⁻¹¹

Optical Power vs Dosage



- irradiation procedure: ~ 5 Mrad/day (6 hours) with the rest of day annealing
- optical power decreases with dosage as expected
- annealing at ~ 13 mA recovers some lost power
- optical power satisfies spec after extended annealing at home institutions

Summary

- VDC-I5e & DORIC-I5e (IBM 0.25 μm):
 - ✓ radiation hard to 62 Mrad
 - ✓ meet ATLAS pixel specs
 - ✓ production is completed
- BeO opto-board:
 - ✓ several pre-production opto-boards have been fabricated
 - □ low PIN current thresholds for no bit errors
 - excellent optical power
- VCSEL lost significant fraction of optical power after irradiation
 power satisfies spec after extended annealing at home institutions
- start opto-link production in July 2004