Optical Link ASICs for LHC Upgrade

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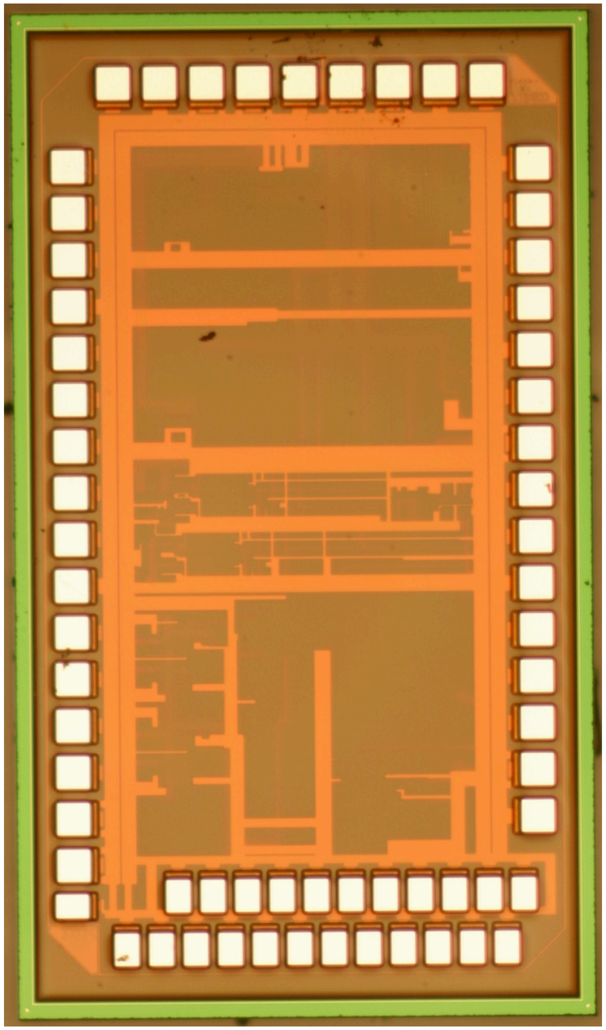
Outline

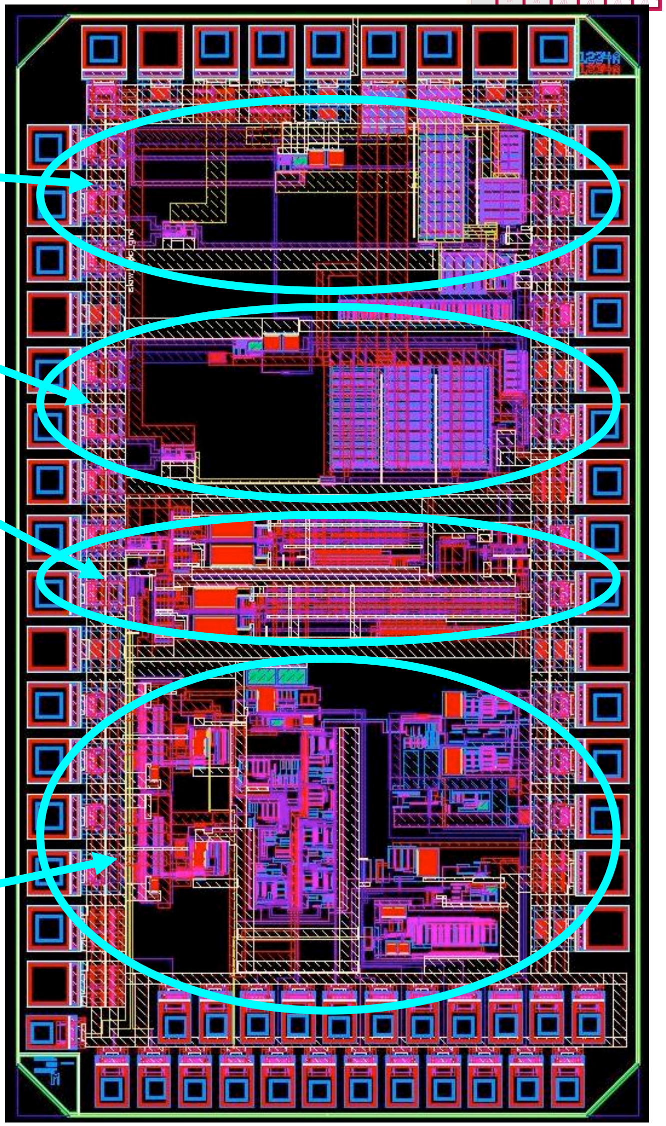
- Introduction
- VCSEL driver chip
- PIN receiver/decoder chip
- Clock multiplier
- Summary

Introduction

- 1st phase of LHC upgrade is planned for 2013:
  - 3 times increase in luminosity to 3×10^{34} cm^{-2}s^{-1}
  - expect significant degradation in the ATLAS pixel detector
  - ⇨ add an insertable barrel layer (IBL) at radius of 3.7 cm
- Possible upgrade for on-detector optical readout system for the IBL:
  - add new functionalities to correct for deficiencies in current system
  - upgrade current optical chips to run at higher speed
  - some of the development could be of interest to SLHC upgrade
  - use 130 nm CMOS 8RF process
  - prototype chips received/irradiated in July/August 2008
  - ⇨ results will be presented below

Opto-Chips





640 Mb/s VCSEL driver

3.2 Gb/s VCSEL driver

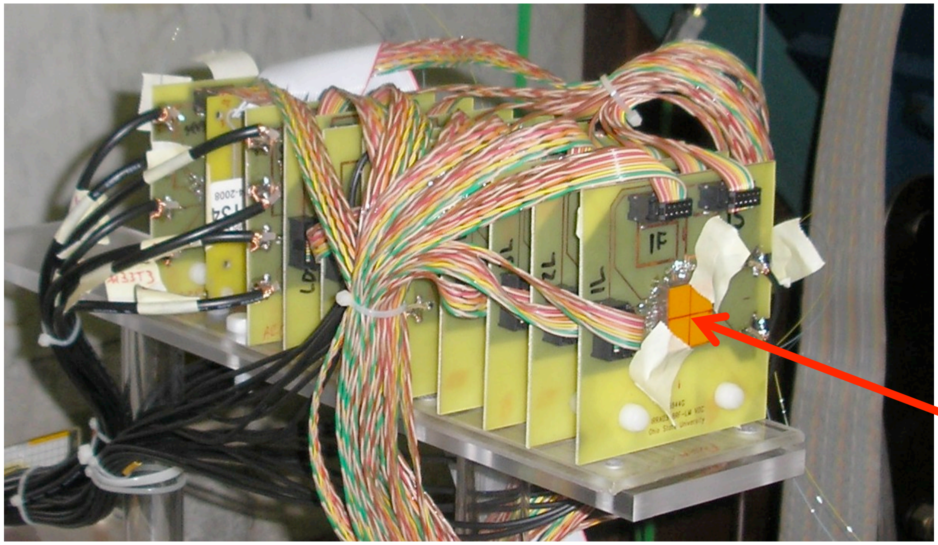
640 MHz clock multipliers
(4 x 160 and 16 x 40 MHz)

PIN receiver/decoder
(40, 160, 320 Mb/s)

2.6 mm x 1.5 mm

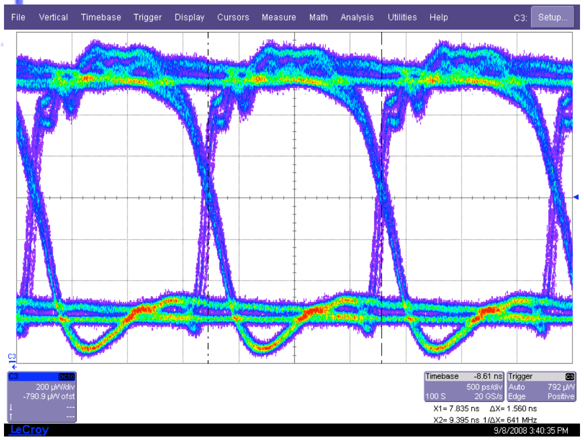
Testing the 130 nm Opto-Chips

- chips were tested in the lab at Ohio State University
- chips were irradiated with 24 GeV protons to SLHC dose at CERN
  - 8 VCSEL drivers: 4 “slow” + 4 “fast”
  - 4 PIN receiver/decoder (purely electrical testing)
  - 4 PIN receiver/decoder coupled to PIN
  - 4 clock multiplier
  - long cables limited testing of driver/receiver to 40 Mb/s
  - special designed card allows testing of clock multiplier at 640 MHz



protons

VCSEL Driver Chip



C3 200 μW/div
-790.9 μW ofst
Timebase -8.61 ns
500 ps/div
100 S 20 GS/s
Trigger Auto 792 μW
Edge Positive
X1= 7.835 ns ΔX= 1.560 ns
X2= 9.395 ns 1/ΔX= 641 MHz
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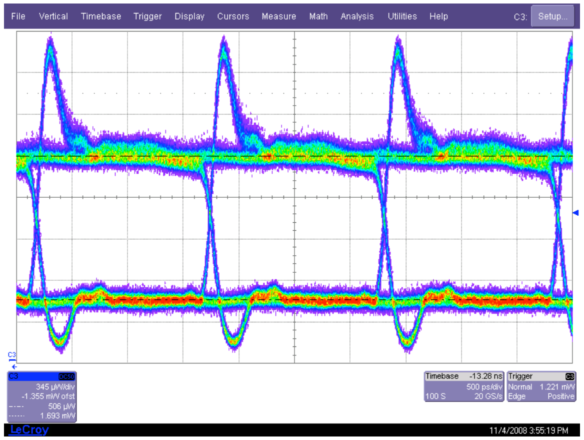
Slow VDC

640 Mb/s

~ 14 mA max



C3 345 μW/div
-1.355 mW ofst
506 μW
1.693 mW
Timebase -13.28 ns
500 ps/div
100 S 20 GS/s
Trigger Normal 1.221 mW
Edge Positive
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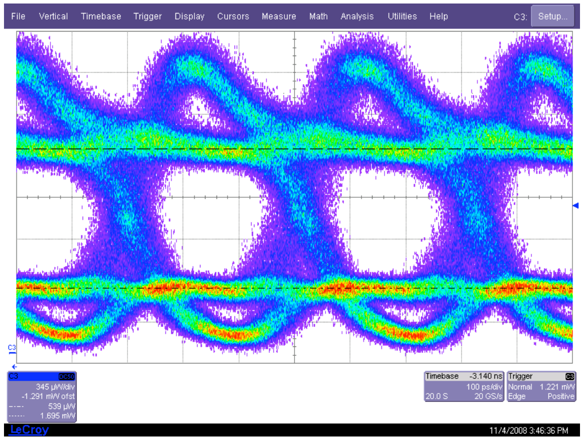
Fast VDC

640 Mb/s

~ 9 mA max



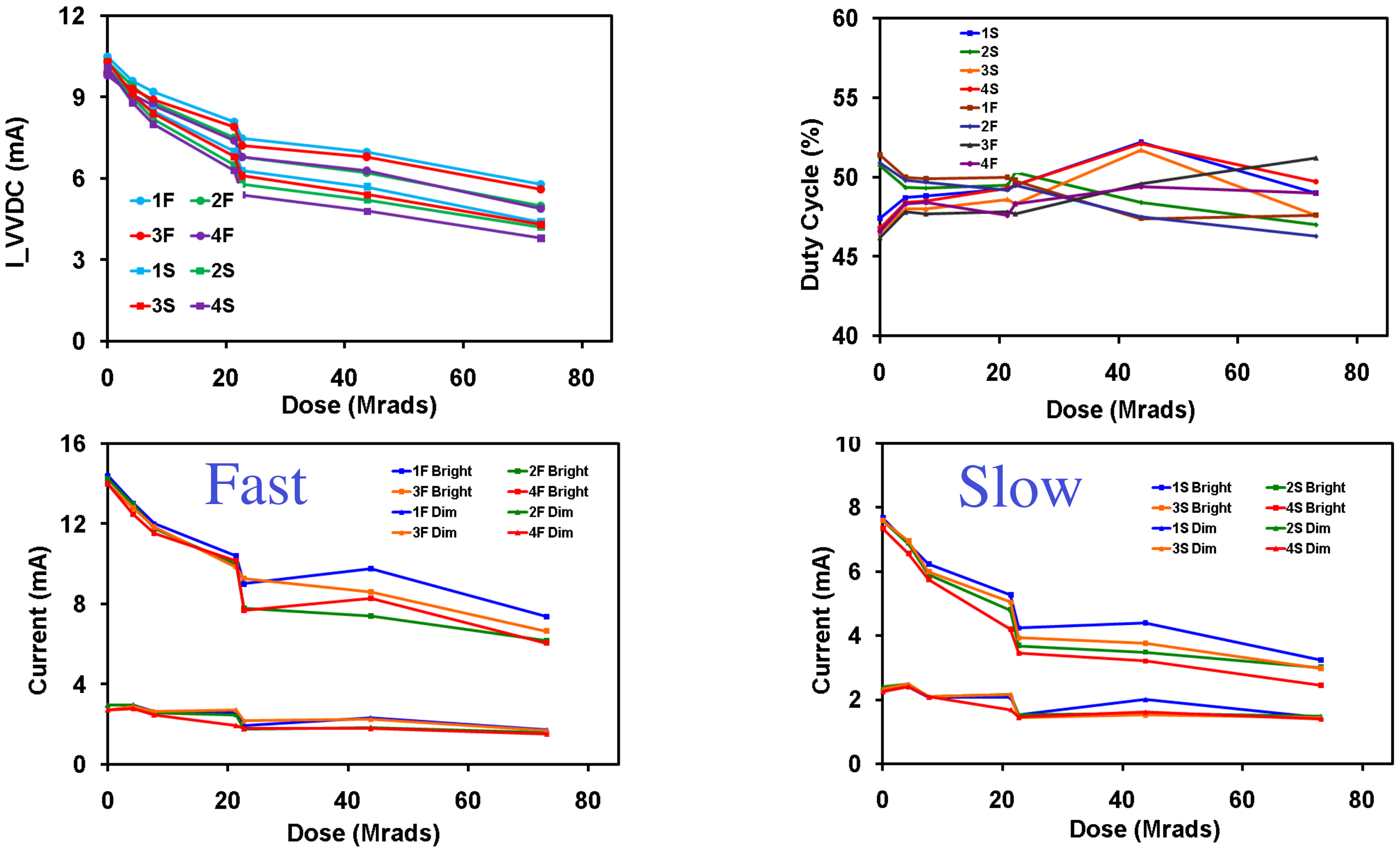
C3 345 μW/div
-1.291 mW ofst
539 μW
1.695 mW
Timebase -3.140 ns
100 ps/div
20.0 S 20 GS/s
Trigger Normal 1.221 mW
Edge Positive
11/4/2008 3:46:36 PM

Fast VDC

3.2 Gb/s

- both slow/fast chips are working
- LVDS receiver/VCSEL driver work at high speed
  - BER < 10^{-13} @ 4 Gb/s using 10 Gb/s AOC VCSEL

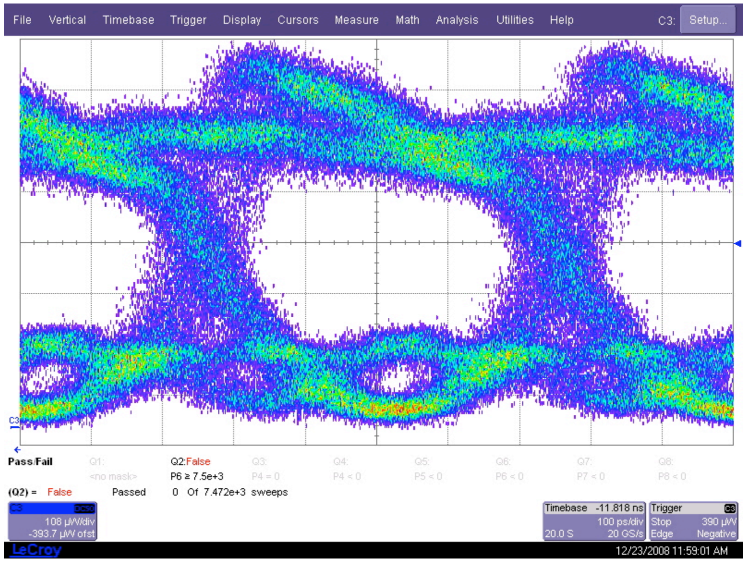
VDC Irradiation



- VDC driving 25 Ω with constant control current (Iset)
- drive current decreases with radiation for constant Iset
  - driver circuit fabricated with thick oxide process

Unirradiated vs. Irradiated VDC

Unirradiated



```
Pass/Fail     Q1:          Q2:False      Q3:      Q4:      Q5:      Q6:      Q7:      Q8:
              <no mask>    P6 ≥ 7.5e+3   P4 = 0   P4 < 0   P5 < 0   P6 < 0   P7 < 0   P8 < 0
(Q2) =  False     Passed    0  Of  7.472e+3  sweeps
C3  DC50                           Timebase  -11.818 ns   Trigger    C3
  108 µW/div                                 100 ps/div   Stop   390 µW
  -393.7 µW ofst                   20.0 S    20 GS/s      Edge   Negative
                                                    12/23/2008 11:59:01 AM
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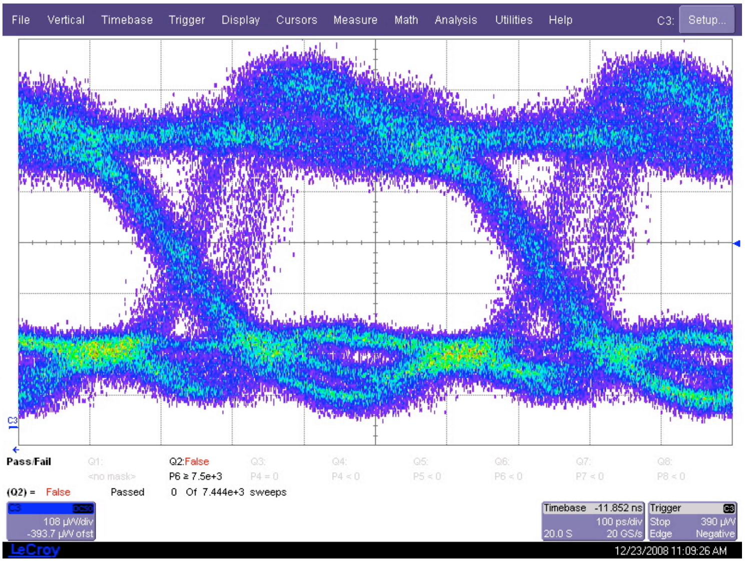
2 Gb/s

Irradiated



```
Pass/Fail     Q1:          Q2:False      Q3:      Q4:      Q5:      Q6:      Q7:      Q8:
              <no mask>    P6 ≥ 7.5e+3   P4 = 0   P4 < 0   P5 < 0   P6 < 0   P7 < 0   P8 < 0
(Q2) =  False     Passed    0  Of  7.444e+3  sweeps
C3  DC50                           Timebase  -11.852 ns   Trigger    C3
  108 µW/div                                 100 ps/div   Stop   390 µW
  -393.7 µW ofst                   20.0 S    20 GS/s      Edge   Negative
                                                    12/23/2008 11:09:26 AM
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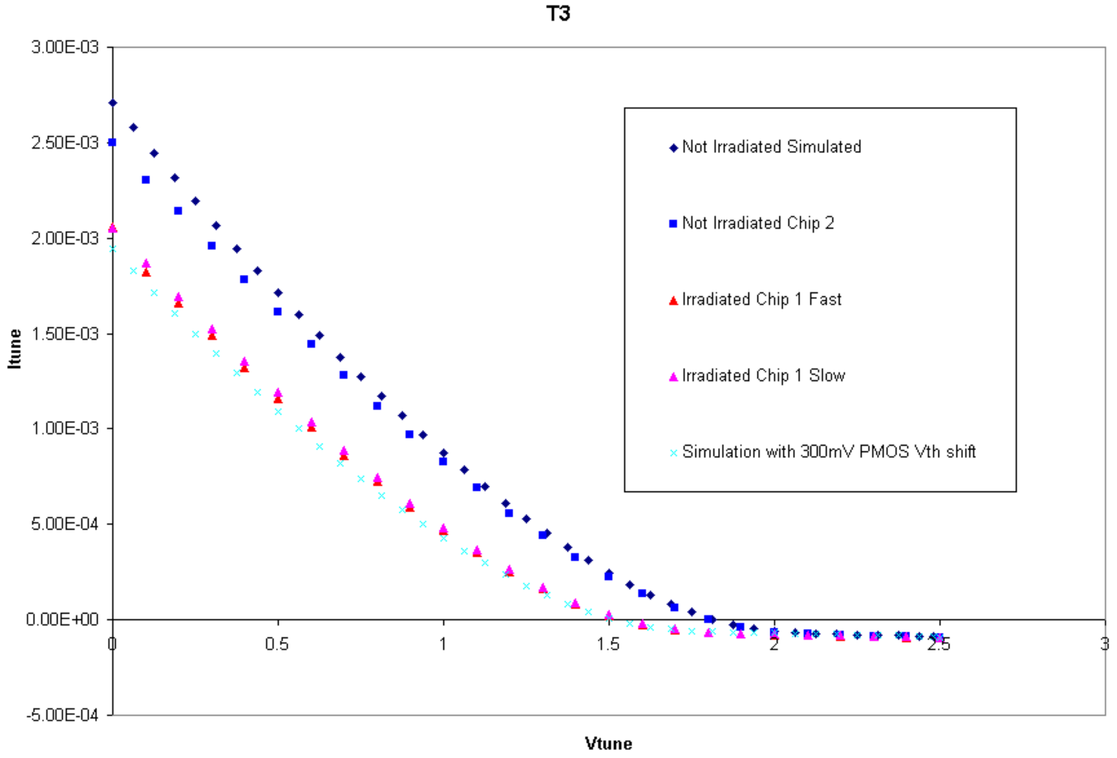
- VDC driving 2.5 Gb/s Optowell VCSEL
- Possible to obtain similar eye diagram by adjusting control currents
  - radiation induced changes in control current circuitry

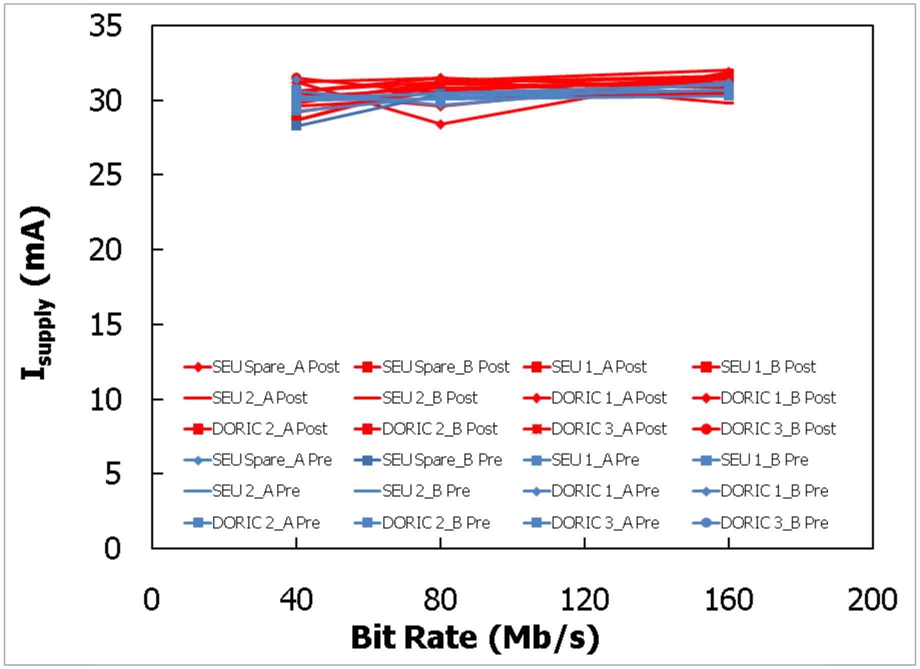
Threshold Shift in Irradiated PMOS

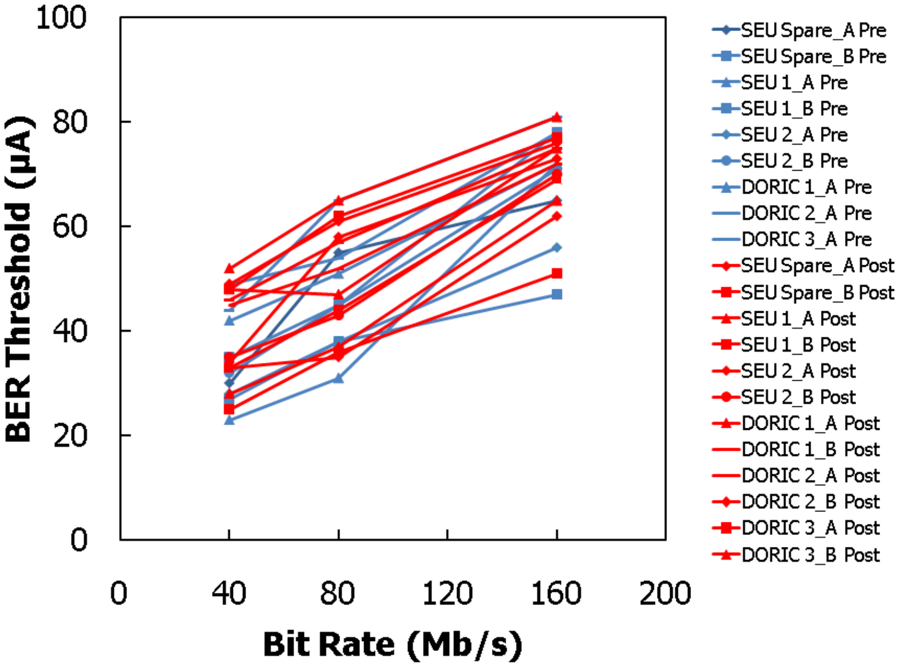


- Have access to two transistors for characterization
  - simulation with 300 mV threshold shift reproduces observed V vs. I
  - PMOS and NMOS have different threshold voltage shifts
  - ⇨ will use only PMOS in the current mirror

Receiver/Decoder Chip

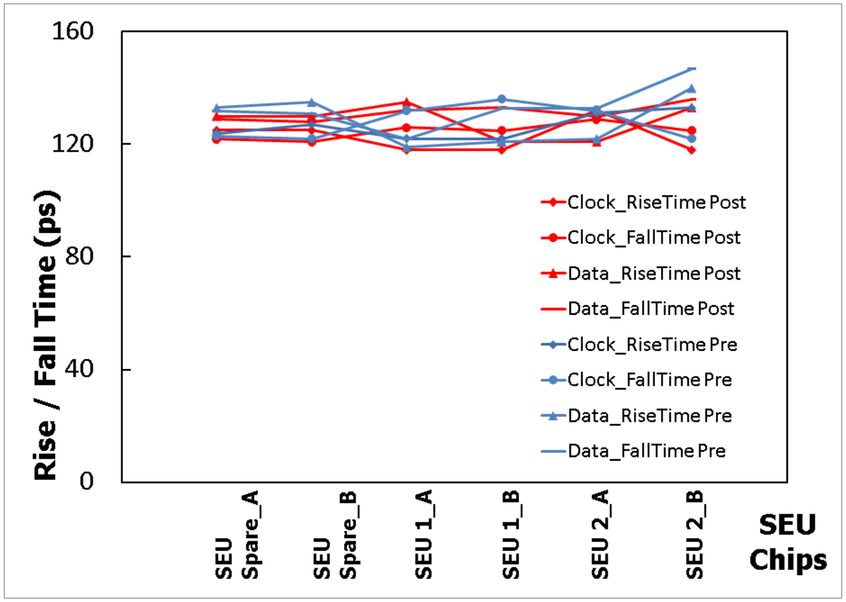
- Designed to operate at 40, 160, and 320 Mb/s
  - can only achieve 250 Mb/s due to lack of time before submission
  - no significant degradation up to SLHC dose

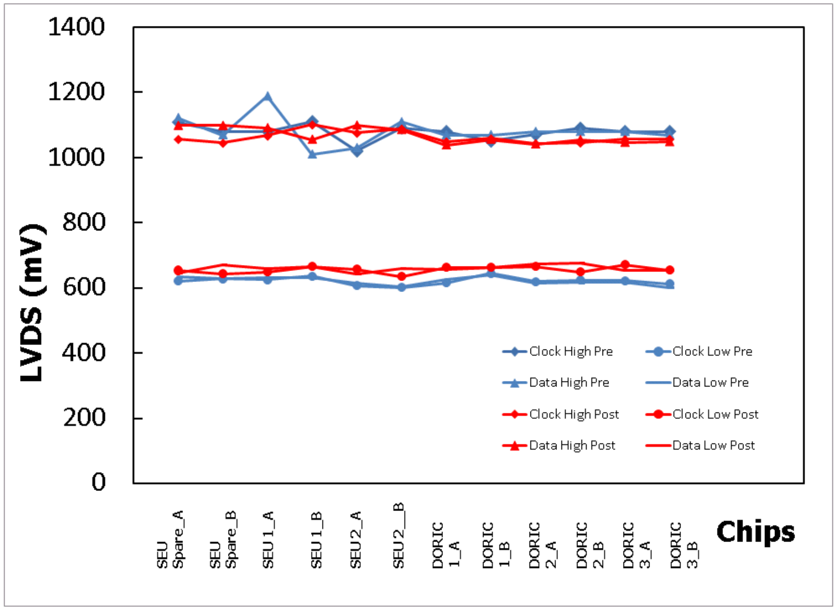




Low Voltage Differential Driver

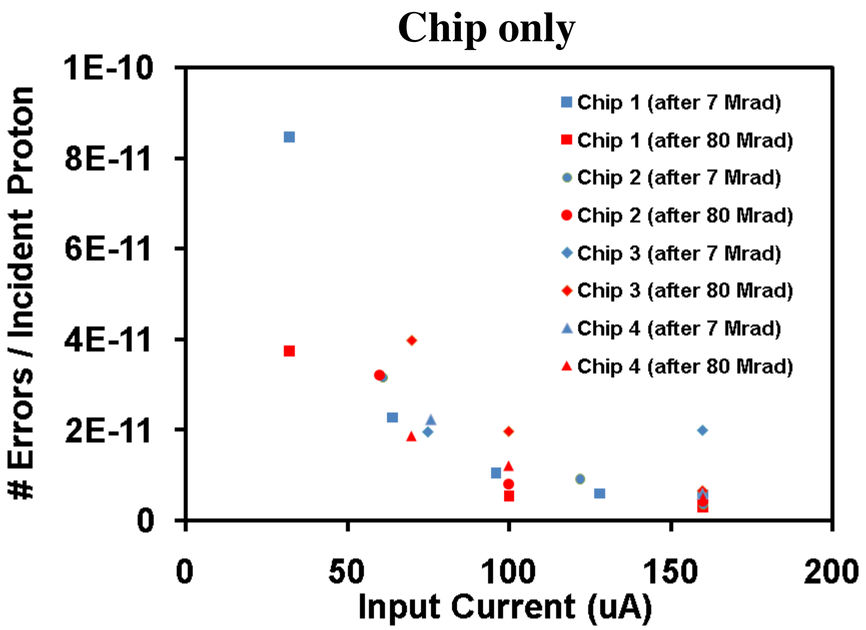
- output has fast rise and fall times
- output has proper amplitude and baseline
  - ◆ small clock jitter, e.g. < 50 ps (1%) @ 160 MHz
  - ◆ no significant degradation up to SLHC dose

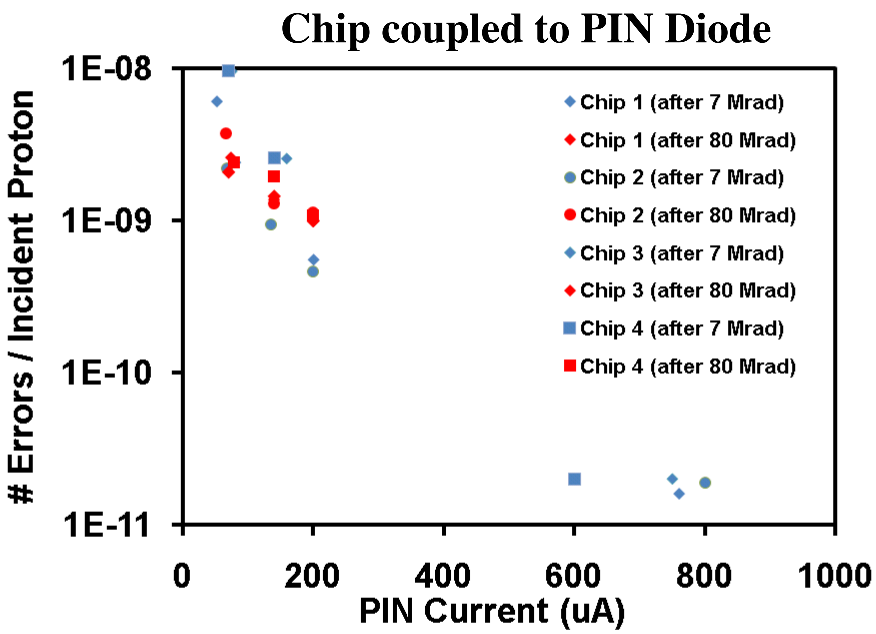




Single Event Upset

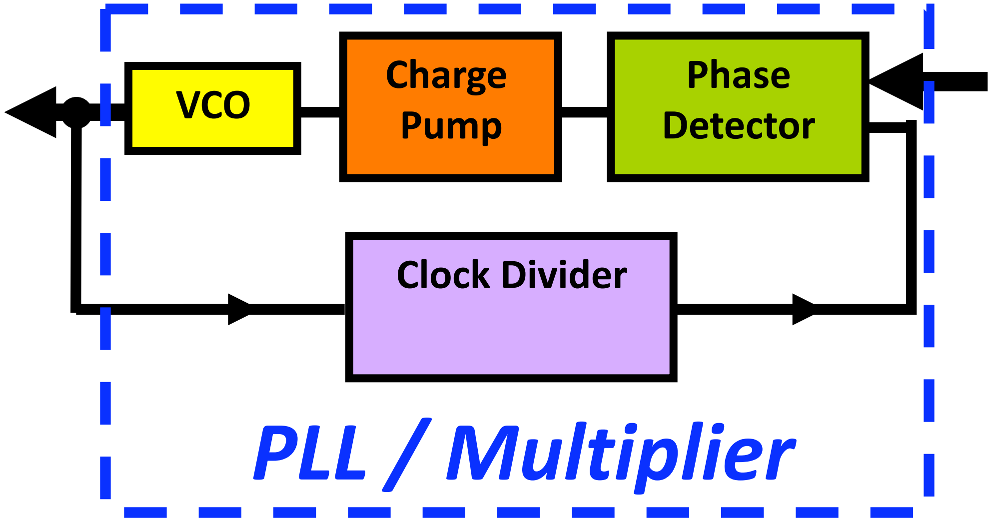
- Single event upset (SEU) measured with receiver/decoder coupled to a Taiwan PIN for 40 Mb/s operation
  - SEU rate much higher for chip coupled to PIN as expected
  - no significant degradation with radiation observed


Chip only


Chip coupled to PIN Diode

Clock Multiplier

- clock multiplier needed to serialize high speed data
- both 4 x 160 MHz and 16 x 40 MHz clock multipliers work
  - use of recovered clock as input does not increase jitter



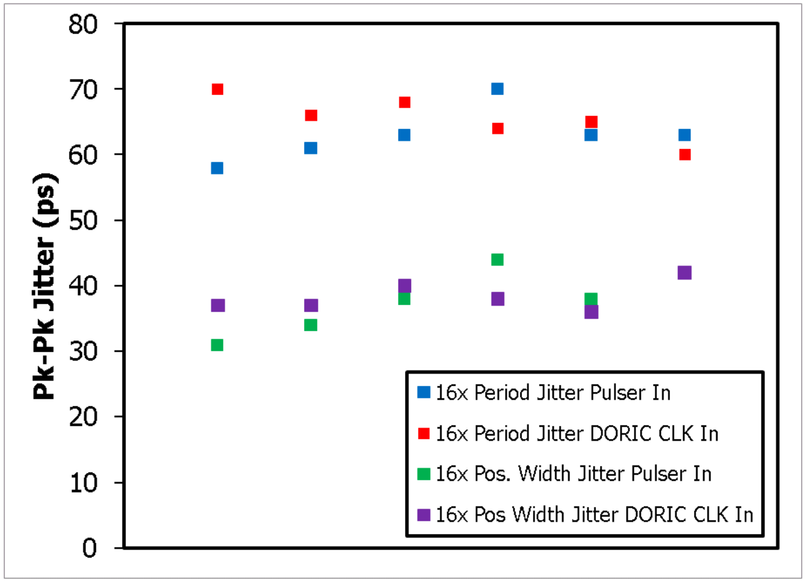
VCO

Charge Pump

Phase Detector

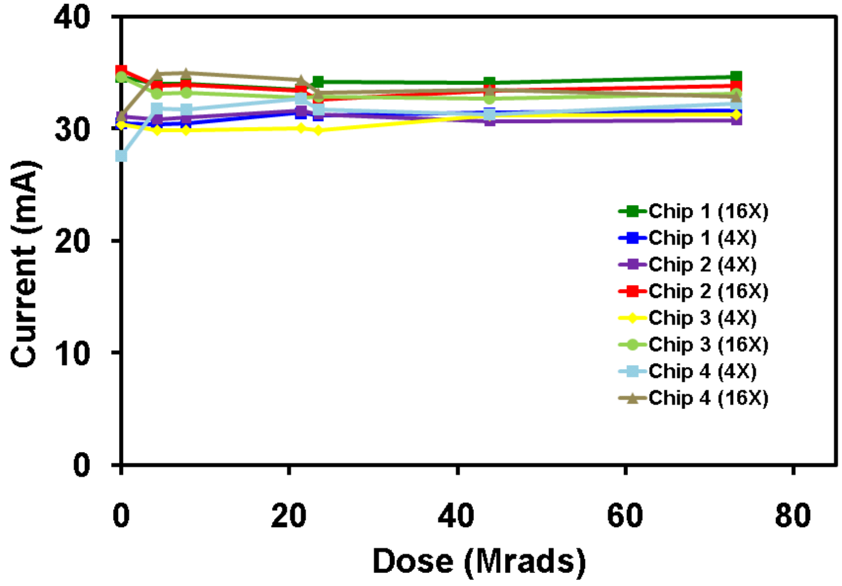
Clock Divider

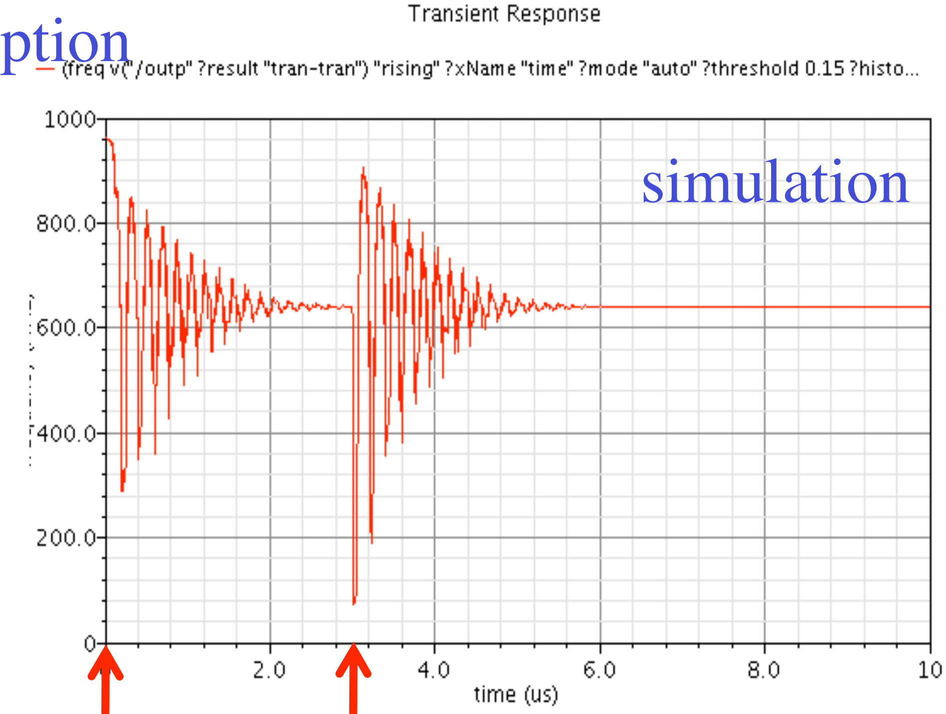
PLL / Multiplier



Clock Multiplier

- SEU in PIN coupled to data/clock decoder disturbed the input clock
  - ➪ observation confirmed with simulation
  - ◆ output clock takes ~ 3 μs to recover
  - ◆ two of the four chips lost lock during irradiation
    - ❑ need power cycling to resume operation at 640 MHz
  - ◆ no change in current consumption





Summary

- first 130 nm submission mostly successful
- no significant degradation up to 73 Mrad
  - observe threshold shift in thick oxide transistor
- aim for next iteration in Spring 2009 with new functionalities
  - individual control of VCSEL currents
  - redundancy: ability to bypass a bad VCSEL/PIN channel