Results on Opto-Link R&D

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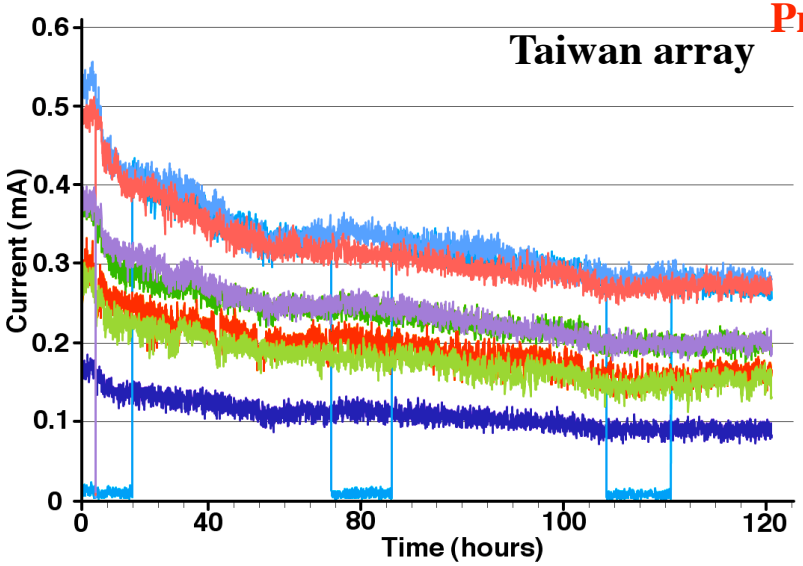
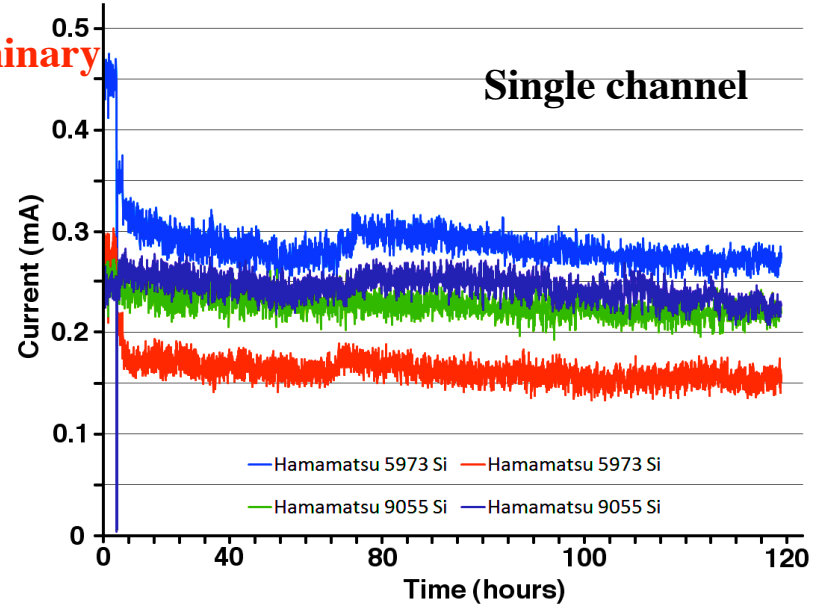
Outline

- Radiation hardness of PIN arrays
- Radiation hardness of VCSEL arrays
- Study of opto-chips
- Summary

Radiation-Hardness of Silicon PIN



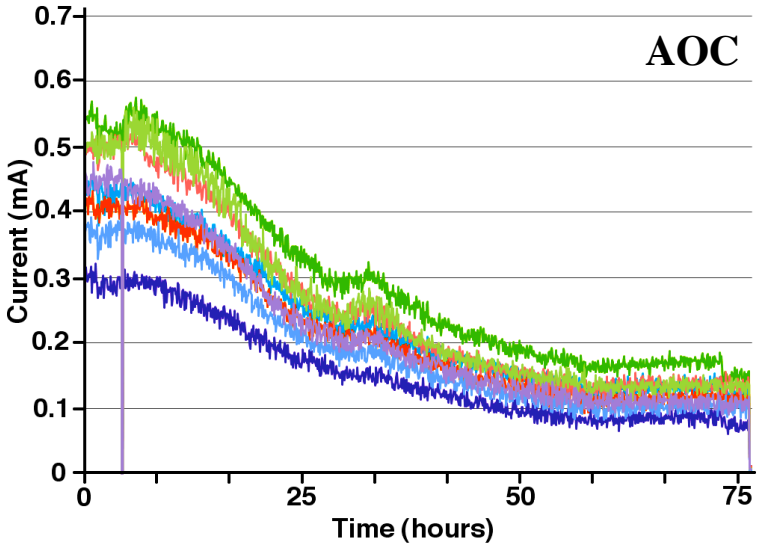
Preliminary

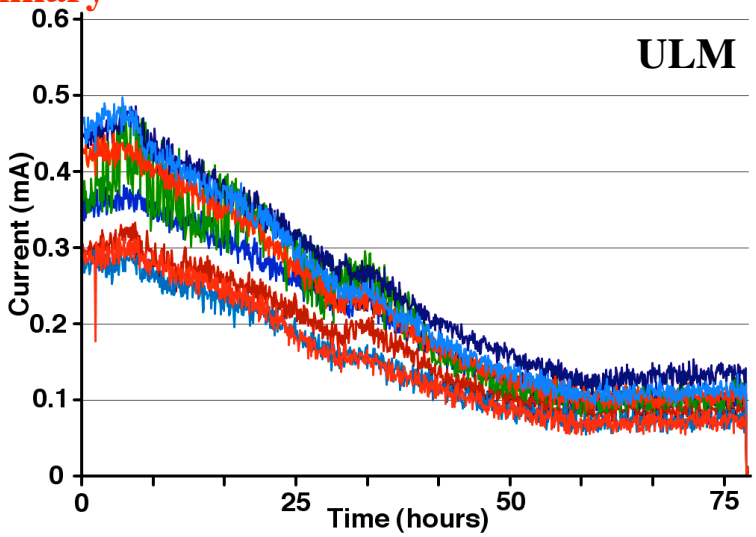


- irradiate PIN with 24 GeV protons at CERN
  - SLHC dosage: 2.6 x 10^{15} p/cm^2 (1.5 x 10^{15} 1-MeV n_{eq}/cm^2)
  - 2007 irradiation with 60% higher dosage:
    - Taiwan array responsivity (A/W): decrease by a factor of 3
  - 2008 irradiation with SLHC dosage:
    - Taiwan array responsivity: decrease by a factor of 2
    - Hamamatsu device responsivity: decrease somewhat less

Radiation-Hardness of GaAs PIN

Preliminary

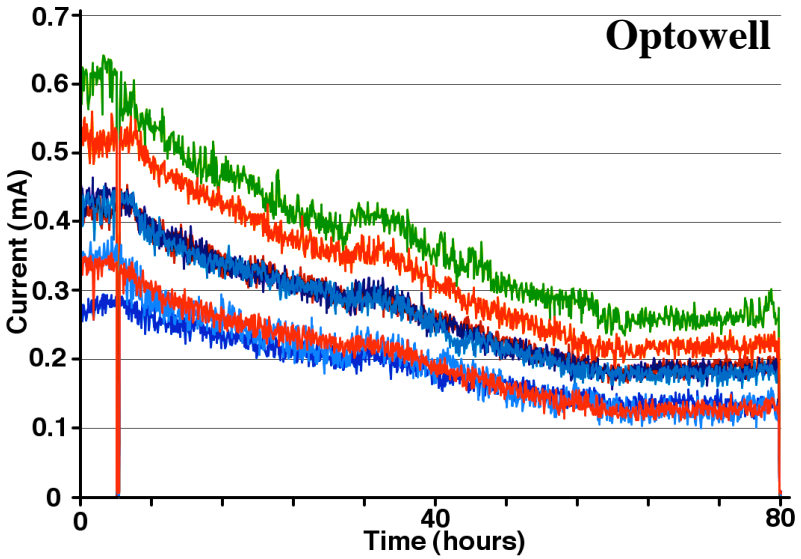


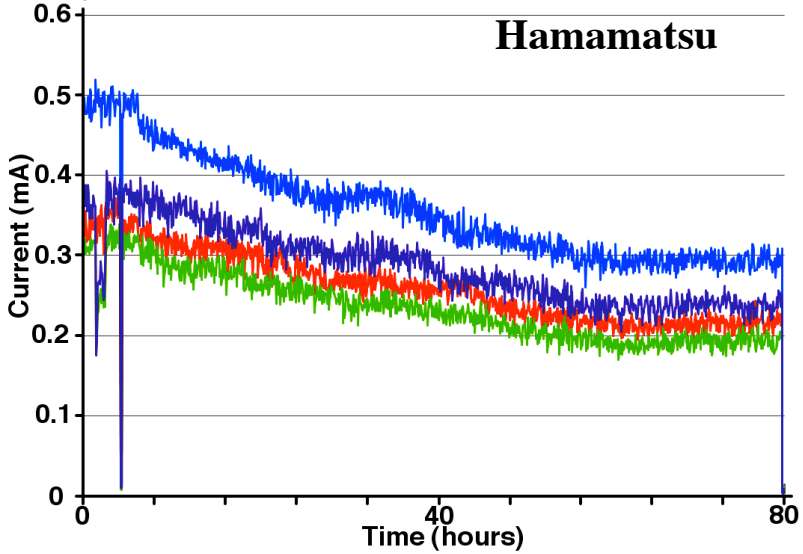


- irradiate PIN with 24 GeV protons at CERN
  - SLHC dosage: 2.6 x 10^{15} p/cm^2 (8.2 x 10^{15} 1-MeV n_{eq}/cm^2)
  - 2007 irradiation with 60% higher dosage:
    - responsivity: decrease by a factor of 10
  - 2008 irradiation with SLHC dosage:
    - responsivity: decrease by a factor of 2-4

Radiation-Hardness of GaAs PIN

Preliminary



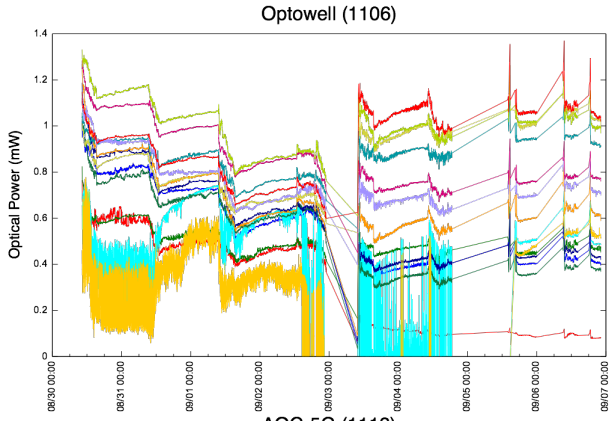


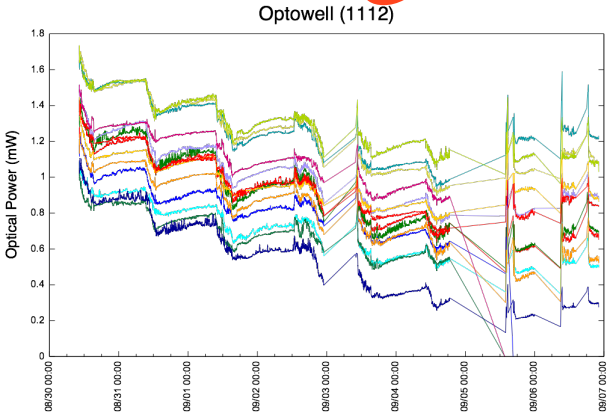
- 2007 irradiation with 60% higher dosage:
  - Optowell responsivity: decrease by a factor of 10
- 2008 irradiation with SLHC dosage:
  - Optowell responsivity: decrease by a factor of ~2
  - Hamamatsu responsivity: decrease by a factor of ~1.6

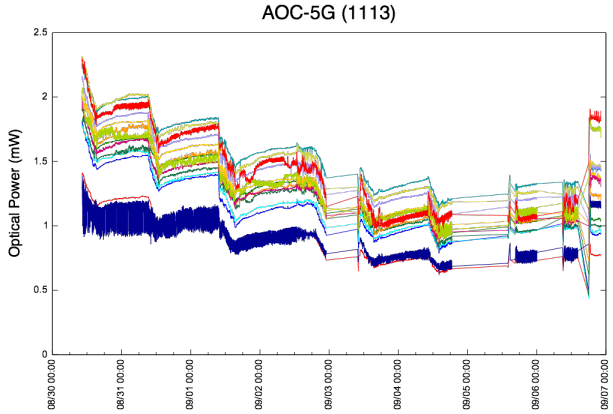
Radiation-Hardness of PIN

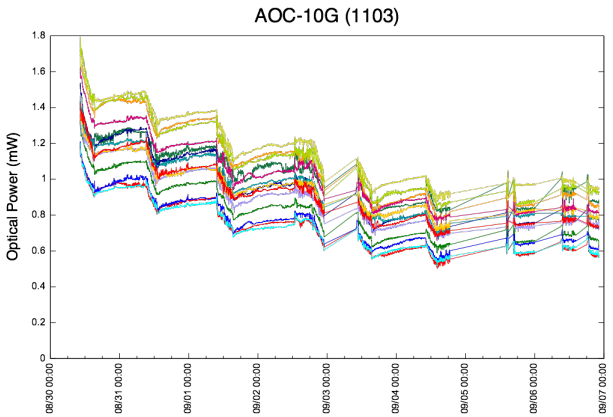
	Gb/s	Responsivity (A/W)	
GaAs		Pre	Post
ULM	4.25	0.50	0.13
AOC	2.5	0.60	0.19
Optowell	3.125	0.60	0.25
Hamamatsu G8921	2.5	0.50	0.32
Si			
Taiwan	1.0	0.55	0.33
Hamamatsu S5973	1.0	0.47	0.37
Hamamatsu S9055	1.5/2.0	0.25	0.21

VCSEL Power vs Dosage









- 2007 irradiation with 60% higher dosage:
  - close to zero power on some channels
- 2008 irradiation with SLHC dosage:
  - AOC(5 & 10 G) have good power

Opto-Chips

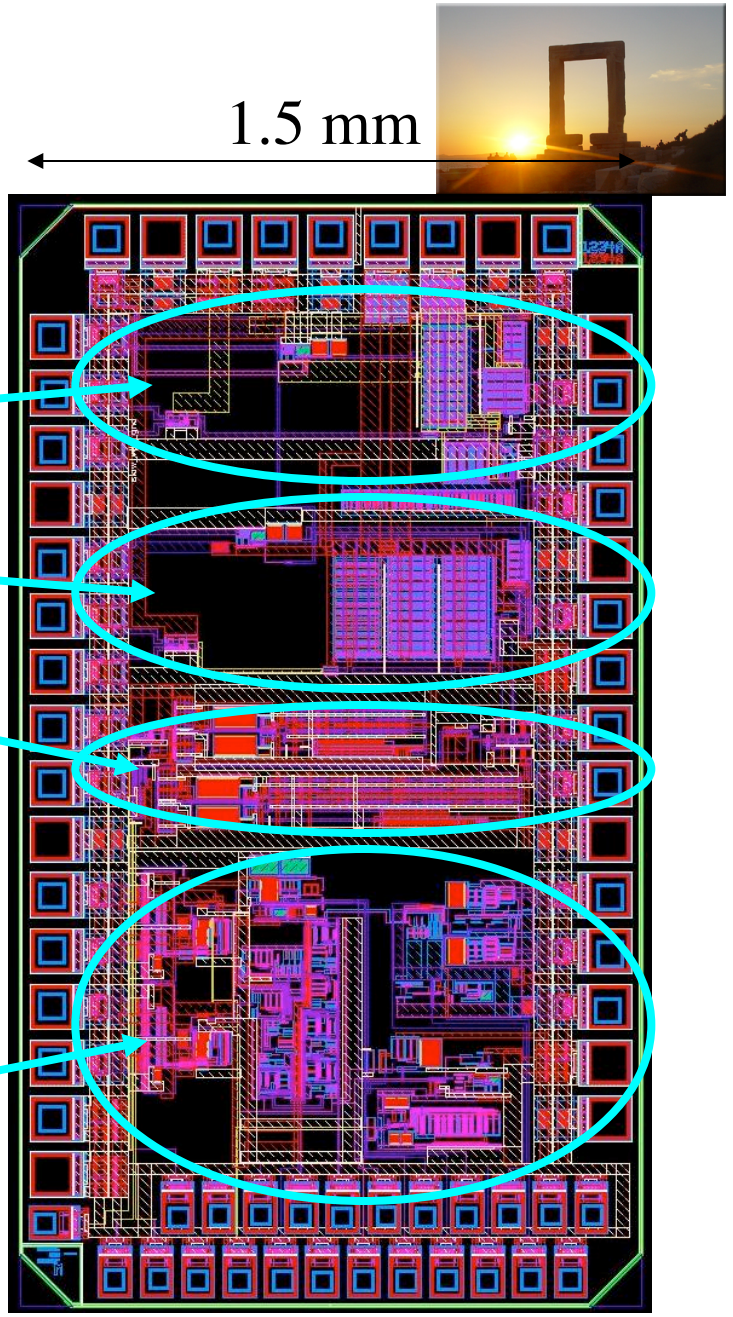
0.13 μm

640 Mb/s VCSEL Driver

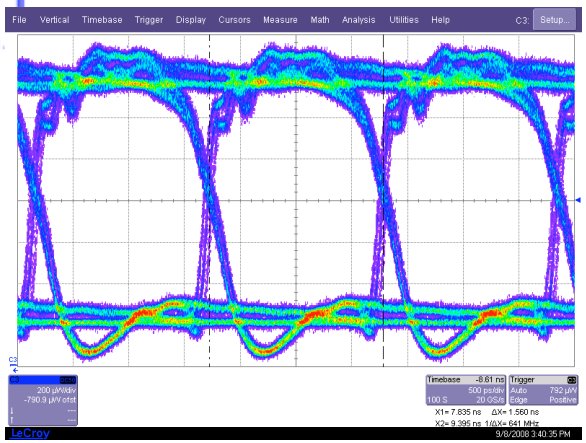
3.2 Gb/s VCSEL Driver

640 MHz clock multipliers
(4 x 160 and 16 x 40 MHz)

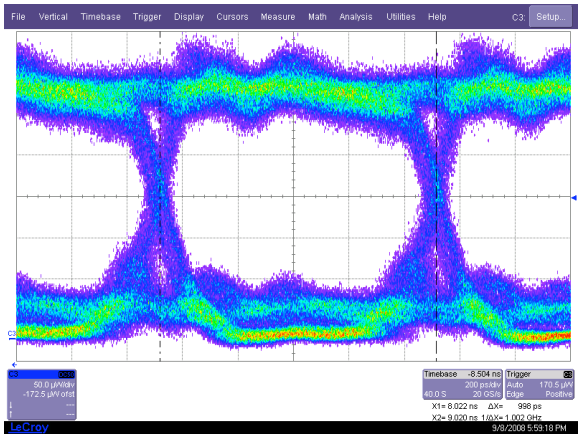
PIN receiver/decoder
(40, 160, 320 MHz)



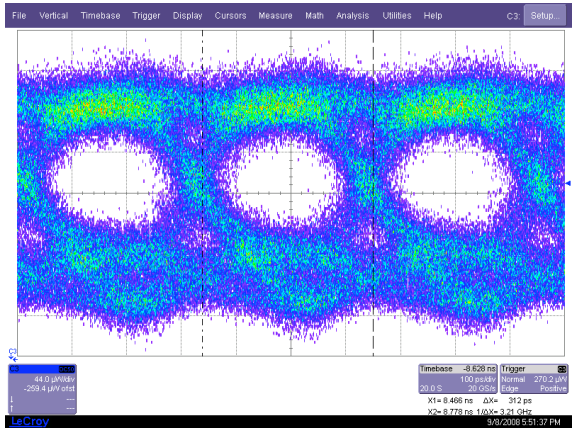
VCSEL Driver Chip



Slow VDC
640 Mb/s

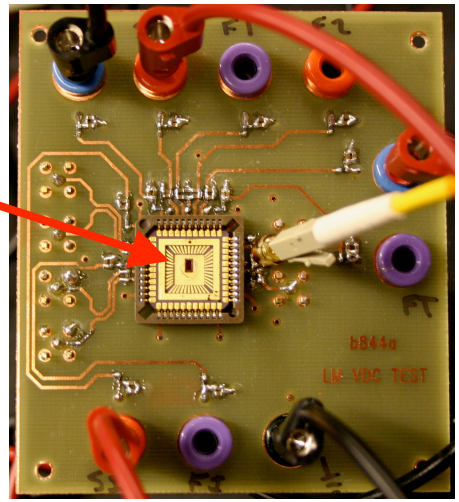


Fast VDC
1 Gb/s



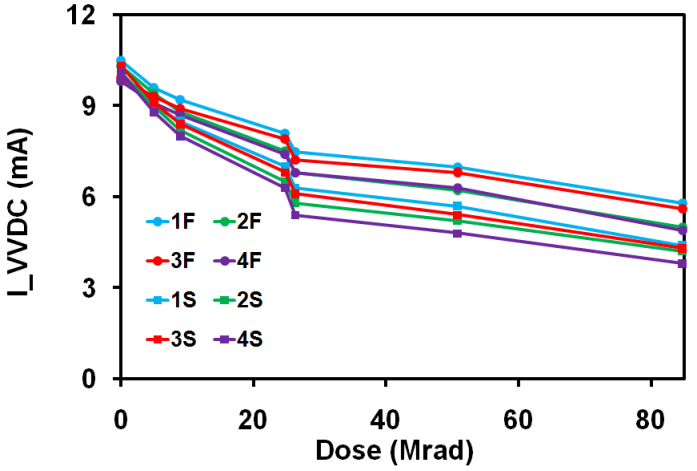
Fast VDC
3.2 Gb/s

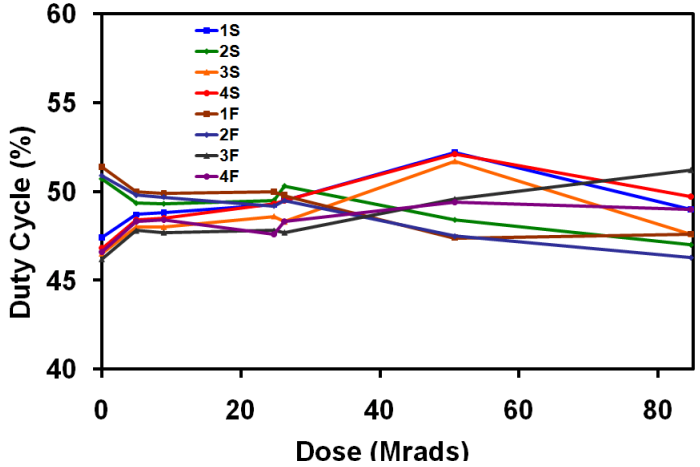
PLCC
package

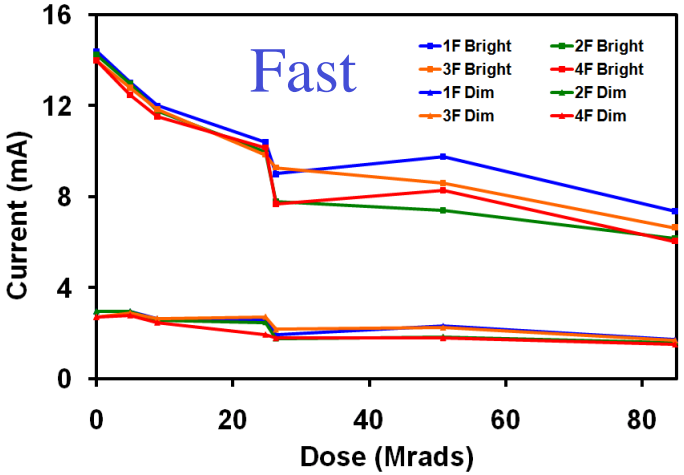


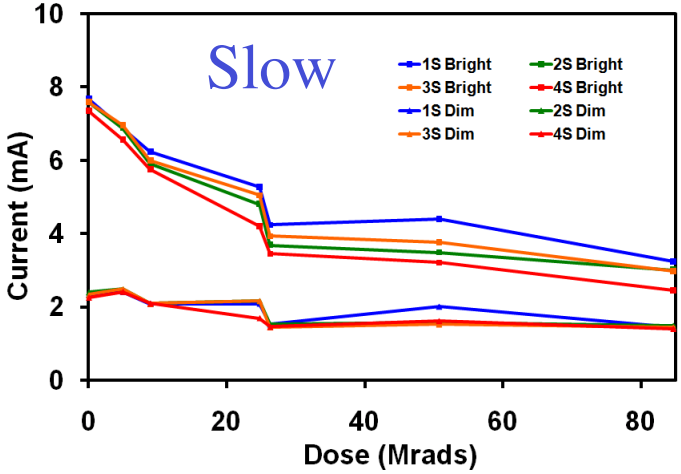
- both chips are working in preliminary study
- LVDS receiver working at high speed
- need detailed study without package

VDC Irradiation





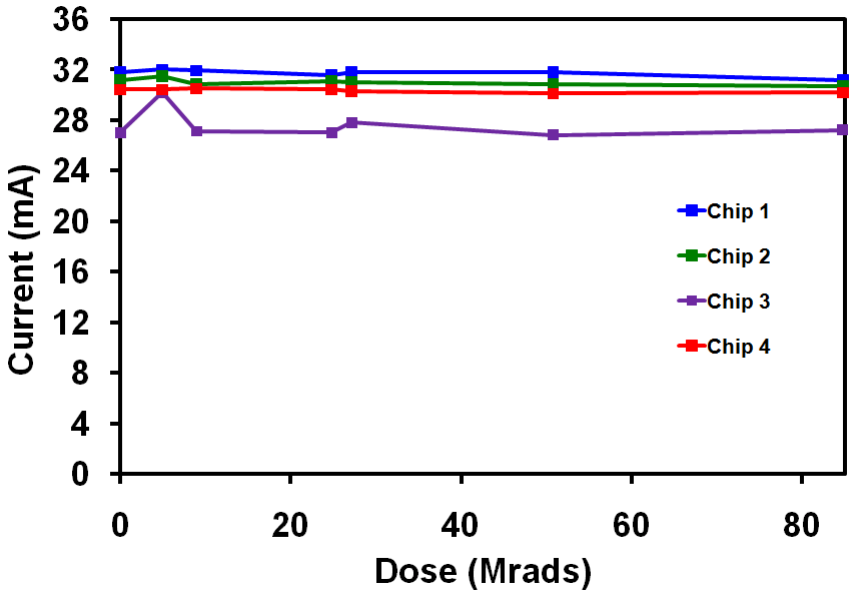




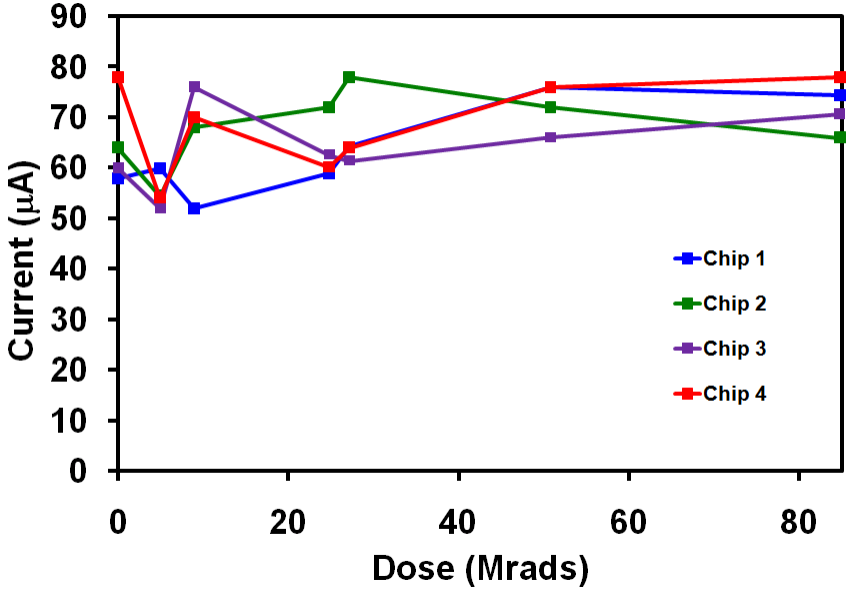
- drive current decreases with radiation for constant ISET
- need detailed study after cool down

Receiver/Decoder Chip

- Properly decode 40, 80, and 160 Mb/s signals but not 320 Mb/s
  - LVDS-like output has proper amplitude and baseline
  - small clock jitter (e.g. < 50 ps @ 160 MHz)
  - no significant degradation after irradiation

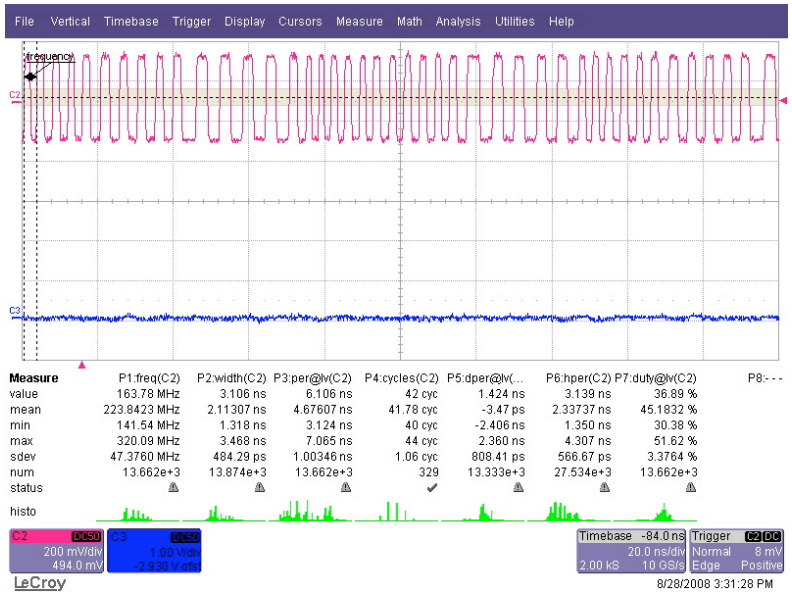


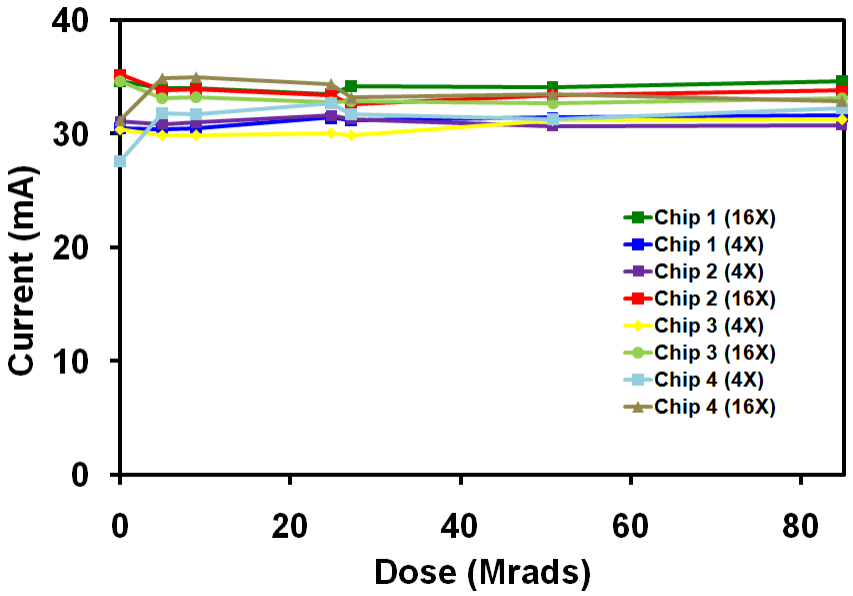
Threshold for 1 bit error/s



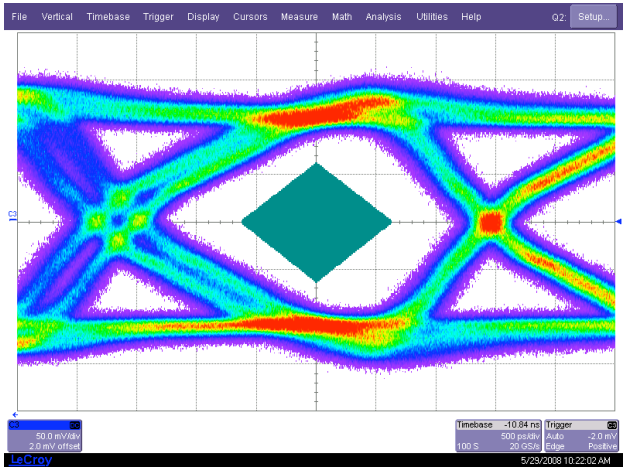
Clock Multiplier

- Both 4 x and 16 x clock multipliers work
  - clock jitter < 8 ps (0.5%)
  - two of the four chips lost lock during irradiation
    - need power cycling to resume operation at 640 MHz
  - no change in current consumption



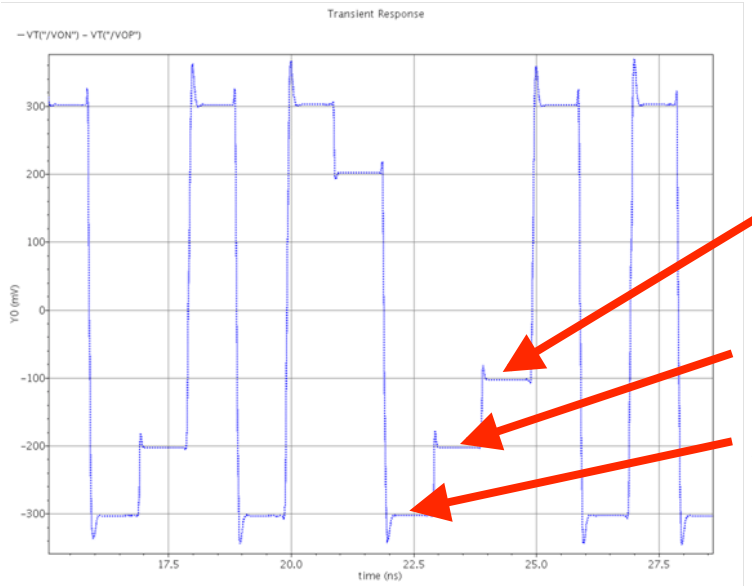


Skinny Wires with Pre-emphasis



320 Mb/s

4 m



No emphasis

1st tap emphasis

2nd tap emphasis

- Signals from modules (320 Mb/s) can be transmitted up to ~ 4 m with pre-emphasis
  - minimum material
  - allow serializer chip to be placed further from the IP to reduce SEU

Summary

- Good PIN candidates identified
- Good VCSEL candidates identified
- First 0.13 μm submission mostly successful
  - full characterization of pre/post irradiation in progress
  - aim for next iteration in winter 2009