Radiation-Hard/High-Speed Parallel Optical Links

K.K. Gan, H. Kagan, R. Kass, J. Moore, D.S. Smith
The Ohio State University

P. Buchholz, A. Wiese, M. Ziolkowski
Universität Siegen

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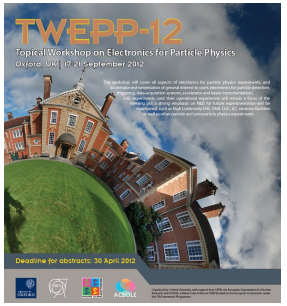
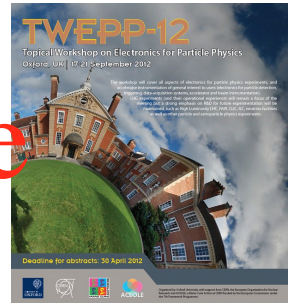
Outline



- Introduction to a compact solution
- Results with 5 Gb/s VCSEL array driver
- Summary

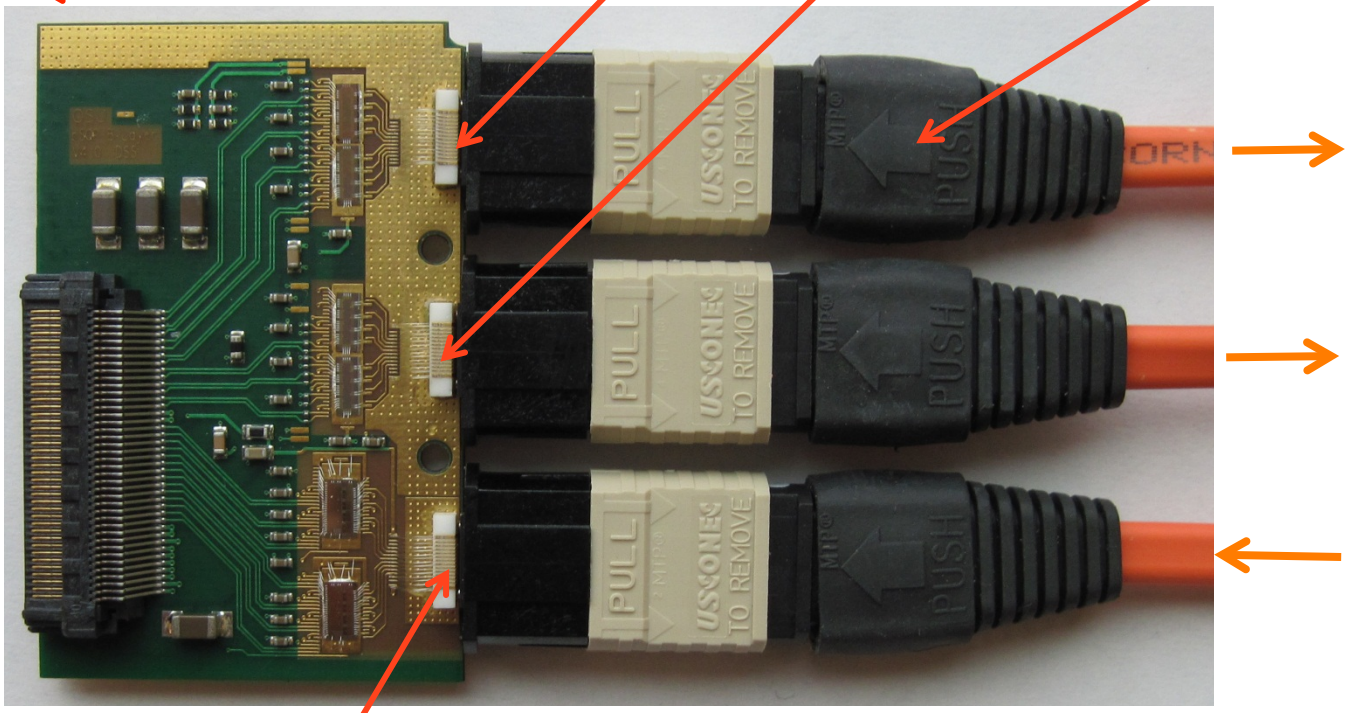
Use of VCSEL Arrays in ATLAS

- Widely used in off-detector data transmission
- First on-detector implementation in pixel detector
  - experience has been positive
    - VCSELs used are humidity sensitive but they are installed in very low humidity location
    - modern VCSELs are humidity tolerant
    - ⇨ will use arrays for next pixel detector upgrade (IBL)

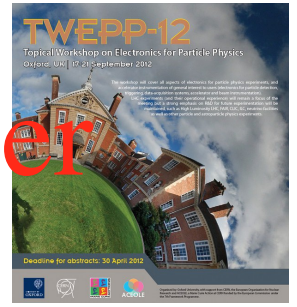


New Parallel Optical Engine

- Improved design for new pixel layer of ATLAS
  - use 12-channel VCSEL and PIN arrays
  - ⇨ 36 optical channels



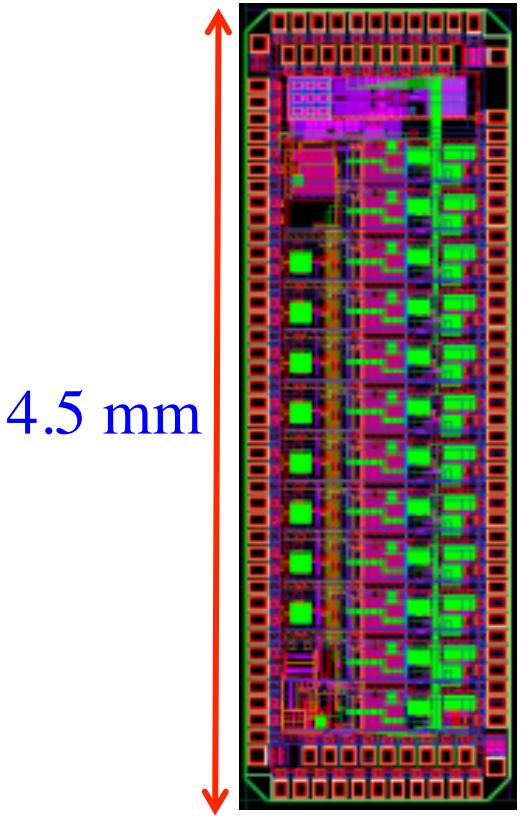
New 12-Channel VCSEL Driver

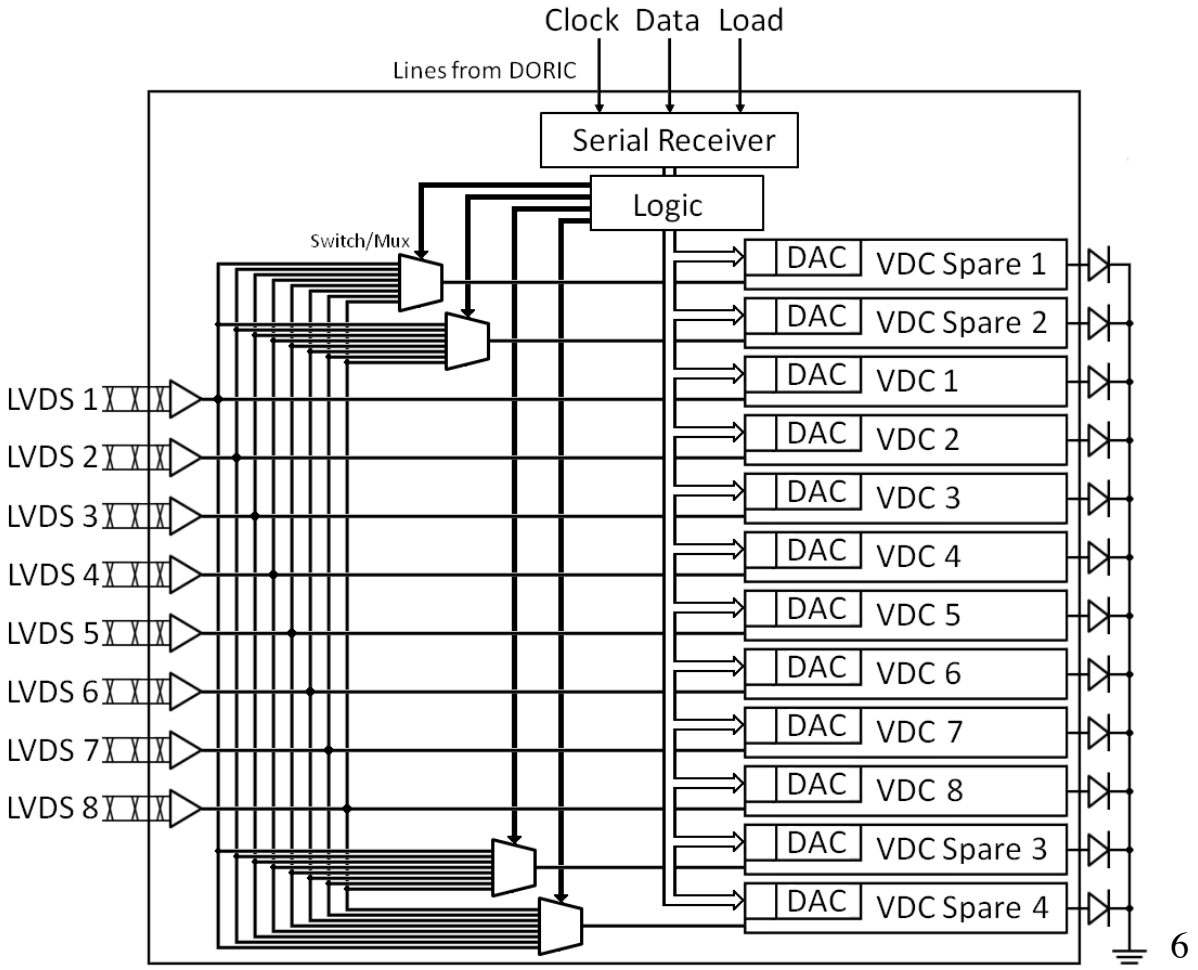


- New ASIC designed using 130 nm CMOS
- Incorporate improvements taking advantage of experience from 1st generation parallel optical engine:
  - ✔ redundancy to bypass a broken VCSEL
    - special thanks to FE-I4 group (Roberto Beccherle et al.) for command decoder circuit
  - ✔ power-on reset in case of communication failure:
    - ✔ no signal steering
    - ✔ 10 mA modulation current (on current)
    - ✔ 1 mA bias current (off current)
- Will only operate at 160 Mb/s for new pixel layer but designed ASIC to operate at much higher speed (5 Gb/s) to gain experience in designing high-speed parallel driver

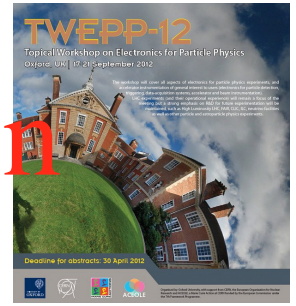
New VCSEL Array Driver

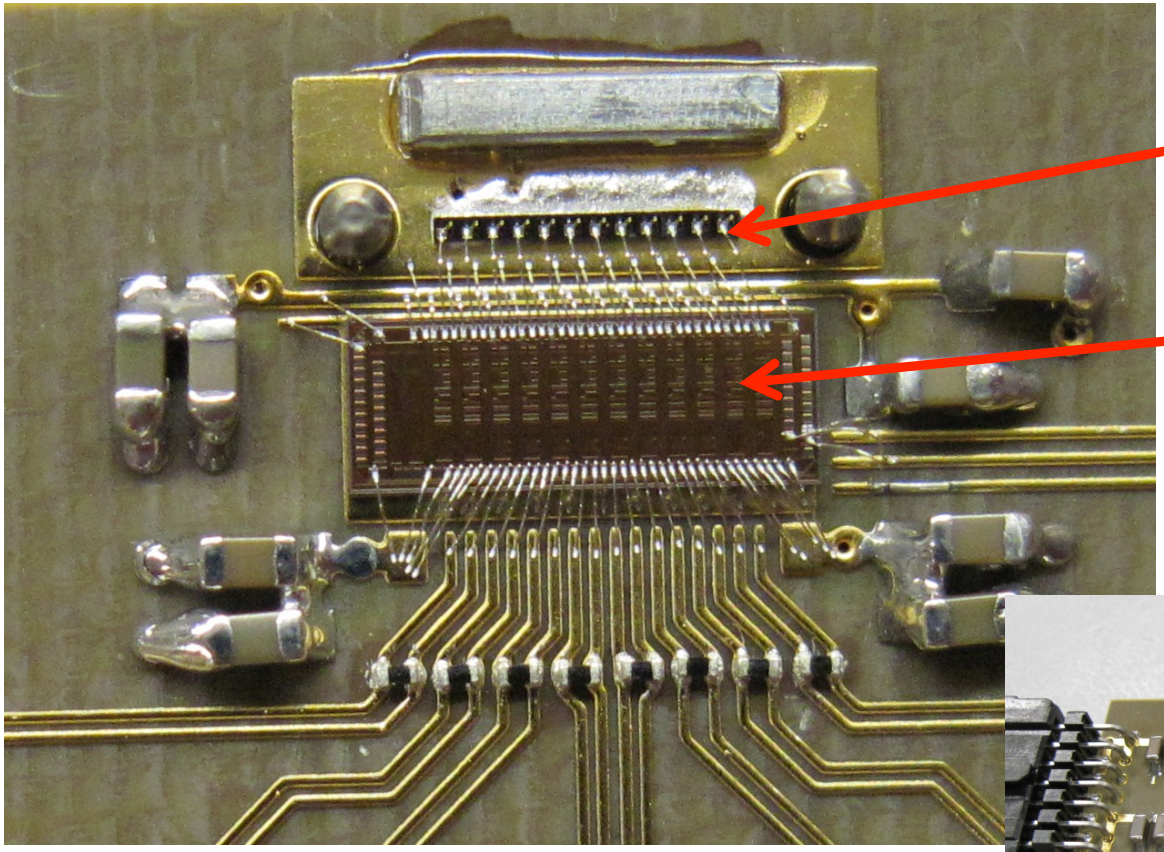
- Only inner 8 channels connected to new pixel modules
  - future driver could reserve only one channel for redundancy





High-Speed Test Configuration

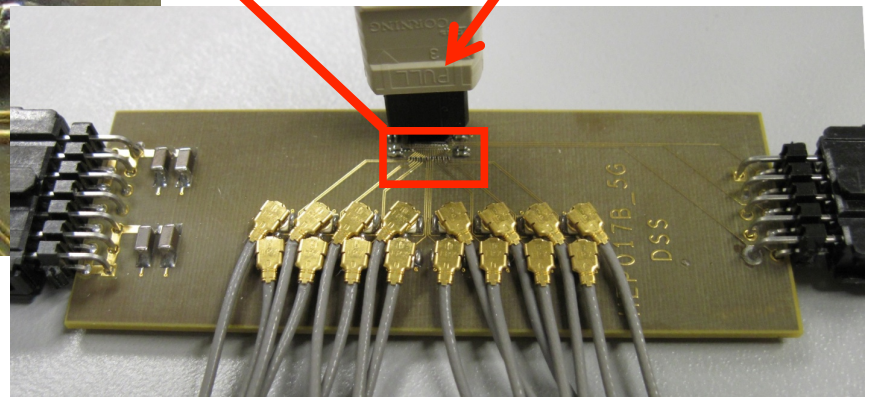




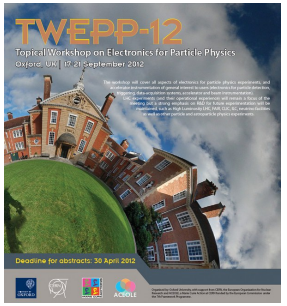
10 Gb/s ULM
VCSEL array

VCSEL
array driver

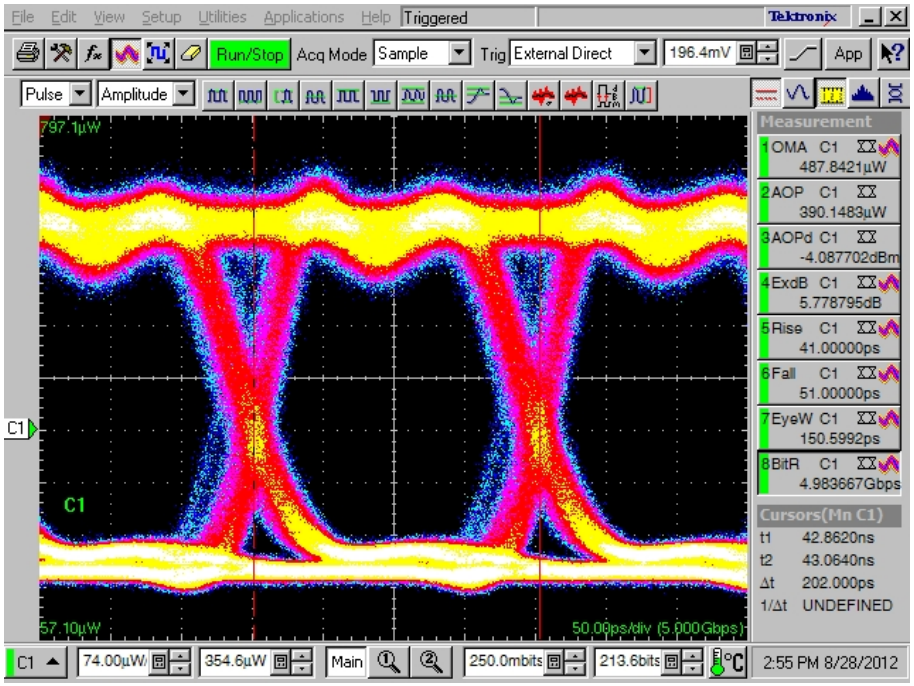
MPO connector

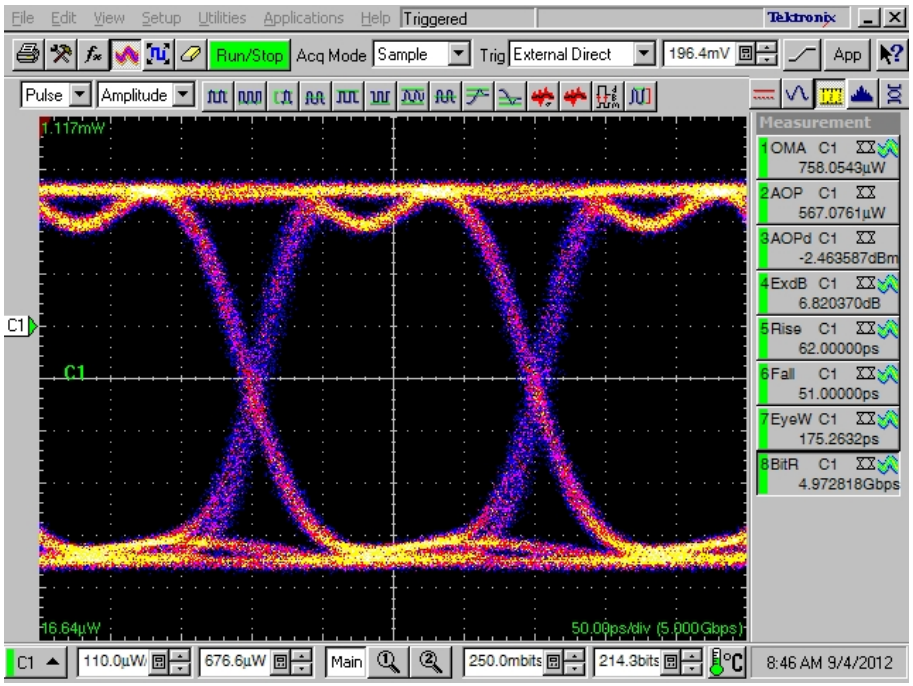


Optical Eye Diagram



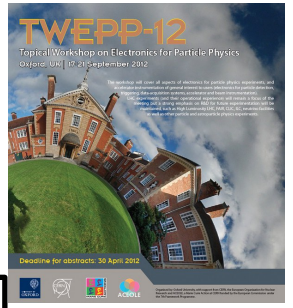
SFP+: single channel

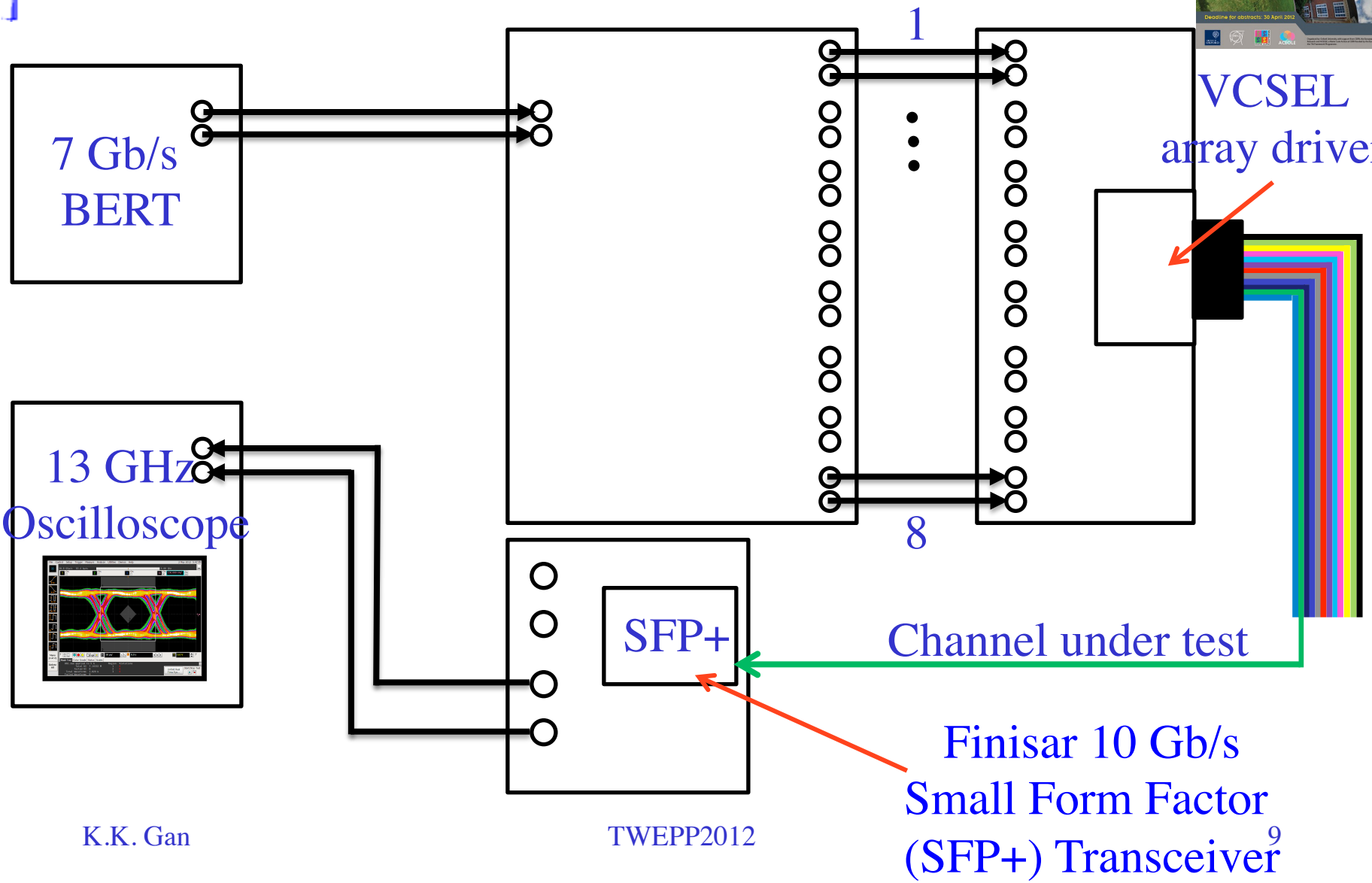




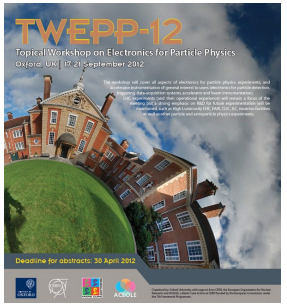
- optical eye diagram @ 5 Gb/s is quite acceptable
  - special thanks to Alan Prosser @ Fermilab for use of equipment

SFP+ as Optical Probe

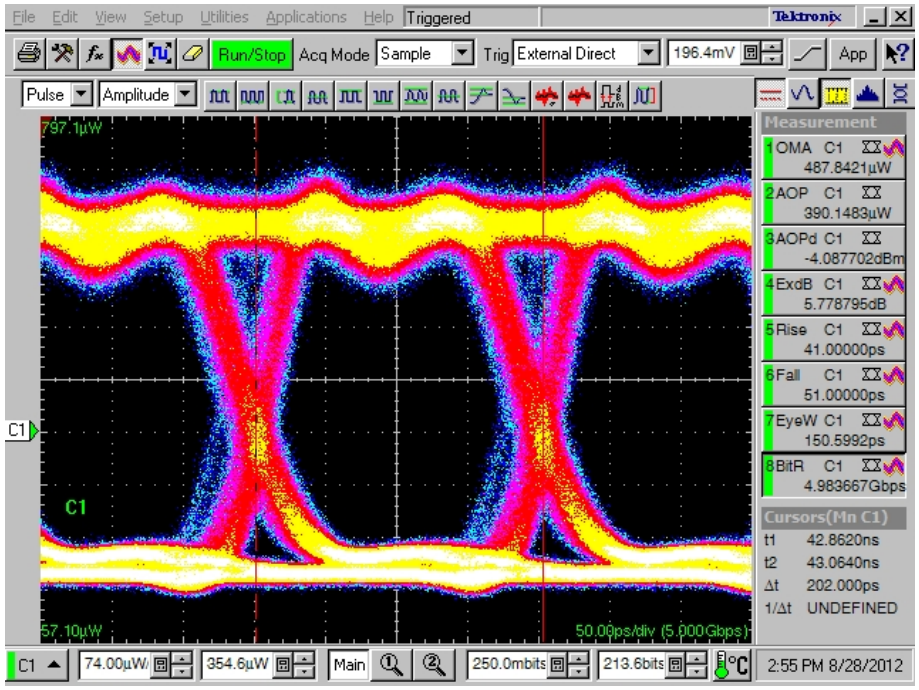




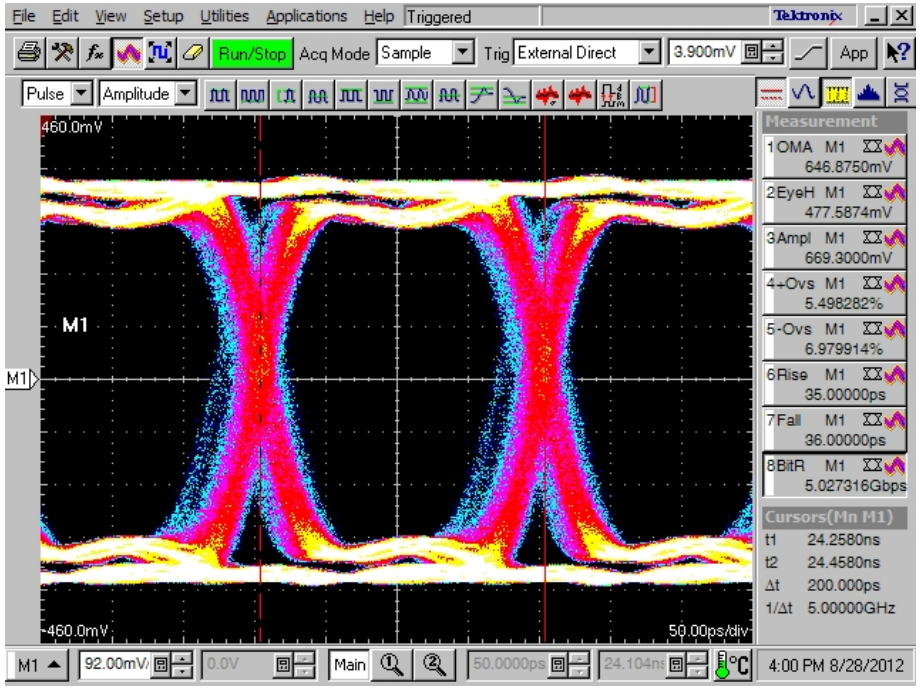
Optical Probe vs. SFP+



Optical probe



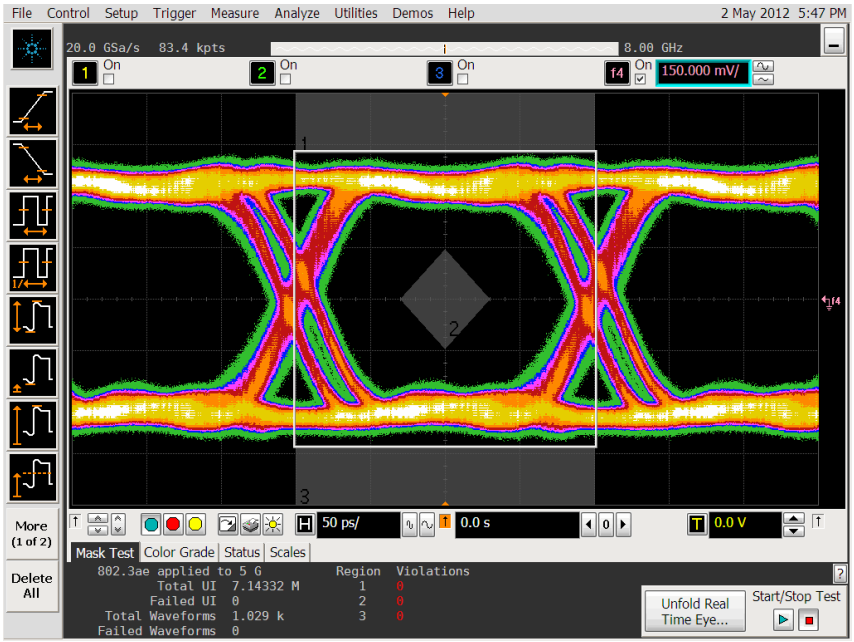
SFP+



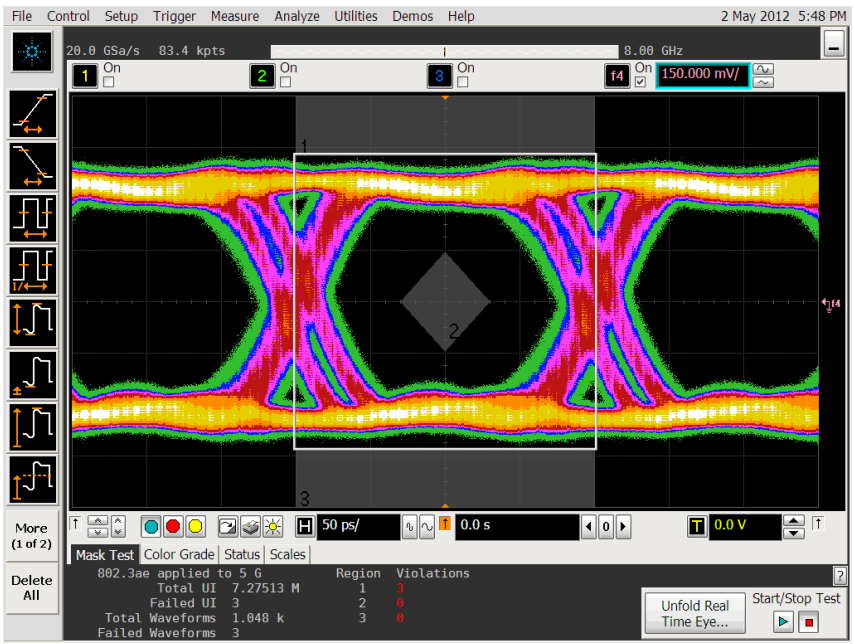
- SFP+ cleans up the eye by slightly improving the rise/fall times

Eye with One/All Channels Active

One channel active



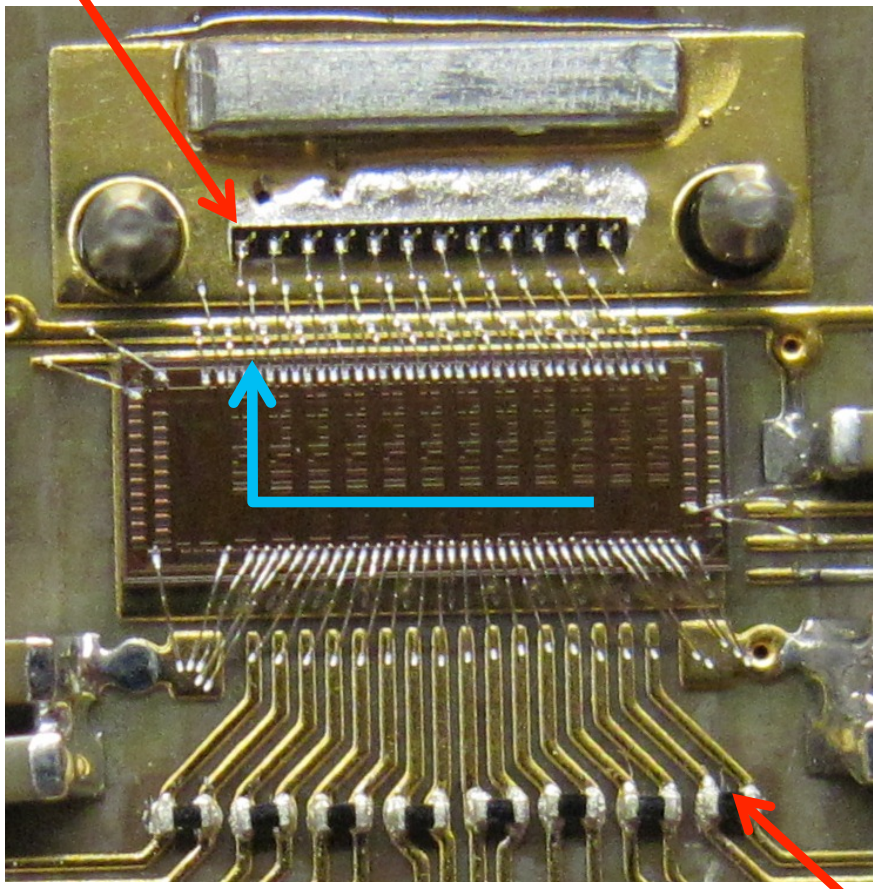
All channels active



- all channels work @ 5 Gb/s with bit error rate < 5×10^{-13} for all channels active
- jitter increases with all channels active but still passes the mask test

Effect of Steering on Eye

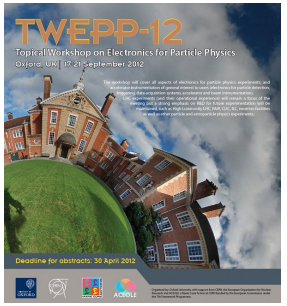
VCSEL spare 1



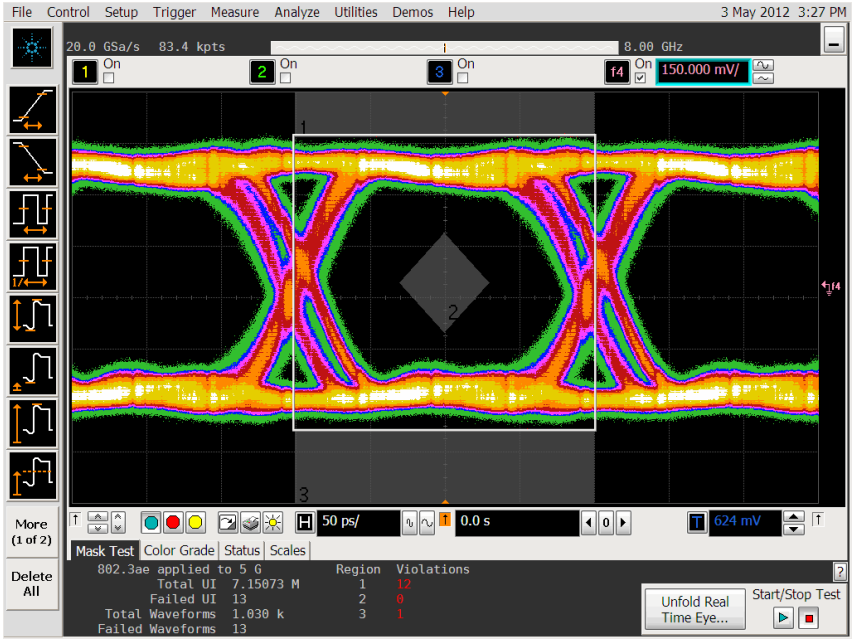
Receiving LVDS signal from channel 8, steering to VCSEL spare 1

LVDS in channel 8

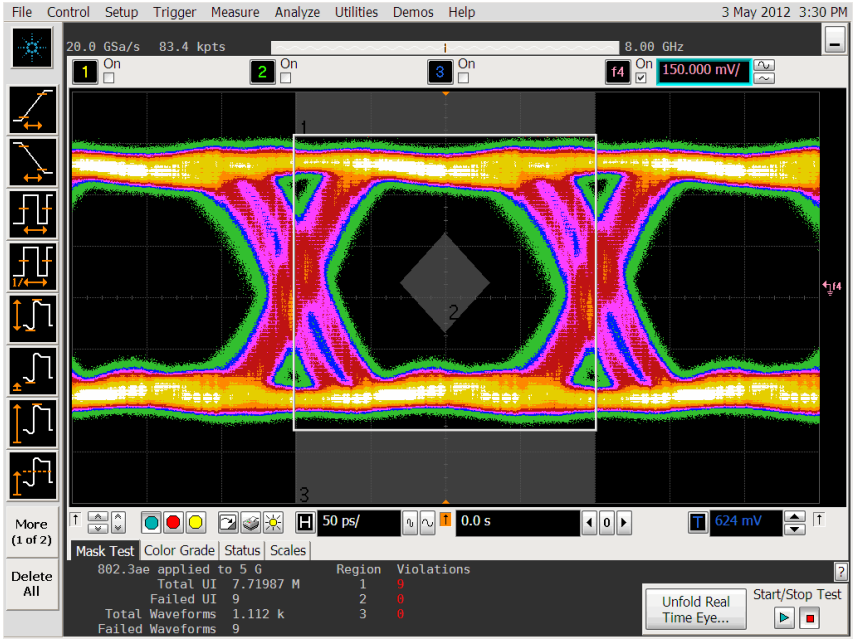
Effect of Steering on Eye



Spare 1 output with other channels off

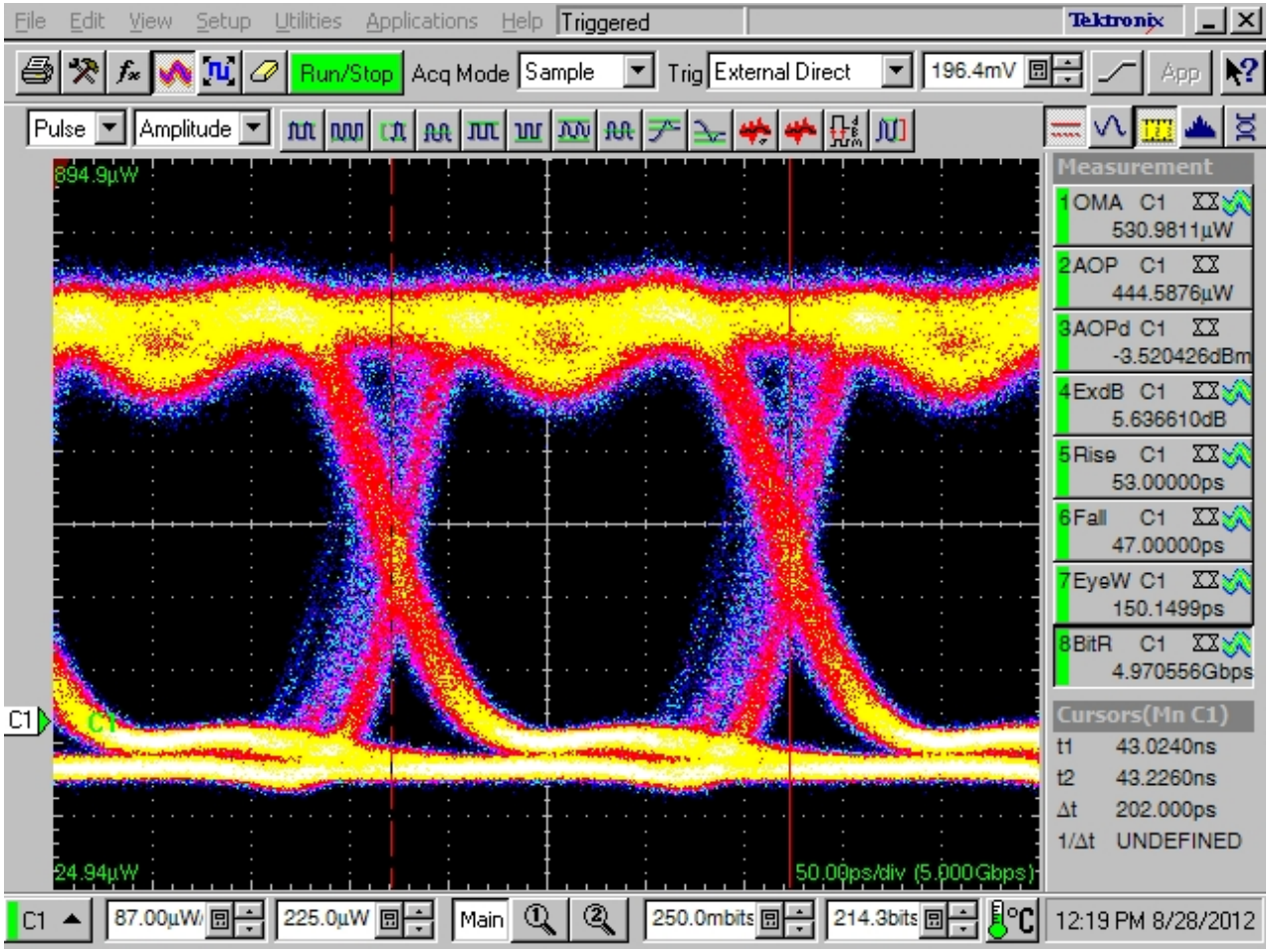


Spare 1 output with all channels active



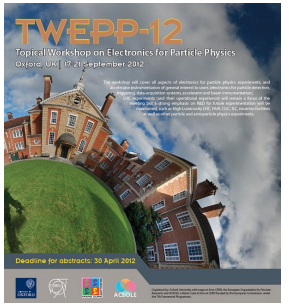
- steered channel still passes the mask test
  - jitter increases with all channels active

Optical Eye Diagram of Steered Signal



- optical eye diagram of steered signal @ 5 Gb/s is quite acceptable

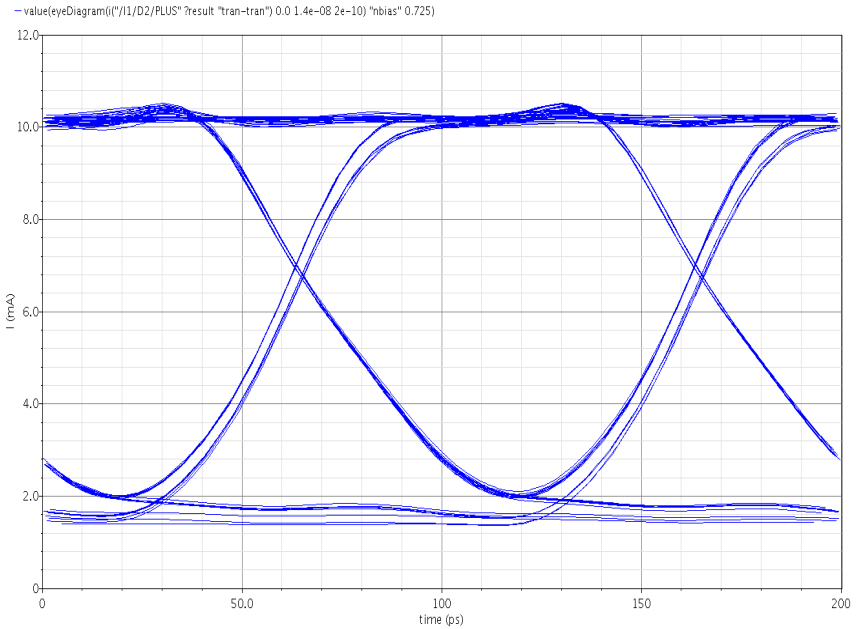
Radiation Hardness



- 10 Gb/s VCSEL arrays have been proven to be radiation hard to tens of Mrad
  - send signal on ~1 m micro co-ax cables to less radiation and more serviceable location
- VCSEL array driver was irradiated with 24 GeV protons at CERN last August to test Radiation hardness
  - await return of irradiated ASICs for characterization

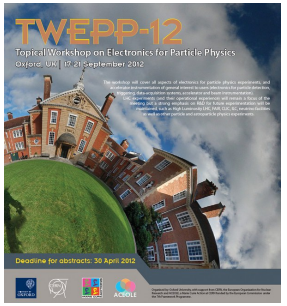
Future Plan

- 10 Gb/s transmission needed
  for ATLAS inner pixel layer and LAr readout upgrades
  - joint ATLAS/CMS proposal funded
    via US DOE generic R&D program
  - layout of driver stage being optimized (130 nm CMOS)



extracted simulation of
driver stage with
bond pad parasitics

Summary



- VCSEL array offers compact solution to data transmission
- 5 Gb/s VCSEL array driver successfully prototyped
- Currently designing 10 Gb/s VCSEL array driver