



Design, Production, and Reliability of the New ATLAS Pixel Opto-Boards

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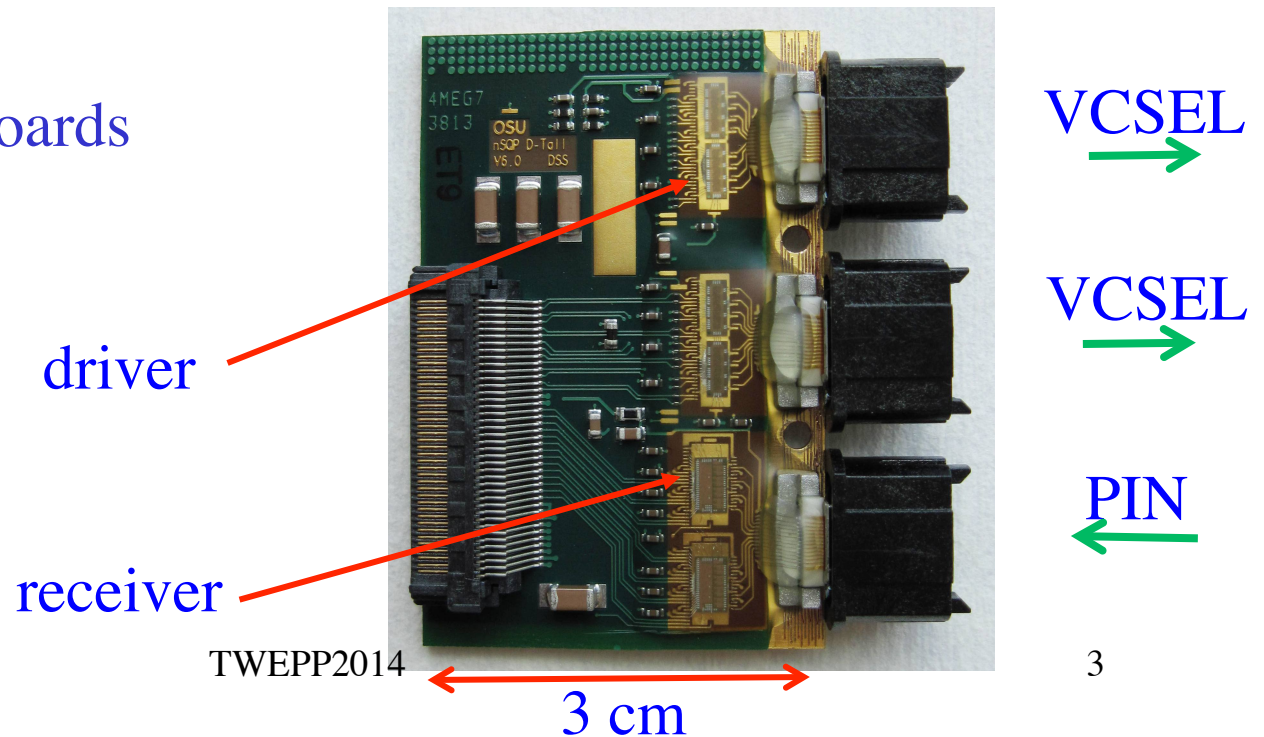
Use of VCSEL Arrays in HEP

- Widely used in off-detector (no radiation) data transmission
- First on-detector implementation in pixel detector of ATLAS
 - ◆ experience has been positive
 - VCSELs used are humidity sensitive but they were installed in very low humidity location
 - modern VCSELs are humidity tolerant
 - opto-links built by OSU have $\sim 0.1\%$ broken links
 - decided to move opto-links to more accessible location
 - ⇒ use arrays for the replacement optical links for current 3-layer pixel detector and the new inner layer (IBL)



Opto-Board Flavors

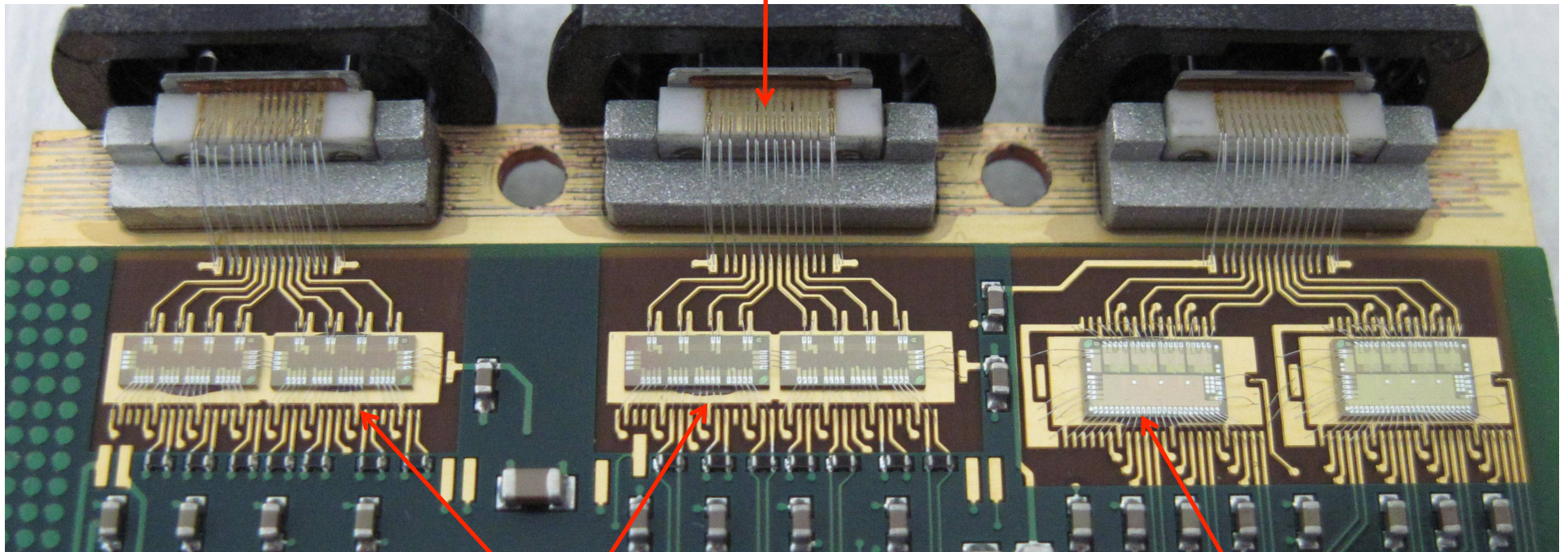
- 3 opto-board flavors
 - outer 3-layers + disks (nSQP):
 - ◆ D opto-board (disk, L1, L2): 7 TTC + 14 data links
 - ◆ B opto-board (B-layer): 7 TTC + 14 data links
 - inner layer:
 - ◆ IBL opto-board: 8 TTC + 16 data links
- 300 boards needed
 - produced ~400 boards
or ~8,500 links





Close Up View

Opto-pack



VDC
(VCSEL driver)

DORIC
(PIN receiver/decoder)



Opto-Board Improvements

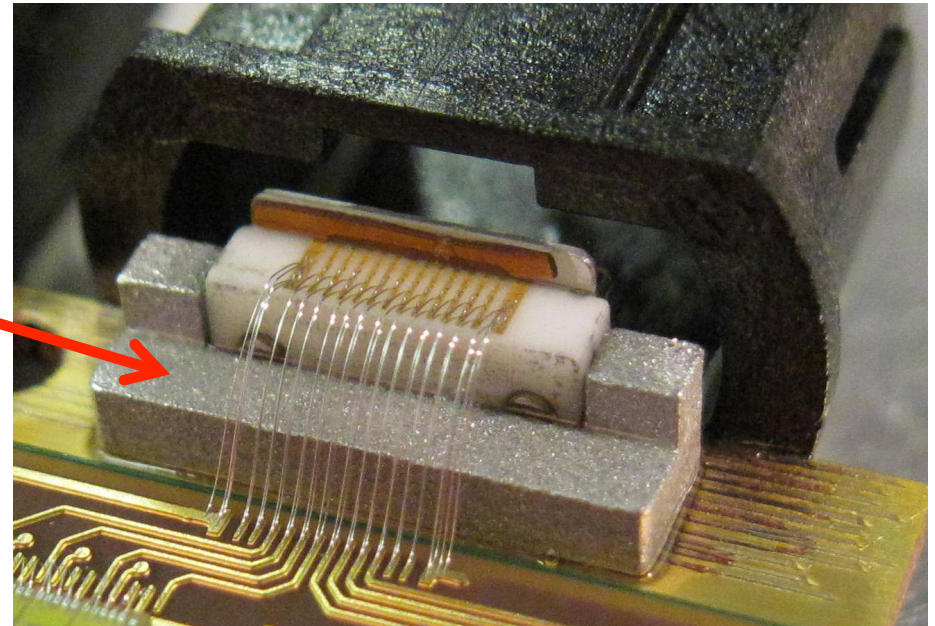
- Implemented several improvements based on experience gained from production of 1st generation opto-boards:
 - replace custom optical connector with MPO for easier mating/de-mating
 - mount array on BeO instead of PCB for efficient heat removal
 - connect optical package to opto-board by wire bonding instead of soldering micro-leads to BeO
 - ◆ soldering was major challenge in previous opto-board production
 - too much heat cause lead detachments
 - too little heat produces cold solder
 - ◆ cold solder is a major cause of opto-link failures
 - ◆ opto-boards built by OSU have ~0.1% broken links



Opto-Pack Enforcement

- Several opto-packs detached at various stages of production
 - ⇒ two improvements:
 - ◆ scoring of PCB surface to improve adhesion
 - ◆ add aluminum brace to greatly increase epoxy contact area
 - ⇒ cannot remove opto-pack without destroying opto-pack

Sandblasted surfaces
to improve adhesion





Problematic Epoxy

- Detachment of MPO connectors on several boards (< 10) early in the production
- 22 boards used epoxy with different color
 - ⇒ replace 66 MPO connectors
 - ◆ 30 insertion tests performed on 40 connectors before removal
 - 10 insertion tests during QA
 - ⇒ no connector detached after 40 insertion tests
 - ⇒ expect no detachment under normal operation
- 19 boards successfully recovered



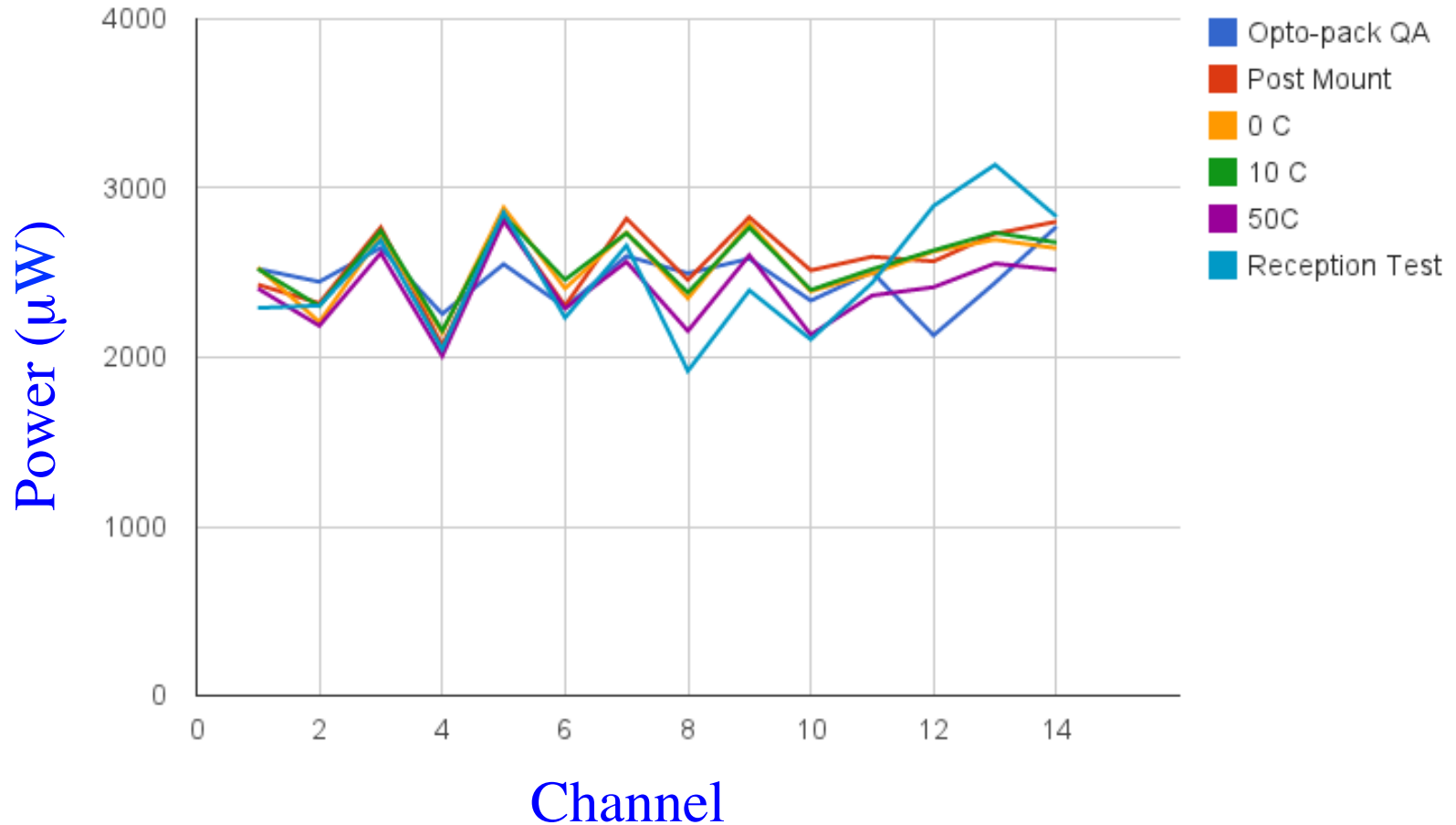
Opto-Board Quality Assurance

- perform QA test similar to 1st generation opto-boards to validate constructed boards
 - ◆ burn in: 72 hours @ 50°C
 - ◆ 10 thermal cycles: 0°C $\Rightarrow$ +50°C
 - 2 hours per cycle
 - 1 hour soak at 50°C
 - ◆ electrical and optical QA



Opto-Board Optical Power

D4201

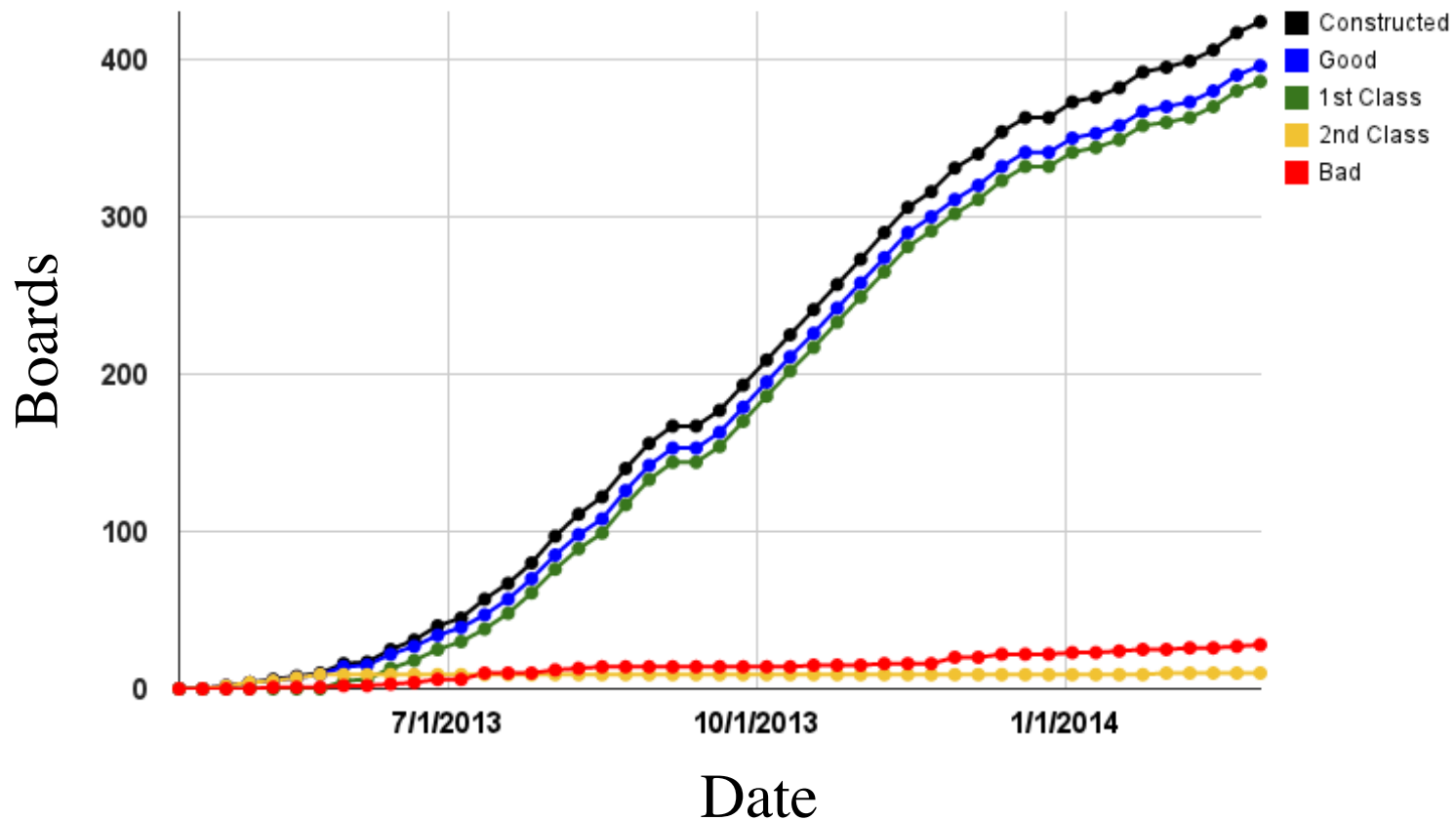


● Excellent optical power!!!



Production Statistics

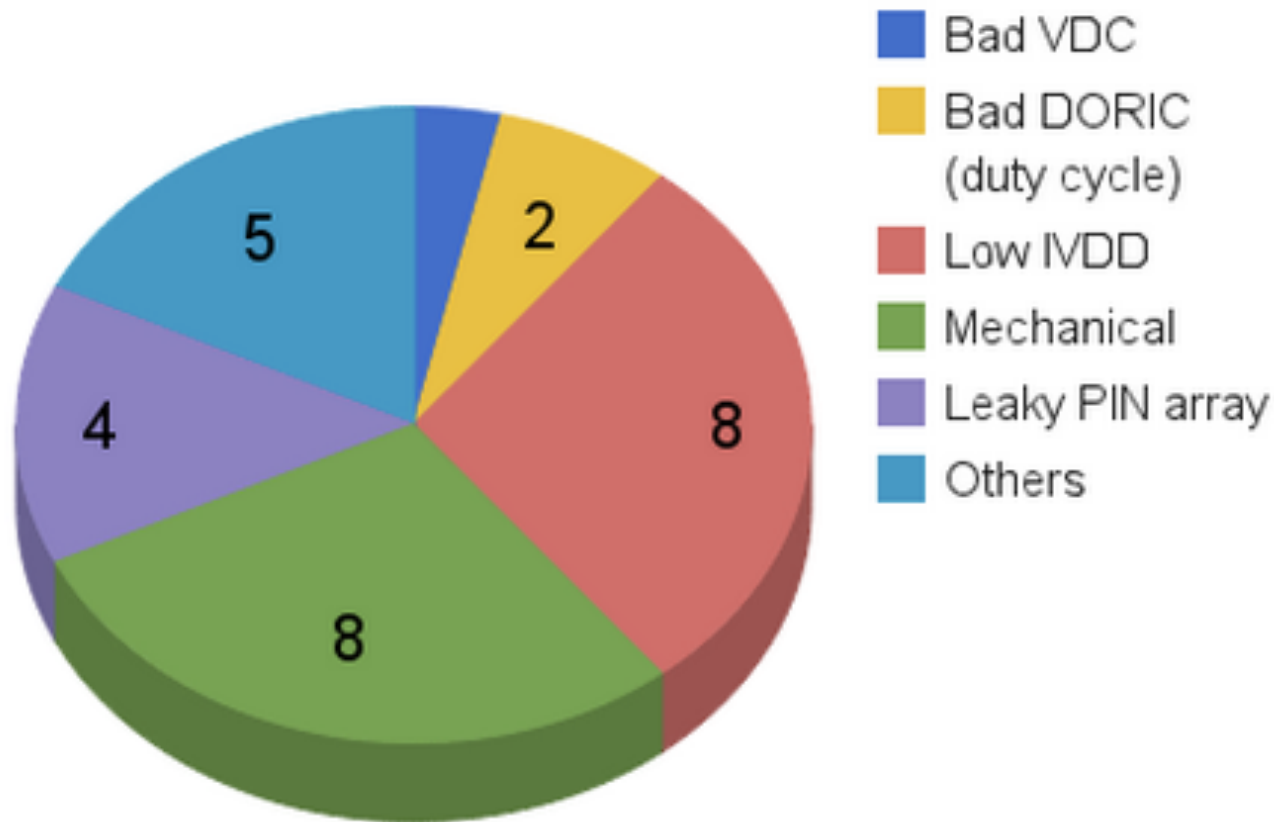
- Total fabricated: 421
 - Good: 393 (1st class: 383, 2nd class: 10)
 - Bad: 28





Summary of Failed Boards

Failed Opto-Boards





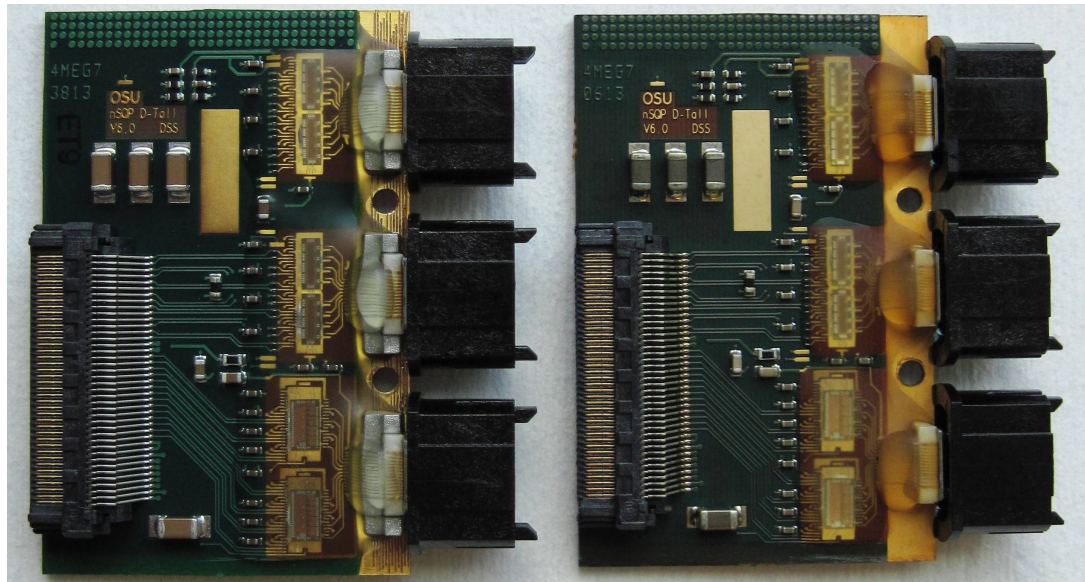
Extended Burn-In

- Several of the 400 boards have problems after burn-in/thermal cycles:
 - ◆ 1 VDC: cannot adjust drive current
 - ◆ 8 VCSEL arrays have low power
 - 3 failed for thermal cycle outside Finisar spec: -25 C
 - ⇒ thermal cycle: 0-50 C
 - 5 arrays not properly glued to BeO substrate
 - ◆ 4 leaky PIN arrays



Accelerated Lifetime Test

- Industry standard: opto-boards should survive for 1,000 hours at 85°C/85% relative humidity
 - ◆ operate each VCSEL channel with 10 mA (pk-pk)
 - ◆ perform weekly measurements
 - VCSEL optical power
 - PIN dark current
 - supply current
 - operate with no error in all channels

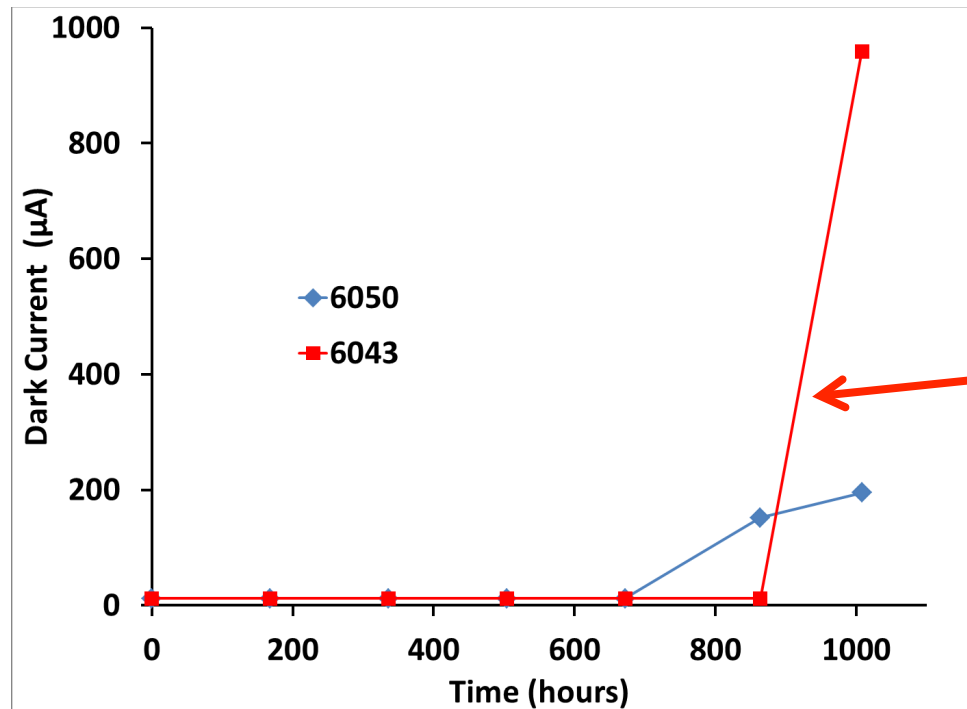


After 1,500 hours
at 85°C/85% RH



Accelerated Lifetime Test-Phase I

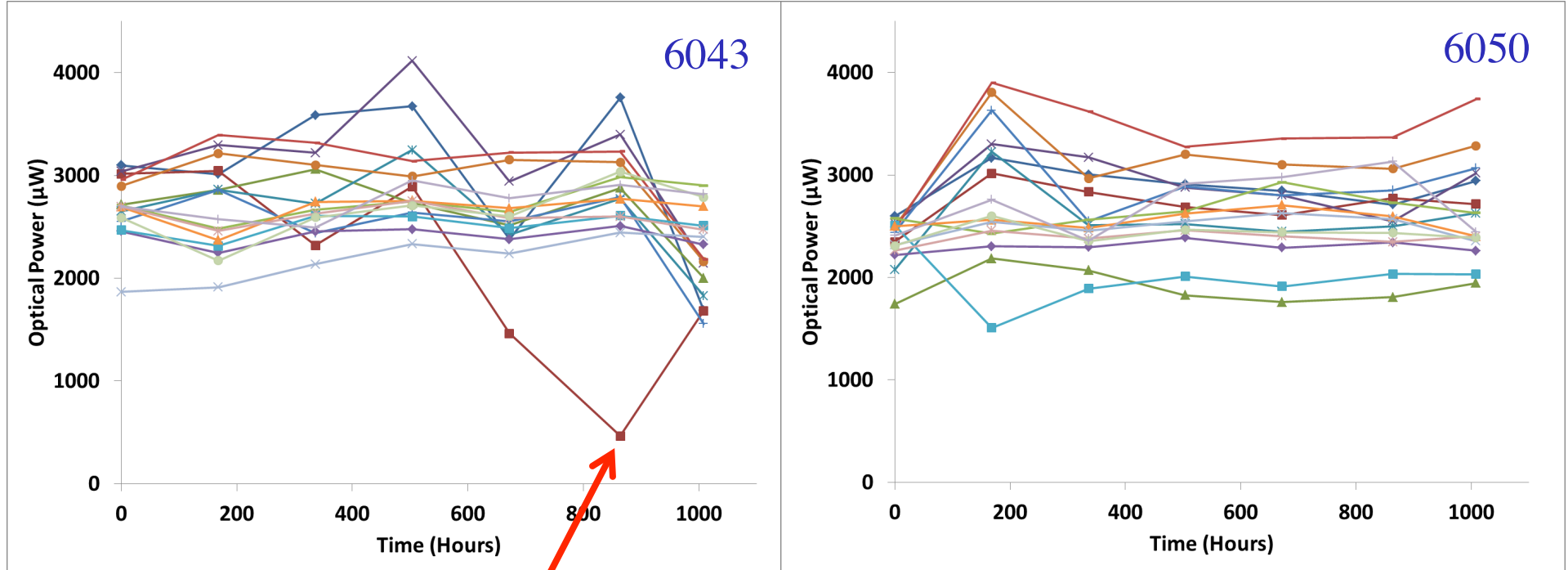
- Started the test with two IBL boards on Feb. 2014
- ◆ All VCSEL channels survived
- ◆ Both PIN arrays became leaky before 1,000 hours
 - PIN biased at 10 V
 - ULM photonics: recommend operate at 5 V even though spec. sheet lists bias as up to 10 V





Accelerated Lifetime Test-Phase I

- VCSEL optical power OK up to 1,008 hours in 85°C/85% RH

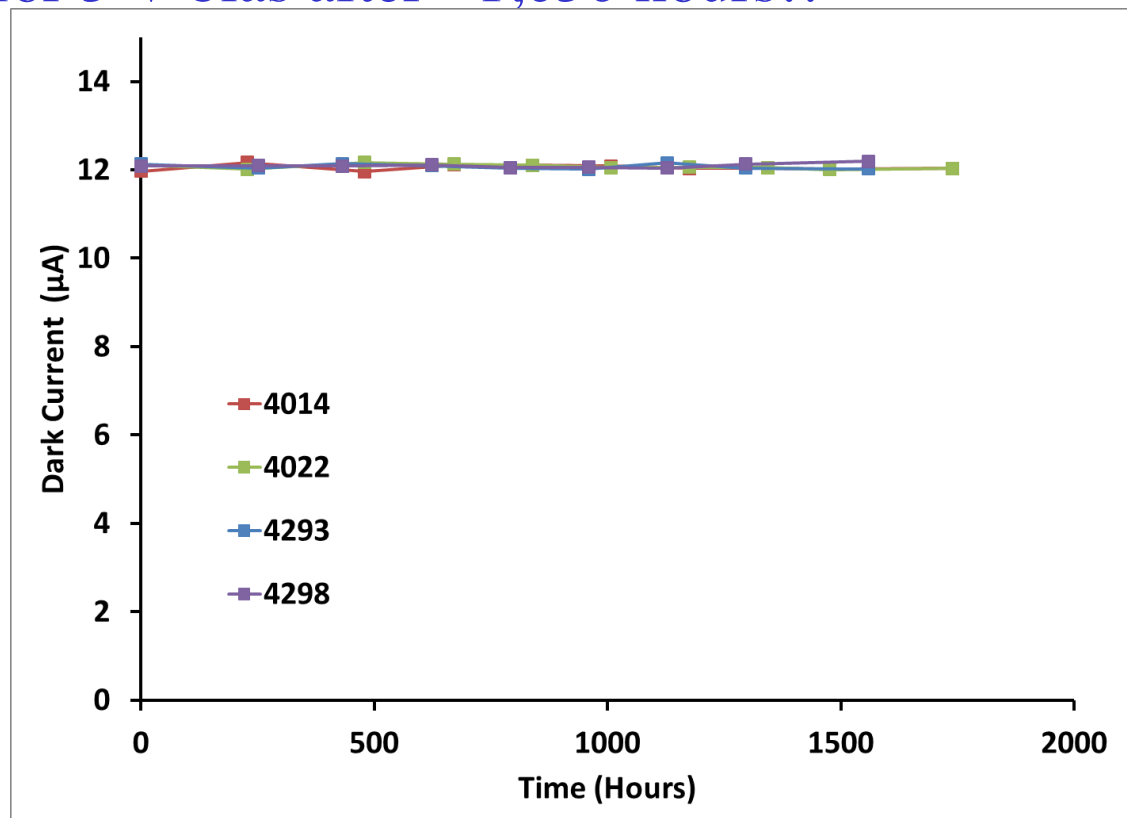


Dirty VCSEL



Accelerated Lifetime Test-Phase II

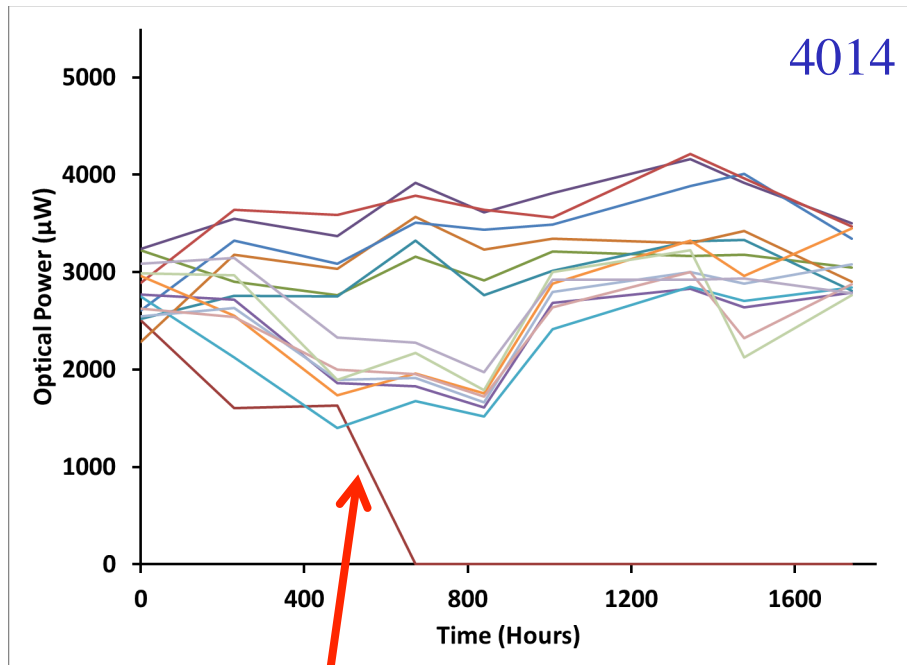
- June/July: started four D opto-boards in 85°C/85% RH
 - ◆ 2 boards fabricated in 6/2013: optical power OK after 1,740 hours
 - ◆ 2 boards fabricated in 12/2013: optical power OK after 1,560 hours
 - ◆ PIN arrays biased at 10 V in ~4 days of burn-in/thermal cycle
 - No leaky PIN arrays for 5 V bias after ~1,650 hours!!





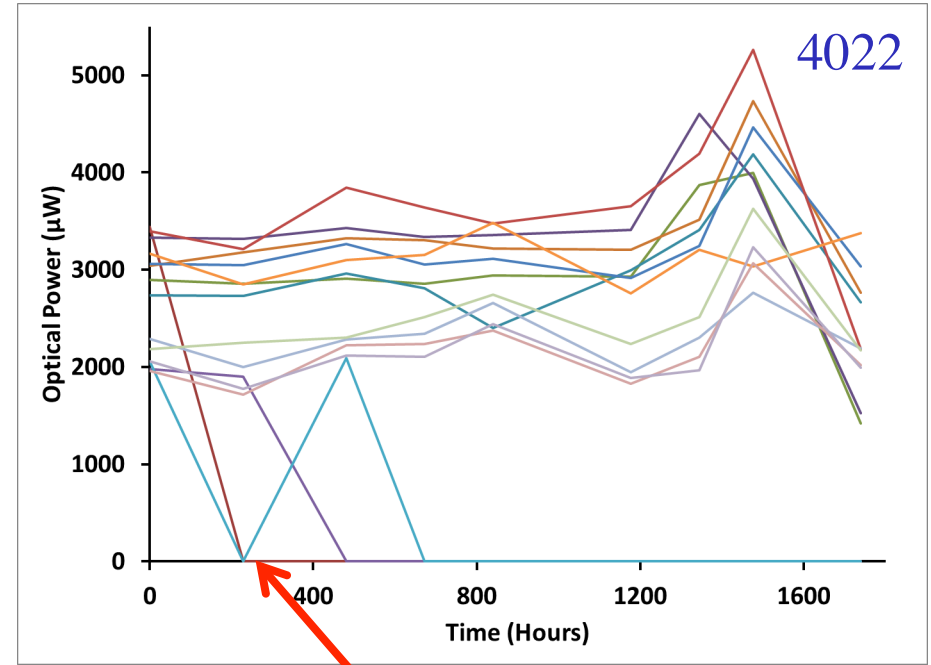
Accelerated Lifetime Test-Phase II

- VCSEL optical power OK up to 1,740 hours in 85°C/85% RH



Wirebond broken during cleaning

K.K. Gan



Board dropped

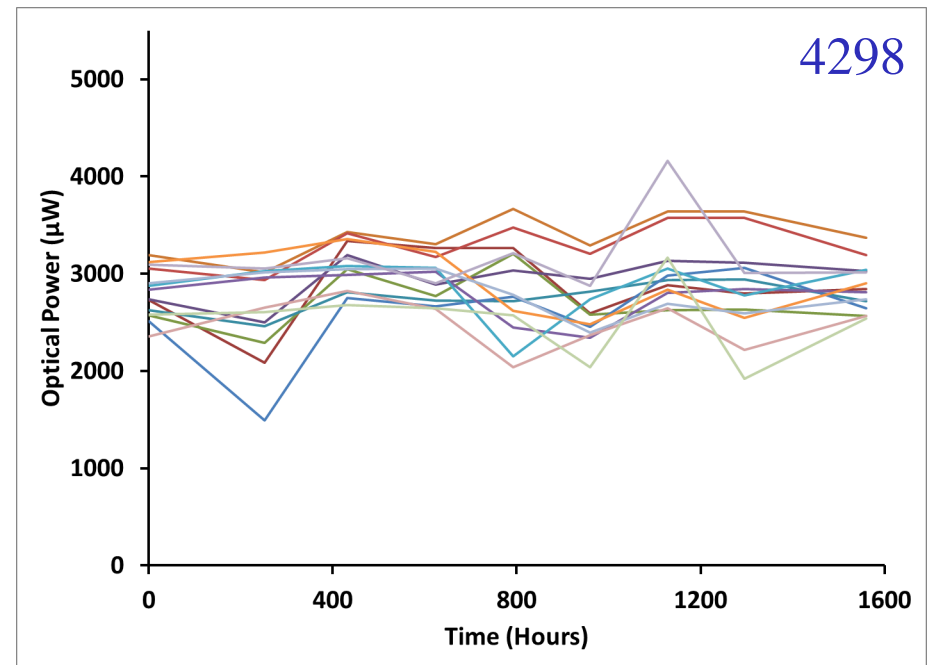
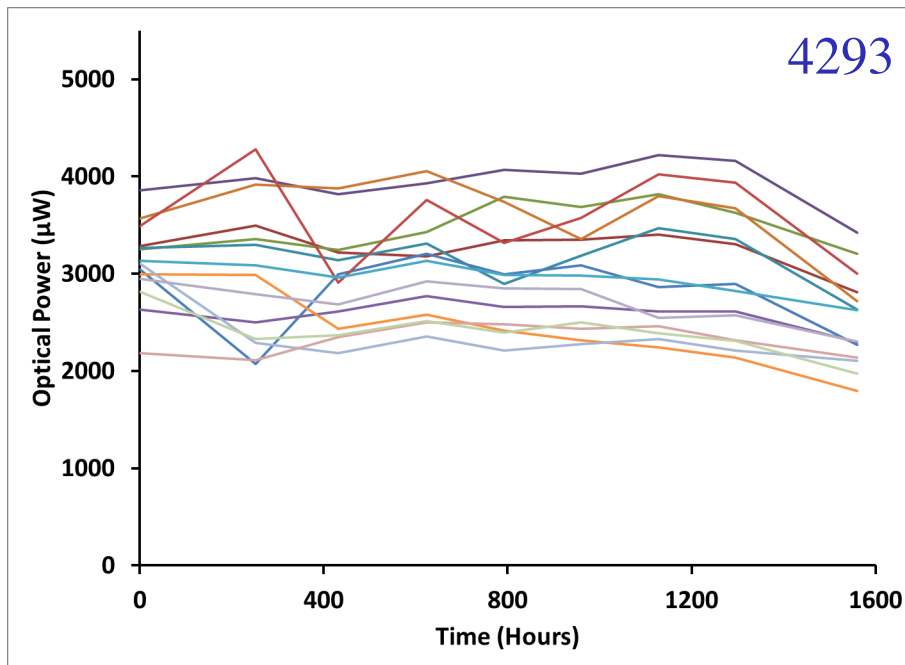
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Accelerated Lifetime Test-Phase II

- VCSEL optical power OK up to 1,560 hours in 85°C/85% RH

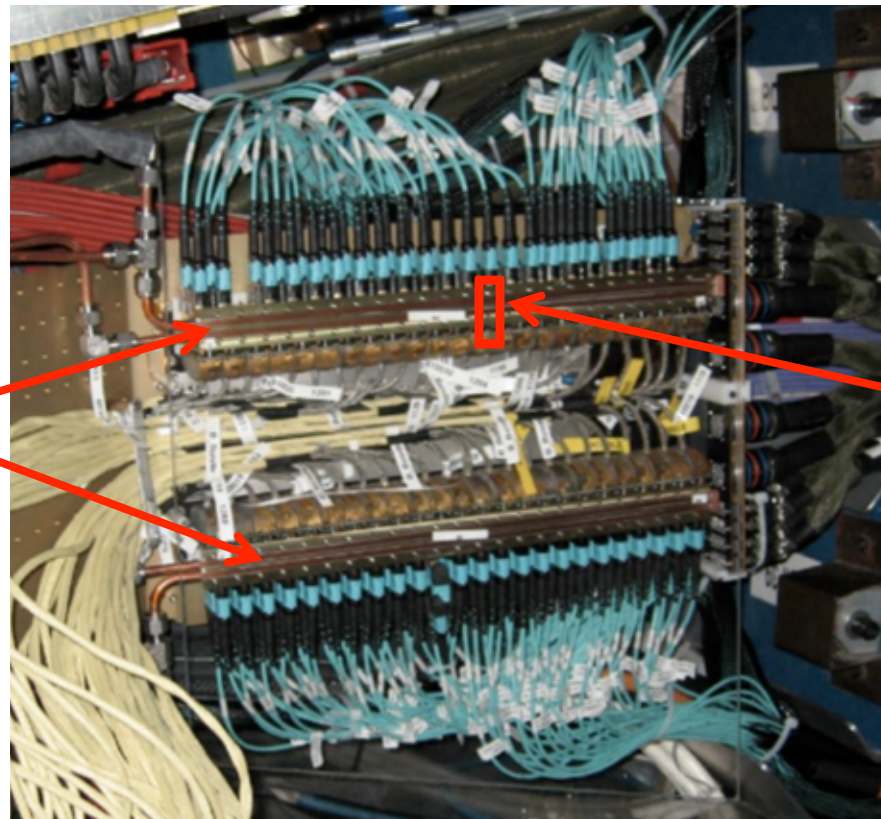




Opto-Boards Installation

- Installation successfully completed in June
 - ◆ smooth installation process
- No infant mortality after 1 month of operation

cooling rail



opto-board



Summary

- fabricated 400 opto-boards with many improvements
- opto-boards production was smooth
- opto-boards successfully installed
- production opto-boards passed accelerated lifetime test
 - ◆ 10 V bias degrades PIN array lifetime!
- planning to begin long term 50°C/50% RH study next