Optical Link Driver/Receiver for Silicon Trackers

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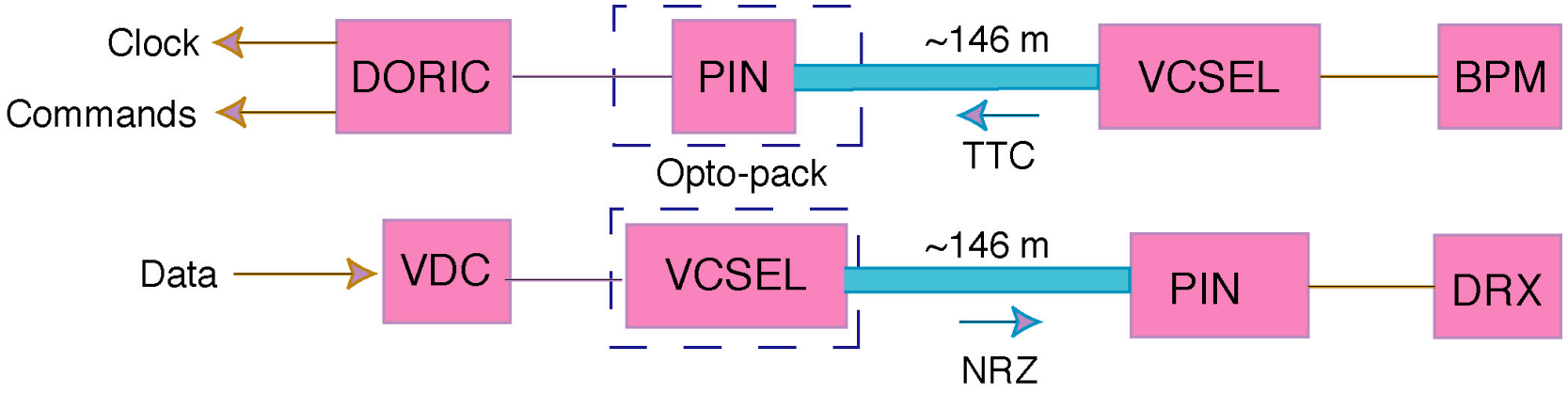
Pixel/SCT Opto-link



VDC: VCSEL Driver Circuit

DORIC: Digital Optical Receiver Integrated Circuit

VCSEL Driver Chip Upgrade

- SCT/Pixel clock speed: 40 MHz
  - ⇨ 80 Mb/s using both clock rising/falling edges to transmit data
- SCT:
  - VDC: two channels/chip, AMS 0.8 μm bi-polar
  - optical package: 2 Truelight VCSELs + 1 Centronic PIN
    - use two data links for redundancy
- Pixel:
  - VDC: four-channels/chip, IBM 0.25 μm CMOS
    - radiation hardness: > 70 Mrad
  - optical package: 8-channel Truelight VCSEL array
    - B-layer uses two data links to transmit at 160 Mb/s
- Future: multiply 40 or 80 MHz clock by 8 or 16
  - ⇨ 0.64 - 2.56 Gb/s which may be adequate for silicon trackers

Use of VCSEL in Upgrade?

- VCSEL arrays from three vendors can operate at ~2.5 Gb/s
  - ⇨ continue use of VCSEL but operate at higher speed is an attractive upgrade possibility for silicon trackers
- radiation hardness of VCSEL is probably adequate
  - Truelight VCSEL loss ~ 20% of light at ~30 Mrad
    - annealing can recover most of the loss
    - annealing is part of SCT/Pixel operation
  - need irradiation at higher dosage to verify radiation hardness
- Pixel detector uses 8-channel VCSEL with MT ferrule
  - same ferrule can support 12-channel array
  - ⇨ higher density transmission with small increase in size of fiber ribbon since shielding is a significant contribution

What Gb/s Driver is Available?

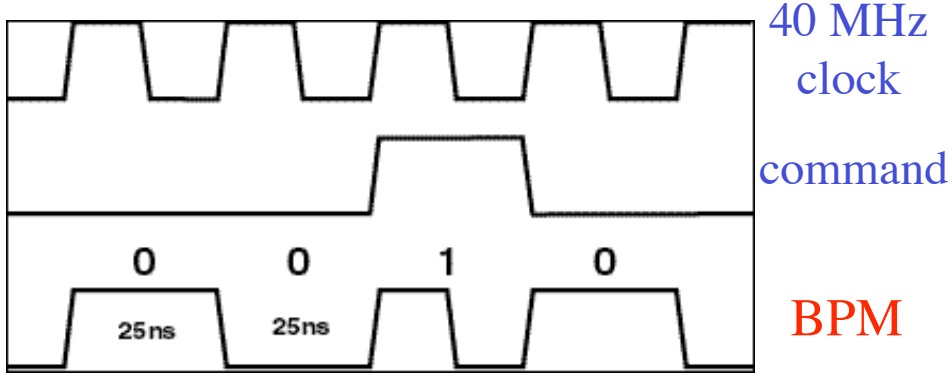
- 5 commercial VCSEL drivers with 2.5-10 Gb/s capacity
  - one driver has 12-channel version
    - designed to be compact and work with 12-channel array?
  - all operate at 3.3 V supply voltage
    - most likely fabricated with 0.8 μm technology
    - ⇨ need to custom design with deep submicron technology to work with VCSEL array
- producing enough voltage to driver VCSEL is a challenge:
  - Truelight VCSEL needs ~1.9 V to produce 10 mA
    - higher current is needed for efficient annealing
  - operating voltage of 0.13 μm chip is 1.2 V
    - thick oxide can operate at 2.5 V
    - ⇨ need to test irradiation hardness of thick oxide chip

Receiver Chip Upgrade

- SCT :
  - DORIC: one channel/chip, AMS 0.8 μm bi-polar
  - optical package: 2 Truelight VCSELs + 1 Centronic PIN
- Pixel:
  - DORIC: four-channels/chip, IBM 0.25 μm CMOS
    - radiation hardness: > 70 Mrad
  - optical package: 8-channel Truelight PIN array
- Future: use 12-channel receiver chip with PIN array?

Use Bi-Phase Mark Encoding?

- both SCT and Pixel use bi-phase marked encoding:
  - clock+command are encoded as single signal for transmission
  - receiver chip decodes the signal to extract clock and command
  - guarantee phase relationship between clock and command
  - no baseline shift due to different string of commands because encoded signal has 50% duty cycle
- continue use of bi-phase marked encoding?



What Gb/s Receiver is Available?

- 4 commercial PIN receivers with 1.25-2.5 Gb/s capacity
  - all single channel device
  - all operate at supply voltage of 3.3 V
    - most likely fabricated with 0.8 μm technology
    - ⇨ need to custom design with deep submicron technology to work with PIN array

Summary

- continue use of VCSEL/PIN arrays but
  operate at 1-2 Gb/s is a possible upgrade scenario
- design of high-speed driver/receiver will be a major challenge