# Proposal to Develop On-Detector Array-based Optical Link

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- Array-based Optical Links of Present Pixel Detector
- Array-based Optical Links of IBL
- Pros and Cons of Array-Based Optical Link
- R&D Plan
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# Introduction

- VCSEL and PIN are available in three forms:
  - single channel or 4 or 12-channel array
    - array: can reserve 1 in 12 channels for redundancy
    - single channel: double the number of channels for redundancy
      - ⇨ array solution reduces the number of opto-modules to be built by a factor of 22
- sub-detector with data/TTC links spread through out the sub-detector:
  - single channel device is more efficient
- sub-detector with data/TTC links concentrated at few locations:
  - array solution is more efficient (more later)
    - pixel detector: data/TTC links are concentrated at ~ 6 m away

# Optical Links of Present Pixel Detector

- Initially based on SCT design as much R&D had been performed
- Academia Sinica (Taiwan) later suggested
  using arrays to simplify construction
  - proposal was accepted and R&D launched
  - ⇨ fabrication of 272 array based opto-modules (opto-boards)
    instead of 1744 single-channel opto-modules

# Optical Links of IBL

- positive/extensive experience leads us to propose continued use of array-based opto-boards with improvements:
  - replace present opto-pack with new design:
    - use BeO as substrate instead of FR-4 for heat management
    - replace micro soldering with wire bonding
      - cold solder is a major source of failures in present pixel links
  - propose to add redundancy by rerouting signal through a spare VCSEL or PIN channel
  - propose to add individual control of VCSEL current
    - account for optical power spread within an array
      - some present pixel links are difficult to operate

# Opto-Modules Need of IBL

- 28 array-based opto-modules are needed for IBL
  - would have to fabricate 448 single-channel opto-modules (1 PIN + 2 VCSEL) for same functionality
  - special thanks to Tony Weidberg for not insisting on using single-channel solution for the present pixel detector

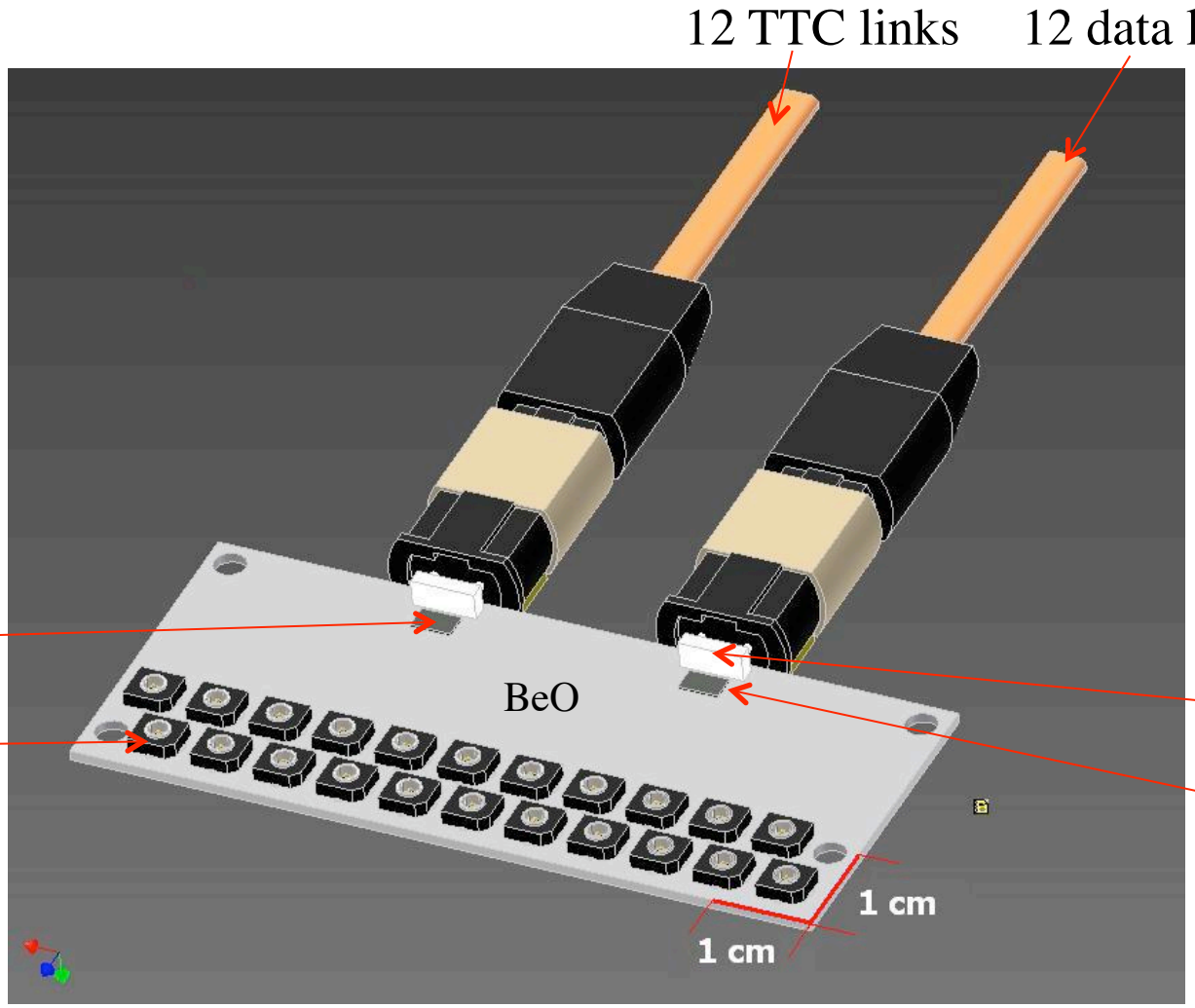
# Pixel Opto-Modules Need at SLHC

- 992 TTC and 992 data links with no bandwidth safety factor
  - 92 array-based opto-modules or 1984 single-channel opto-modules for the same functionality

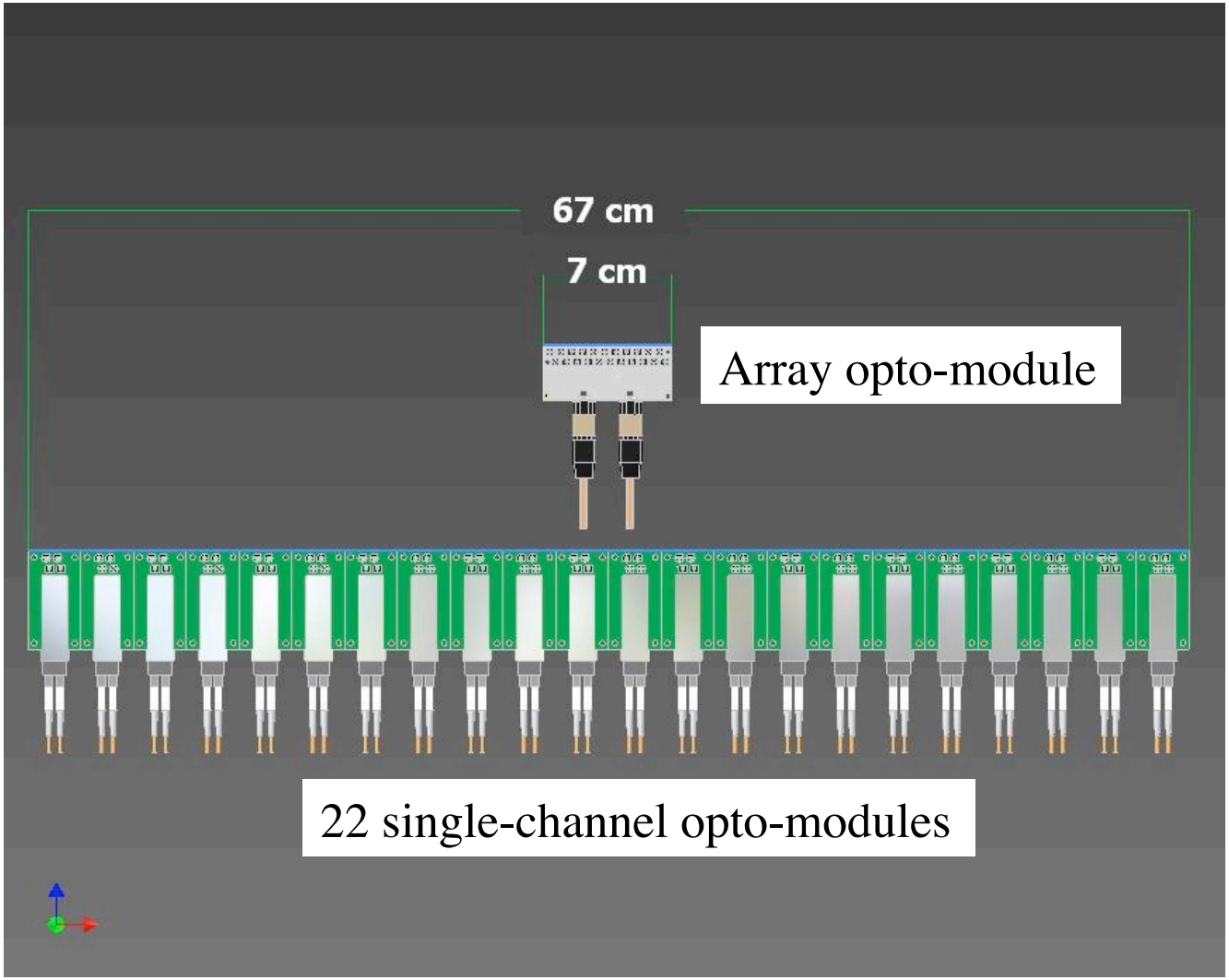
# Pros of Array-Based Optical Link

- highly compact
  - much less material in front of LAr
- simplify fabrication/installation
  - 22 times less opto-modules to build, test, and install
- no ribbon to LC fanout
  - reduce optical power loss
  - simplify installation
- reduce electrical services
  - single power line for receiver/driver ASICs instead of 11 individual power lines
  - single power line for a PIN array instead of 11 individual lines
- simplify cooling
  - cool a small area rather than much larger area
  - consume half as much power

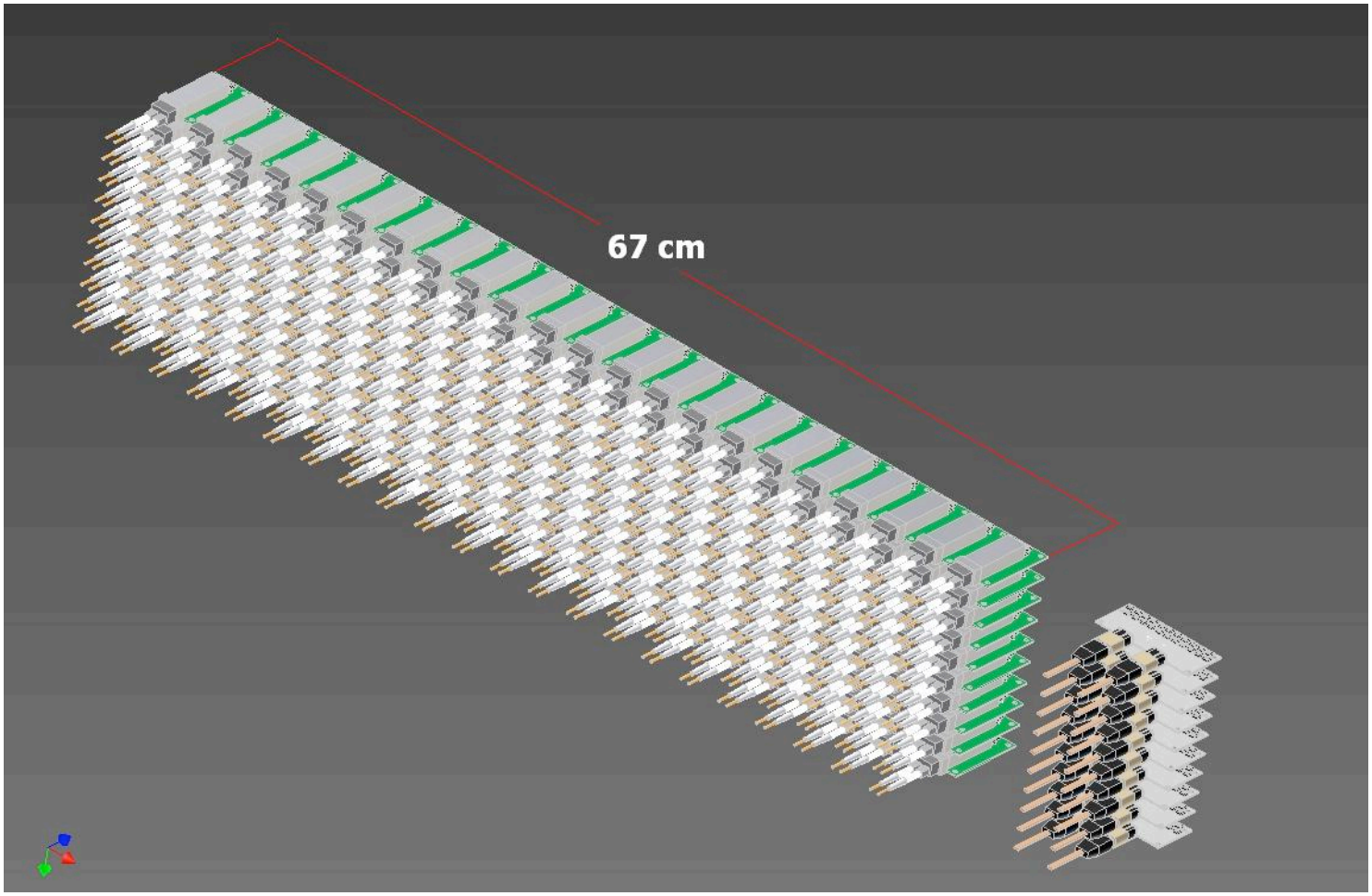
# Array-Based Opto-module



# Array/Single-Channel Opto-Module



# Array/Single-Channel Opto-Module



# Cons of Array-Based Optical Link

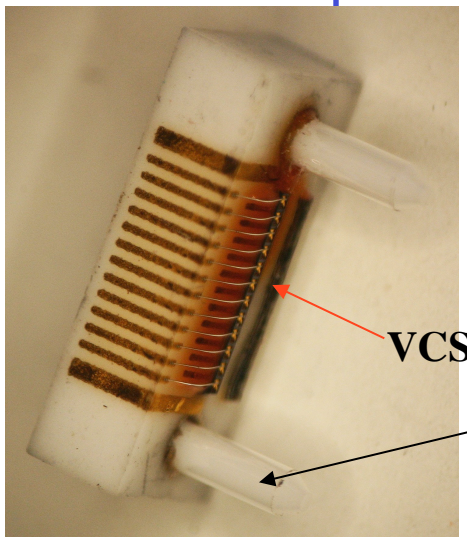
- single point connection failure in power to ASIC or PIN could disable an opto-module
  - opto-modules will be accessible every 1-2 years

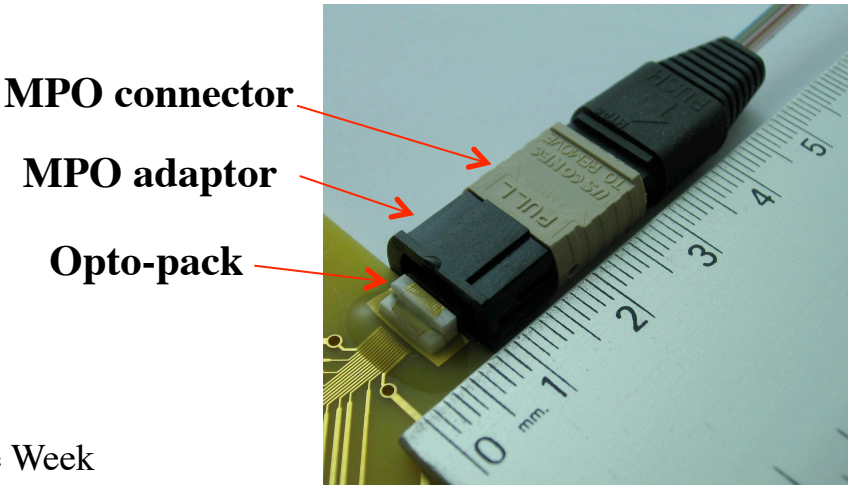
# R&D Plan

- opto-pack R&D plan
- array ASIC R&D plan
- opto-board R&D plan

# Opto-pack R&D Plan

- Large amount of R&D already performed due to IBL
- VCSEL/PINs are aligned at Ohio State University (10-30 minutes)
  - 63 VCSEL opto-packs fabricated
    - 51 opto-packs have optical power > 1 mW @ 7 mA
      - can produce more power as spec on max current is 11 mA
  - 46 PIN opto-packs fabricated
  - Siegen plans to work with IZM on VCSEL/PIN alignment
  - NIKHEF plans to work with industry on VCSEL/PIN alignment

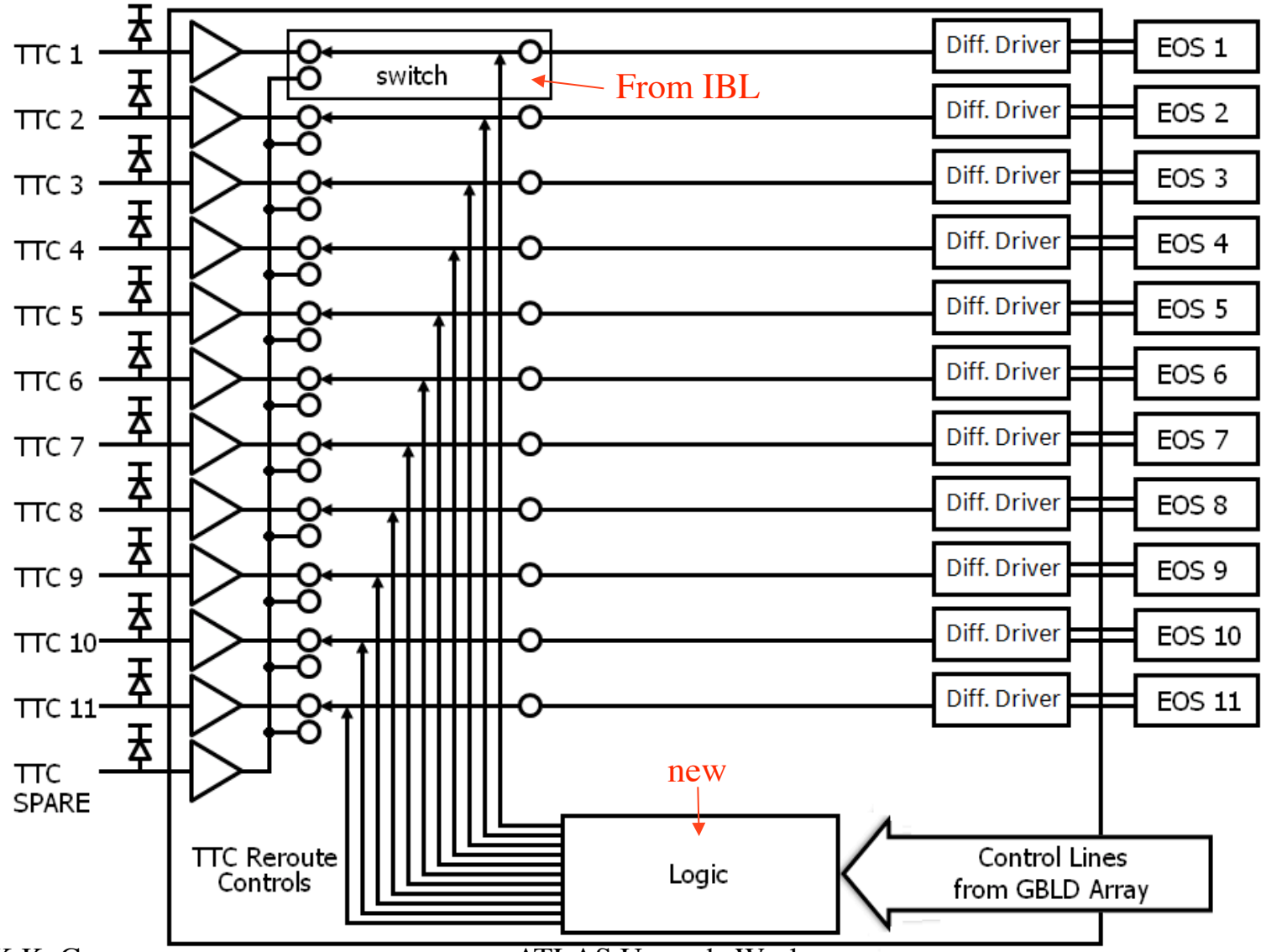


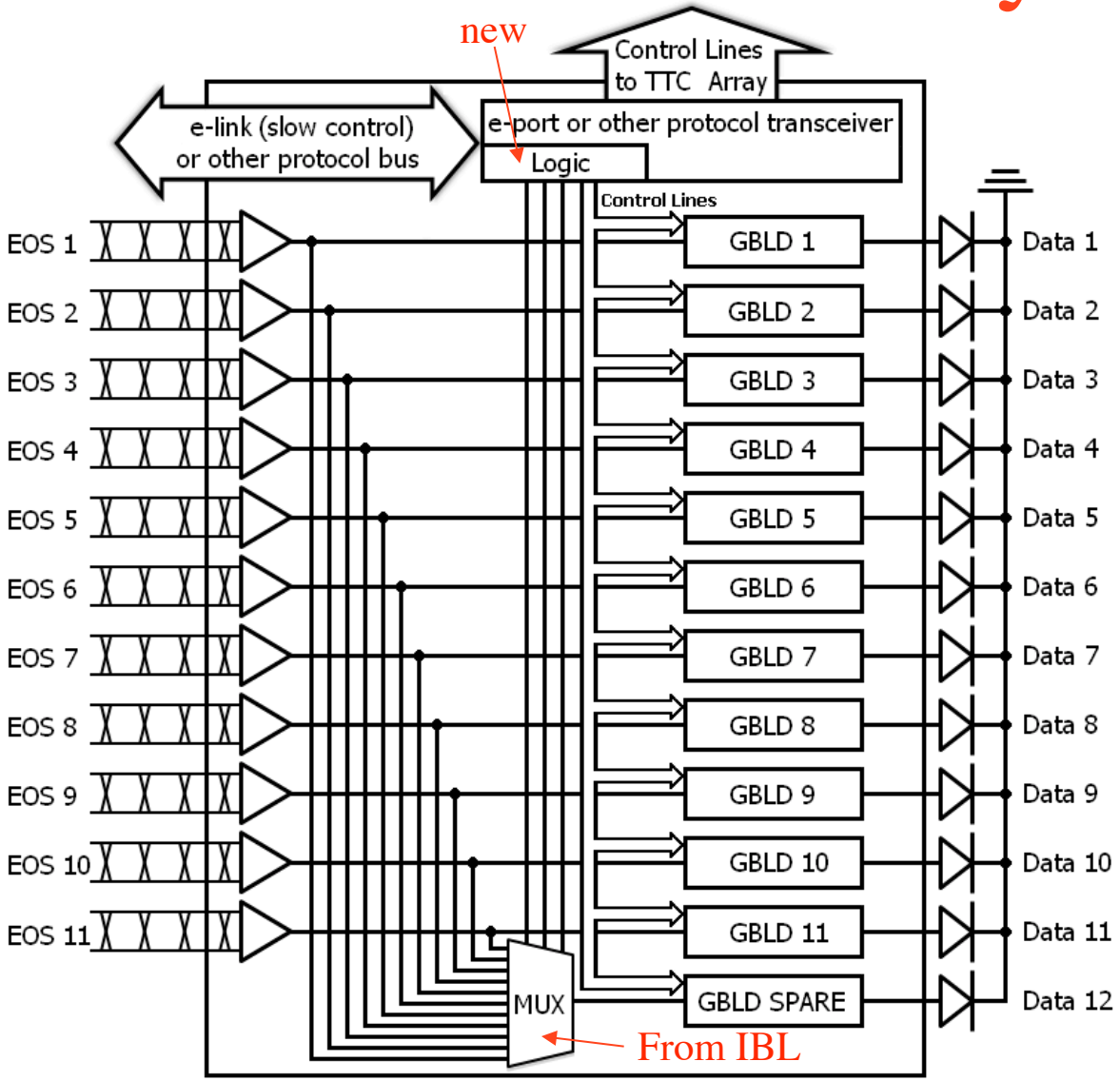
# Array ASIC R&D Plan

- VCSEL driver/PIN receiver developed by GBT/VL must be laid out as an array
  - need to work closely with GBT/VL groups
  - special thanks to P. Moreira for thoughtful advice

# PIN Receiver Array

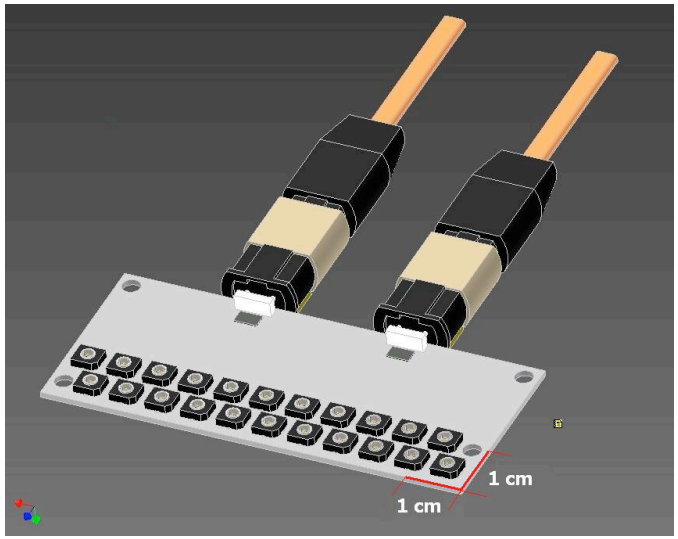


# VCSEL Driver Array



# Opto-board R&D Plan

- pre-emphasized 4.8 Gb/s signals
  in ~6 m micro-coax cables to/from end-of-stave
  - need to ensure that the signals are not compromised
    in last 2 cm between coax connectors and array ASIC
  - must use RF design in board layout



# R&D Schedule

- Phase I:
  - 11/2010: 4-channel ASIC submission
  - 03/2011: prototype high-speed opto-board with FR4
  - 07/2011: irradiation of opto-board with array ASICs
    - test radiation hardness and SEU tolerance
- Phase II:
  - 11/2011: 12-channel ASIC submission
  - 03/2012: improved prototype high-speed opto-board
  - 07/2012: irradiation of opto-board with array ASICs

# R&D Resources

| | Tech.* | Eng.* | Experience/Comments |
|---|---|---|---|
| OSU | 0.5 | 0.5 | designed DORIC/VDC + designed/produced opto-boards |
| Siegen | 0.3 | 0.7 | designed DORIC/VDC + designed/produced opto-boards |
| Wuppertal | 0.5 | 0.4 | produced opto-boards + designed/produced off-detector links |
| NIKHEF | 0.5 | 0.5 | LHCb |

* FTE for technicians and engineers. In addition, physicists (students, post-docs etc) contribute to the R&D.

# Summary

- on-detector array-based optical links have many advantages
- a team with extensive experience with array-based opto-links at LHC proposes to develop array-based opto-links for SLHC pixel detector
- modest effort is needed to prove the feasibility
  - feasibility can be tested with 4-channel array by 2011