Radiation-Hard/High-Speed VCSEL Array Driver

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Outline

- Introduction
- Preliminary design of 10 Gb/s VCSEL array driver
- Summary

Use of VCSEL Arrays in HEP

- Widely used in off-detector (no radiation) data transmission
- First on-detector implementation in pixel detector of ATLAS
  - experience has been positive
    - VCSELs used are humidity sensitive but they were installed in very low humidity location
    - modern VCSELs are humidity tolerant
    - opto-boards removed last summer
      - opto-boards built by OSU have ~0.1% broken links
    - new opto-boards will be installed in a more accessible location
    - new opto-boards will use arrays, including the new layer (IBL)

Opto-Links for Phase II Pixel Detector

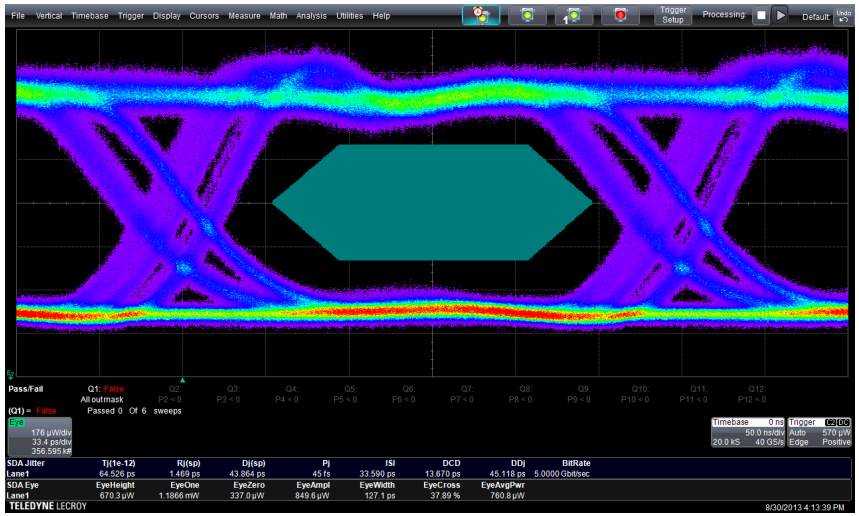
- opto-links will be located away from IP after 5 m of electrical cables
- logical to continue the use of arrays due to space limitation and the positive experience, including the ease of handling
  - joint ATLAS/CMS proposal to develop array-based solution is funded by US DOE generic R&D program for three years

Results on 5 Gb/s VCSEL Driver

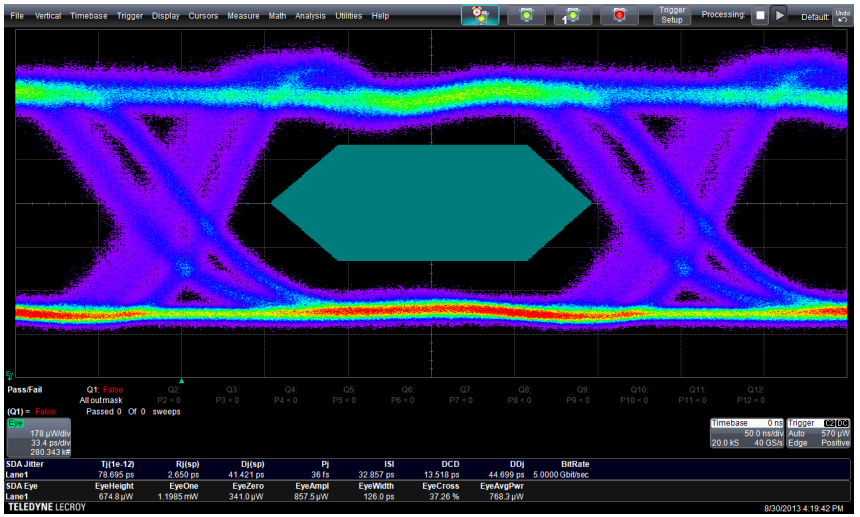
- 12-channel VCSEL array driver designed using 130 nm CMOS
- Incorporate improvements taking advantage of experience from 1st generation opto-links:
  - redundancy to bypass a broken VCSEL
  - power-on reset in case of communication failure:
    - no signal steering
    - 10 mA modulation current (on current)
    - 1 mA bias current (off current)
- All functionalities successfully implemented
- Performance at 5 Gb/s is satisfactory

Effect of Steering on Optical Eye Diagram

Spare 1 output with other channels off



Spare 1 output with all channels active

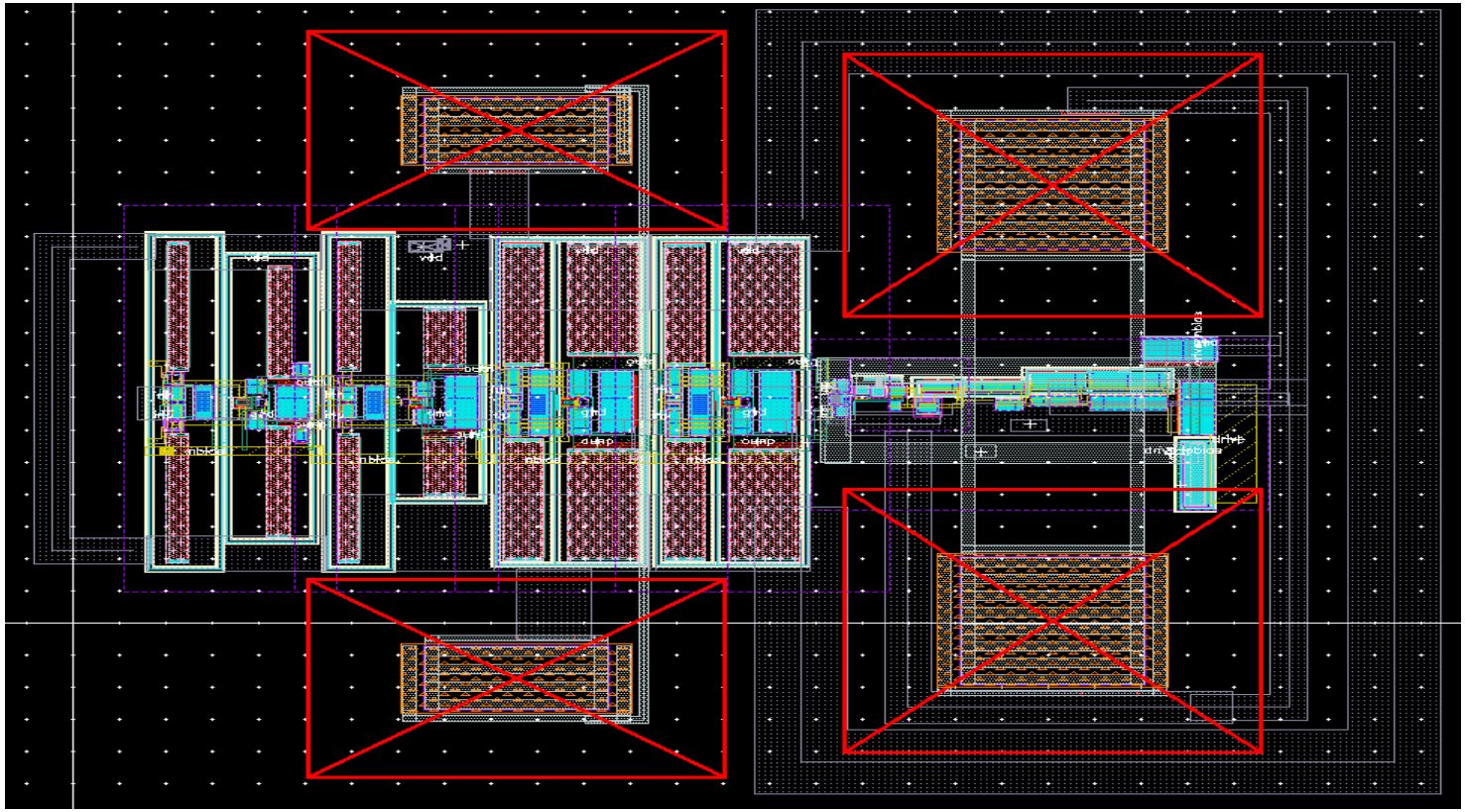


- steered channel still passes the mask test
  - jitter increases with all channels active

10 Gb/s VCSEL Driver Status

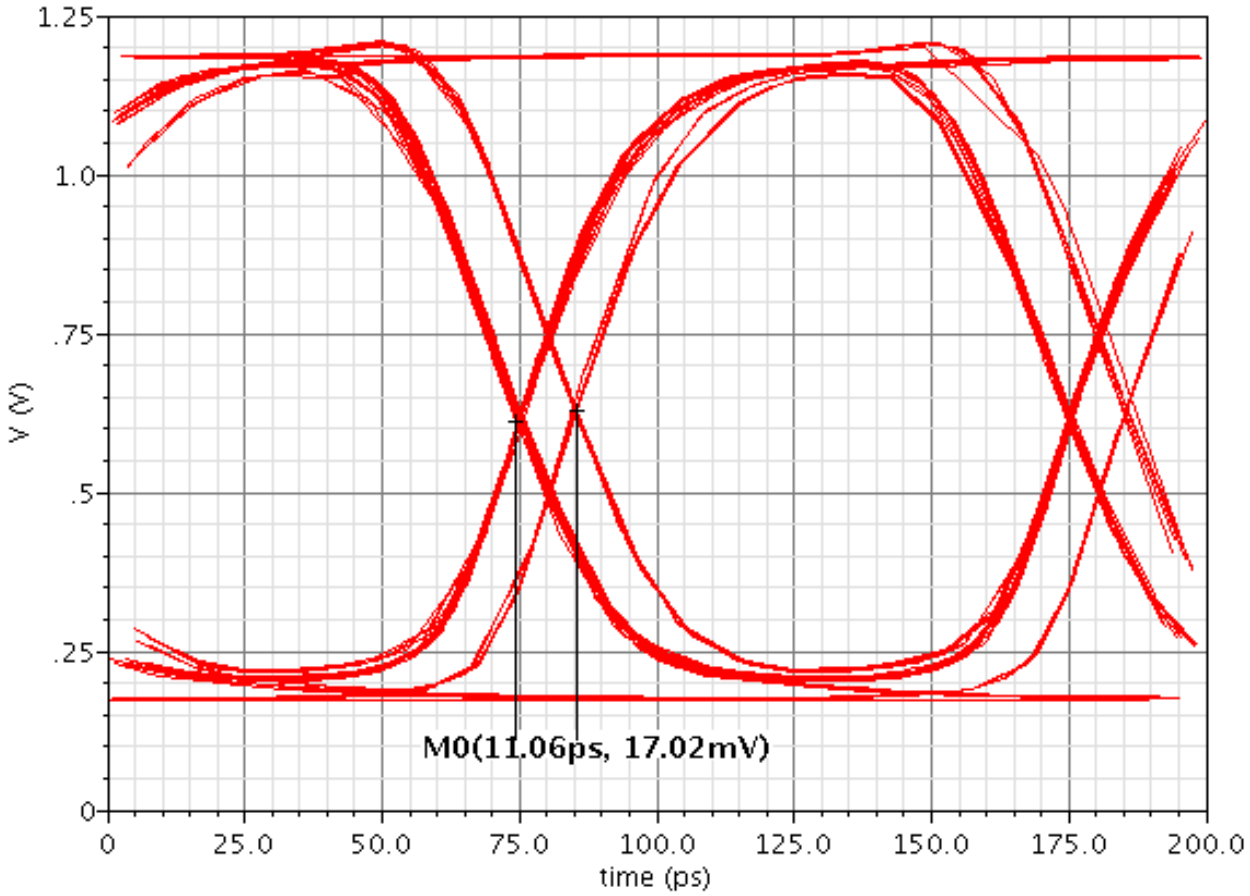
- Complete layout without bond pads is functional but has high jitter: 23 ps
- Total current consumption ~40 mA
  - 18 mA for the receiver
  - 20 mA for the output driver

Layout

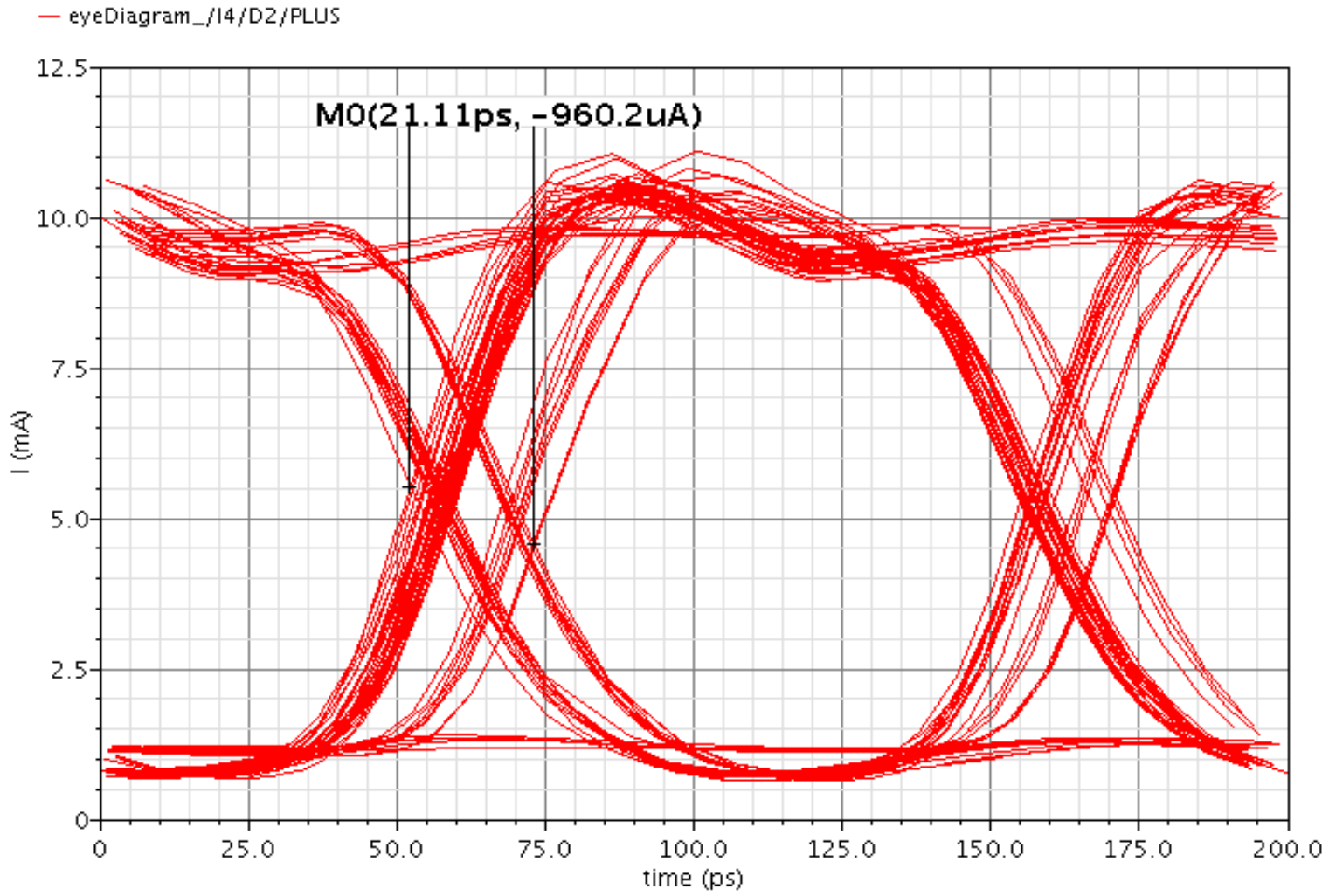


150 μm x 125 μm

CML Receiver Output



VCSEL Driver Output Current



Future Plan

- Submit a 4-channel version for fabrication in June
  - delivery of ASIC in early September
  - irradiation in late September