Measurement of VCSEL Lifetime on Opto-Boards

K.K. Gan
The Ohio State University

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Outline

- Tests at Siegen/CERN
- Test at Ohio State
- Discussion of proposed sample allocation

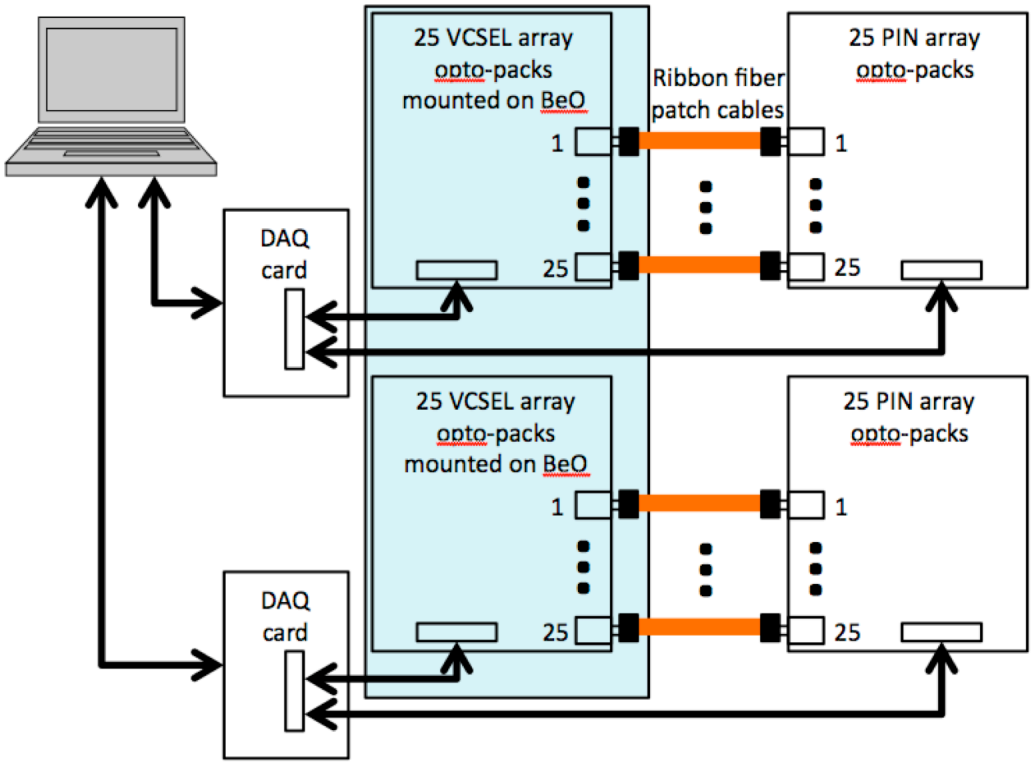
Lifetime Test of Truelight VCSEL

- Priority of various tests is to measure lifetime of installed VCSELs
  - understanding failure mechanism is of low priority
- Siegen is performing test of four opto-boards
  - transmitting clock (50% duty cycle) at room temperature
    - Wuppertal will measure optical spectrum monthly
    - status: operational since July
- Similar study of 6-7 boards on test system at CERN
  - transmitting clock at all times
    - will measure optical spectrum monthly
    - status: 6 boards operational since late August

VCSEL Lifetime Test of at Ohio State

- Ohio State has found ~50 VCSEL arrays from original production
  - 400 channels will be monitored
    - represents a significant fraction of final system: 1,788 channels
      - ⇨ no need to use thermal acceleration
    - ~50% have improperly cured epoxy
  - will mount VCSEL on BeO board to emulate detector environment
  - will keep chamber at ~20^0 C flushed with N_2
  - will transmit bursts of 80 Mb/s pseudo-random data
    - burst duration: adjustable
    - burst repetition rate: ~100 KHz
  - can measure light-current-voltage (LIV) curves as needed
  - will measure optical spectrum monthly
    - will perform more frequent measurements during first month

Test Setup



- Design of various PCBs in progress
- Most components are on order
  - BeO boards delivery time: 8 weeks
    - vendor has expedited the fabrication

Proposed Sample Allocation

Duty Cycle (%)	~0	25	50	100
Arrays	272	2	46	2

Installed opto-boards

- Requested some Truelight VCSEL arrays as control sample
  - awaiting delivery confirmation
- Must perform post-mortem of all initial failures to exclude any ESD induced fatality
- Spectrum measurements will qualitatively verify the degradation vs. duty cycle
- We can't do everything we wish to do without sacrificing the statistical precision of lifetime measurement

Mitigation

- VCSEL lifetime can be extended with following adjustments
  - operating at lower temperature
    - current operating temperature is already optimized
  - operating at lower drive current
    - strongly coupled with operating temperature
    - not much room for further adjustment
  - operating at 80 Mb/s to reduce transmission duration
    - implemented
  - turn off one of the two links on B layer
    - no net gain in lifetime as
      total amount of data transmitted remains unchanged

25% vs. 50% Duty Cycle Sample

- Priority is to verify as soon as possible whether failure rate of VCSEL on opto-boards is same as those of TXs
- Should we split the sample into two to run at 25% and 50% duty cycles?
  - Cutting sample by half increase the chance of being victim of statistical fluctuation
  - Lifetime prediction based on 50% duty cycle gives most pessimistic prediction?

Lifetime Dependence on Temperature

- Temperature of opto-boards can be adjusted by few degrees
  - average temperature: 17 C
  - maximum temperature: 22 C
  - Arrhenius acceleration factor should be very modest
    - anybody interested to measure Arrhenius factor of current TX VCSELs to see how well it works?
  - should some opto-board arrays be operated at different temperature or just measure lifetime at 22 C?
    - minor detail: need to buy an environment chamber for this study

Lifetime Dependence on Current

- Expect to operate VCSELs at about same drive current over time due to self annealing of radiation damage
- To see lifetime dependence on drive currents requires operating two samples at very different currents
  - should some arrays be allocated for this?