Optical Link Architecture
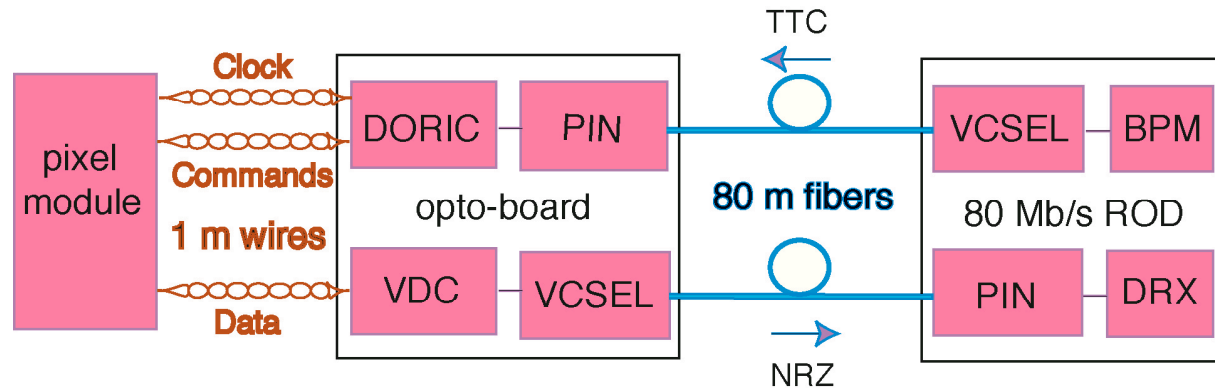
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March 22, 2007

Opto-link Architecture

- 272 opto-boards
  - 2240 data links
 - 1904 TTC links

MCC/Opto-Chip Connections

- use micro twist-pair wires

  for transmission between MCC and opto-chip

  ⇨ decouple production of pixel modules and opto-boards

- opto-boards located at patch panels (PP0)

  ⇨ much reduced radiation level

  ◆ 10 years: 17 Mrad or 3.7 x 10^{14} 1-MeV n_{eq}/cm^2

Fibers

- use two kinds of fibers fusion spliced together:
    - 8 m of rad-hard/low-bandwidth SIMM fiber ribbon
   - 70 m of rad-tolerant/medium-bandwidth GRIN fiber ribbon

VDC: VCSEL Driver Circuit

- Convert LVDS input signal into single-ended signal appropriate to drive VCSEL diode

- Output (bright) current: 0 to 20 mA
  - ◆ controlled by external current I_{set}

- Standing (dim) current: ~ 1 mA
  - ◆ improve switching speed

- Rise & fall times: 1 ns nominal

- "On" voltage of VCSEL: up to 2.3 V at 20 mA for 2.5 V supply

- Constant current consumption!

- Use IBM 0.25 μm CMOS

- Use Truelight high-power oxide common cathode VCSEL array
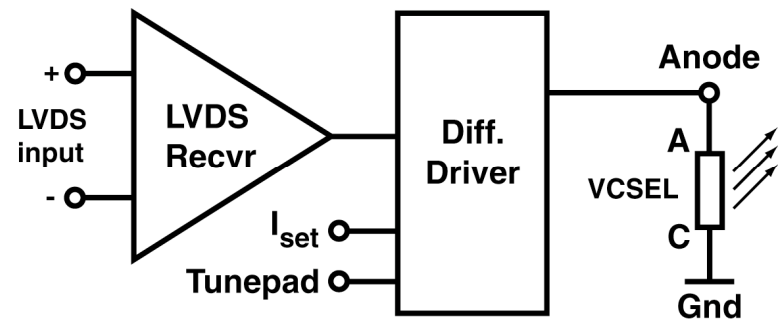
DORIC: Digital Optical Receiver IC

- Decode Bi-Phase Mark encoded (BPM) clock and command signals from PIN diode

- Input signal: 40-600 μA

- Extract: 40 MHz clock

- Duty cycle: (50 ± 4)%

- Total timing error: < 1 ns

- Bit Error Rate (BER): < 10^{-11} at end of life

- Use IBM 0.25 μm CMOS

- Use Truelight common cathode PIN array

40 MHz clock

command

BPM
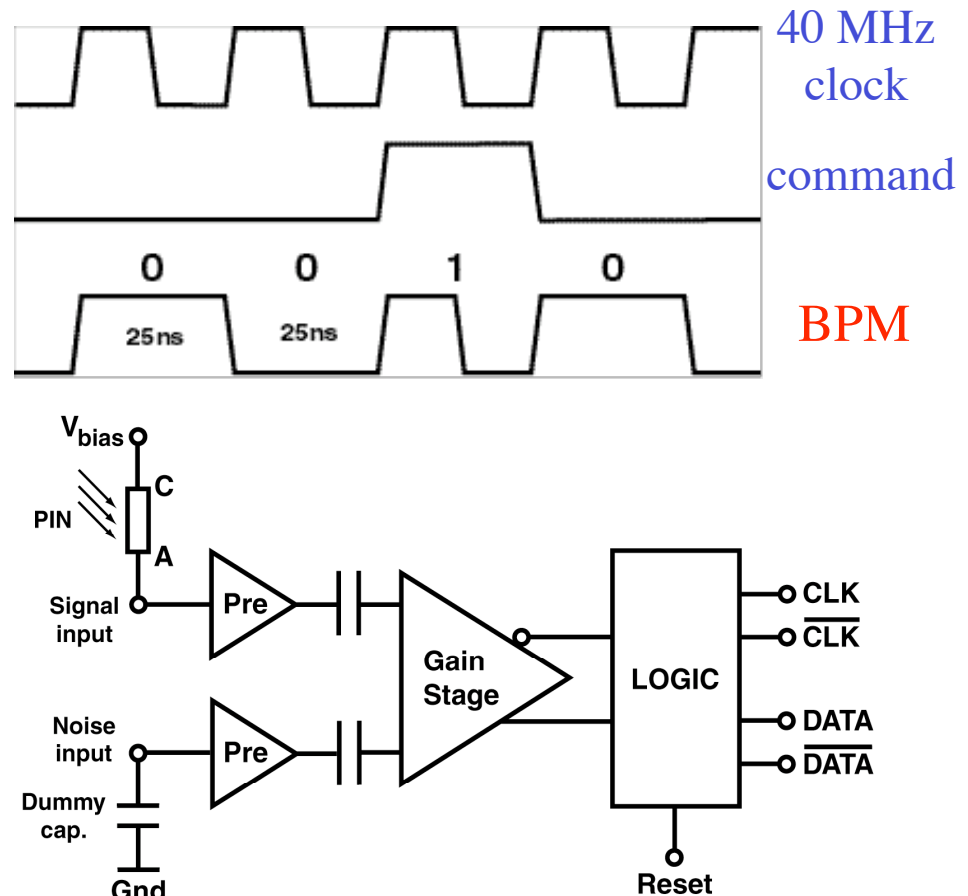
Opto-board

- converts: optical signal ↔ electrical signal

- contains 7 TTC and 7 data links

- B-layer opto-board contains extra 7 data links
    - ⇨ total bandwidth: 160 Mb/s

- use BeO for heat management

BeO Opto-board

VCSEL opto-pack

housing

2 cm

PIN opto-pack

VDC

DORIC
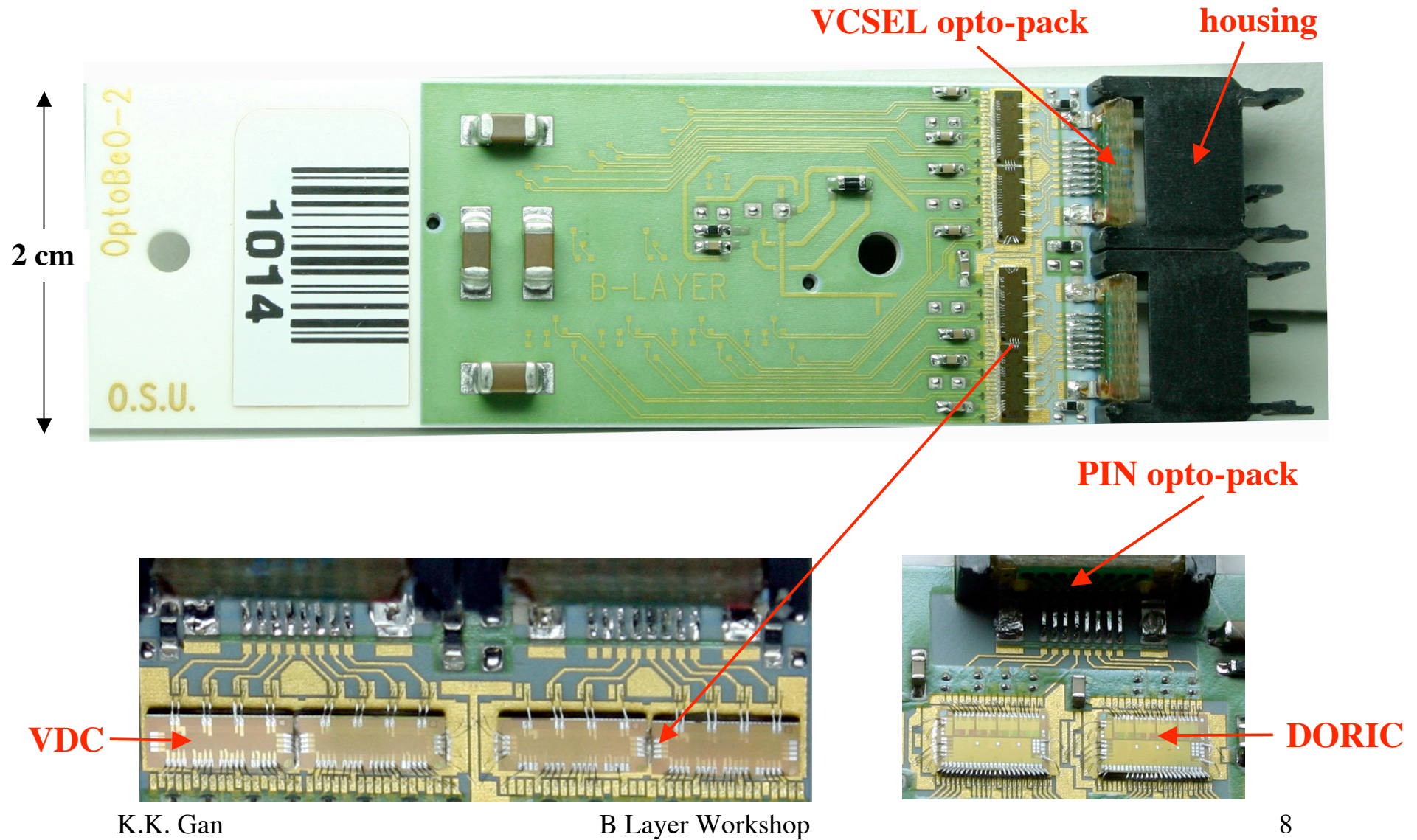
What Have We Learned?

✔ micro twist-pair wires:

  ◆ decouple production of pixel modules and opto-boards

  ◆ much reduced radiation level

✔ detachable fiber ribbon:

  ◆ ribbon is much less fragile than single fiber

  ◆ no single fiber pigtail to break

⇨ four separately produced/replaceable components:

  ◆ module + twist pair + opto-board + ribbon

  ◆ should preserve this modularity for ease of production/installation (reduce cost) for somewhat lower bandwidth (increase cost)

What Have We Learned cont…

✘ need longer term study with larger sample

   ◆ only three VCSEL opto-packs were monitored over one month

   ◆ VCSEL arrays develop common serial resistance

     ⇨ not enough voltage to drive VCSEL to produce light

✘ need much better QA on opto-packs

   ◆ better control of conducting epoxy thickness and curing

   ◆ better tracking of dice/wafers

✘ system test with production components before large production

   ◆ bypass cap not mounted on VISET for fear of developing leak

     ⇨ noise not observable during QA due to low-noise test system

   ◆ slow turn-on VCSEL not detectable without production fibers

     ⇨ should continuously transmit data to VCSEL

   ◆ PP0 operating cooler than anticipated with little temp control