Tracker Optical Link Upgrade Options and Plans

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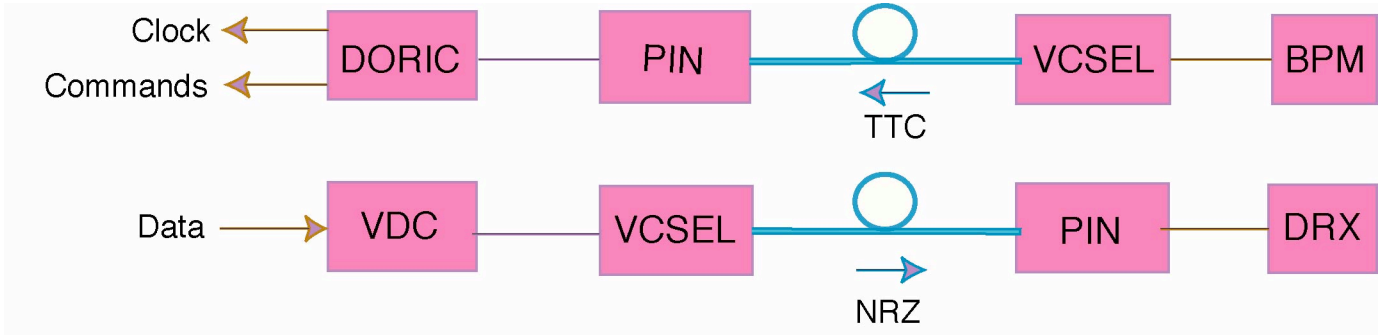
Outline

- current pixel/strip opto-links
- lessons learned
- upgrade options
- summary

Inner Detector Optical Links

- SCT: ~ 12,000 links, including data transmission redundancy
- Pixel: ~ 4,000 links
  - based on SCT design
- both use driver/receiver of similar architect:
  - VDC: VCSEL Driver Circuit
  - DORIC: Digital Optical Receiver Integrated Circuit

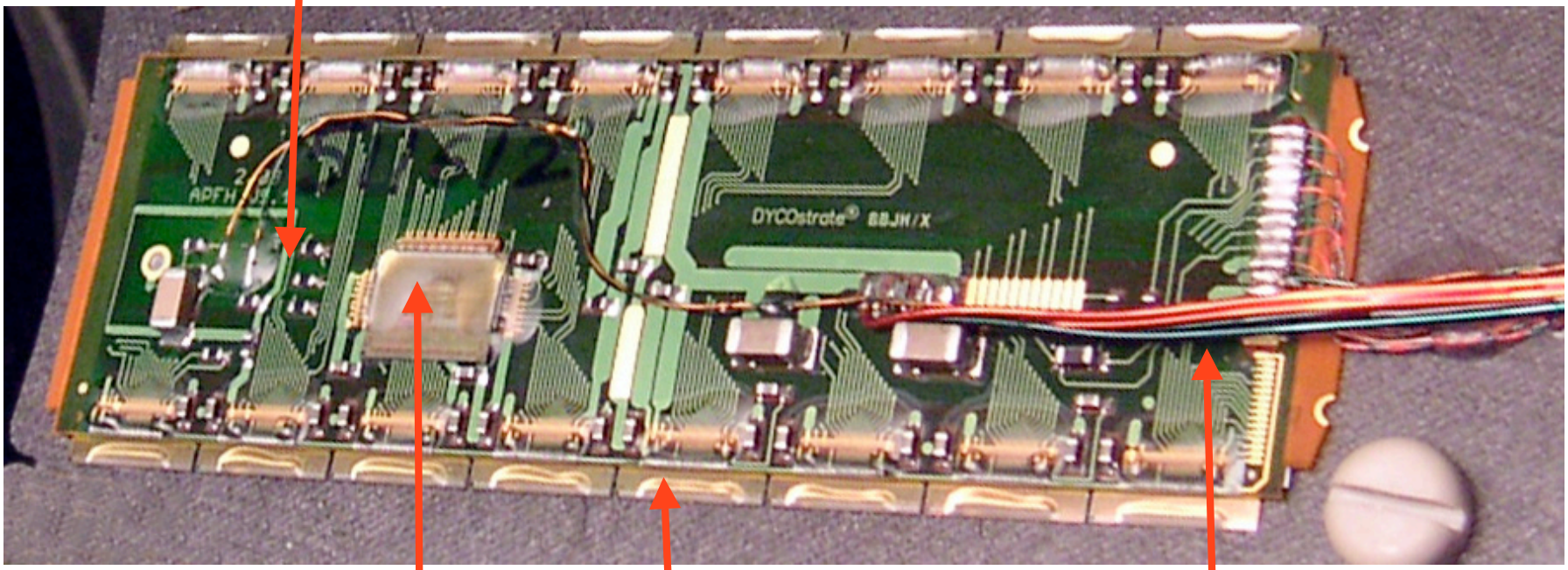


Inner Detector Optical Chips

- SCT:
  - AMS 0.8 μm bi-polar
  - VDC: two channels/chip
  - DORIC: one channel/chip
  - optical package: 2 Truelight VCSELs + 1 Centronic PIN
    - use two data links for redundancy
  - speed: 40 Mb/s
- Pixel:
  - IBM 0.25 μm CMOS
  - four channels/chip
  - optical package: 8-channel Truelight VCSEL/PIN arrays
  - speed: 80 Mb/s using both clock rising/falling edges
    - B-layer uses two data links to transmit at 160 Mb/s

Pixel Module

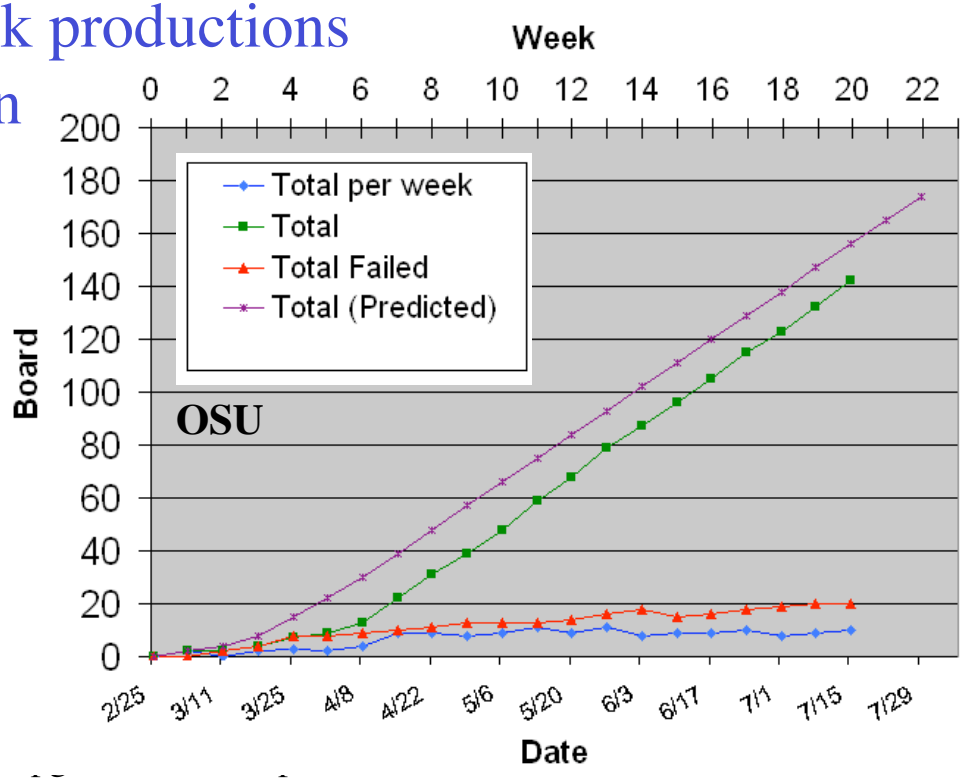
Original opto-link location
(two single fibers)



MCC **FE (16)** **Type 0 cable**

Optical Link/FE Connections

- SCT:
  - use short flex to avoid electromagnetic interference
- Pixel:
  - use ~ 1 meter of micro-twisted pairs (60 and 100 μm)
  - ⇨ decouple module & opto-link productions
  - ⇨ greatly simplify construction
  - ⇨ 2 BeO board flavors
  - ⇨ few production problems



SCT Optical Harness

- complicated designs
  - difficult to assemble with high yields
  - large number of flavors
- non-modular design
  - difficult to replace any component that fails
- single fiber is fragile
  - pixel uses 8-fiber ribbon

⇨ prefer upgraded link to be similar to pixel with ~ 1 m of wire link

ID Fluences at SLHC

- estimated fluences in 10^{15} 1-MeV n_{eq}/cm^2 after 5 years:

	Si	GaAs
B-layer	20	160
Layer 1	7.5	53
Layer 2	4.0	23
PP0	2.5	14
SCT1	1.6	7
SCT4	0.9	3

← current pixel opto-link

Data Bandwidth at SLHC

- SCT:
  - current module: 12 cm long strips
  - ⇨ SLHC module: 3 cm (inner) and 12 cm (outer)?
    - bandwidth/module: 40 Mb/s
- Pixel:
  - current pixel: 50 μm × 400 μm
  - ⇨ ~ 3 times finer segmentation?
    - ⇨ charge sharing produces ~30% more hits
    - bandwidth/module:
      - B-layer = 1.3 × [10/3] × 160 Mb/s = 700 Mb/s
      - outer layer/disk = 1.3 × [10/3] × 80 Mb/s = 350 Mb/s

Upgrade Wishes

- prefer ~ 1 m of wire link between FE and opto-link
  - decouple module and opto-link production
    - ⇨ simplify construction and improve yield
  - much reduced radiation level
- highly desirable for upgraded pixel and SCT to use as much common components as possible
- but vastly different data bandwidth
  - SCT: 40 Mb/s
  - Pixel: 350/700 Mb/s
    - ⇨ adapt solution similar to GOL chip of LHCb?

GOL-like Solution for SCT?

- GOL (Gigabit Optical Link) chip:
  - serialize 32 links of 40 Mb/s to transmit at 1.28 Gb/s (effective)
- connect half a stave to a GOL-like chip for SCT?
  - serialize 24 links of 40 Mb/s to transmit at 960 Mb/s?
  - inner SCT: 24 pairs of wires from modules to GOL at end of stave
  - outer SCT: 6 pairs of wires/half stave (4 half staves/GOL)
    - material contribution from wires
  - ✔ ~ 6 × reduction in fiber count from current SCT
  - × messy to connect a small chip to 24 pairs of wires
  - × input speed too slow for pixel opto-link
    - not a common solution for pixel and SCT
- GOL-like solution is probably not desirable

MCC-like Solution for SCT?

- MCC (Module Control Chip):
  - serialize 16 FEs on a pixel module to transmit at 80/160 Mb/s
- opto-board at end of stave connects to 8 MCCs via wires
- inner SCT: one MCC serving eight 3-cm modules?
  - MCC is mounted along stave
  - MCC connects via flex to 8 FEs
    - connection more complex if modules are not coplanar
  - half stave: 3 pairs of wires from MCC to opto-board
- outer SCT: one MCC serving eight 12-cm modules?
  - MCC is mounted near end of stave
  - MCC connects via wires to 8 FEs on two half staves?
  - half stave: 6 pairs of wires from FEs to MCC
- transmits data at 320 Mb/s (8 × 40 Mb/s)

✔ ~ 8 × reduction in fiber count from current SCT

MCC-like Solution for SCT (cont.)?

- outer SCT: opto-board supports ~ 11 half staves
- inner SCT: opto-board supports ~ 3 half staves
- Pixel: opto-board supports 6-7 modules on 1 half stave (current)
  - VCSEL/fiber ribbon contains 8 channels
  - ⇨ waste of space and bandwidth!
  - should avoid this early in the design!

⇨ common solution for pixel and SCT operating at 320 Mb/s

- compatible with estimated bandwidth of 350 Mb/s for pixel

How to use 10 Gb/s Opto-link?

- 250 pairs of wires carrying 40 Mb/s
  from SCT to 10 Gb/s driver is unrealistic
- need MCC-like chip for SCT/pixel
  - 32 pairs of wires from MCCs operating at 320 Mb/s
  - ✔ reduce fiber count by factor of ~ 250 from current SCT
    and 32 from current pixel system
  - × very high reliability is needed since a link
    covers ~ 11% of the solid angle of a B-layer!
    - must survive 10 m drop and run over by a truck (lorry)
  - need to use single mode fibers for high speed transmission
    - VCSEL to fiber alignment much more challenging
  - × expensive to develop custom rad-hard/compact 10 Gb/s link
  - × expensive to equip multiple sites with 10 Gb/s test system

Silicon-on-Sapphire Alternative

- integrated serializer, driver, VCSEL
  in single chip to operate at 3-10 Gb/s
  - integration of driver/VCSEL is unique in SOS
    - current opto-board uses short on-board connections
  - serializer/driver integration is not unique and may not be optimal
  - expect to be radiation hard and less sensitive to SEU
    - validation with irradiation needed
  - need to develop efficient/compact VCSEL/fiber coupling
- SMU works in close collaboration with Peregrine and SMIC

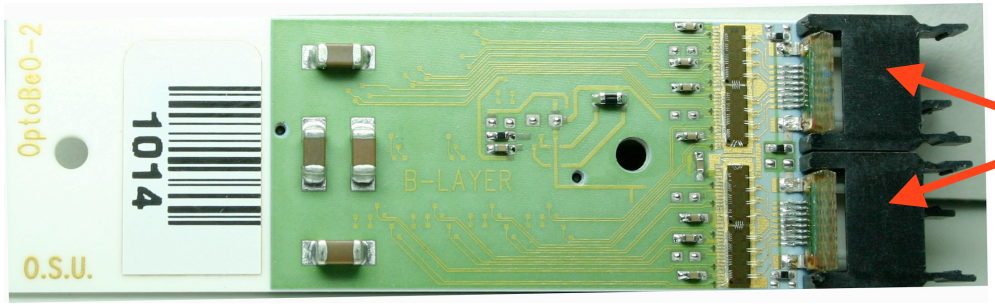
TTC Upgrade Scenarios

- TTC: Timing, Trigger and Control signals
- present system: 1 TTC link for each SCT or Pixel module
  - ◆ data is bi-phase mark encoded with 40 MHz clock
  - × would require much more TCC fibers for inner SCT
- SCT with MCC as in Pixel system?
  - ◆ one TTC link for 8 SCT modules
  - ✔ ~ 8 × smaller TTC fiber count than current SCT
- regenerate TTC for 8 links on an opto-board?
  - ✔ another 8 × reduction in TTC fiber count
    - ■ current opto-board provides TTC and data links to same module
    - × need TTC only opto-board to use ribbon instead of single fiber
  - × require highly reliable links
  - × no clock phase adjustment for each MCC
  - × more sensitive to SEU for transferring 8 × more TTC bits

Upgrade TTC Speed

- upgrade: low speed link?
  - ✔ low sensitive to SEU which changes only one data bit
  - ■ generate ~ 8 × faster clock in MCC
  - ■ is it fast enough to reconfigure FE/MCC due to SEU during data taking with causing deadtime?
- upgrade: high speed link?
  - × more sensitive to SEU which could change multiple bits
  - ✔ fast reconfiguration of FE/MCC due to SEU

More Channels/Volume for Pixel Link?



VCSEL opto-pack

- opto-board: 2 VCSEL + 1 PIN opto-packs
- upgrade opto-board: half as wide only 1 VCSEL + 1 PIN opto-packs
  - B layer: 1 standard board + 1 board with 1 VCSEL opto-pack only

  ⇨ ~ 2 × more links per unit volume
- use 12-channel VCSEL/PIN/fiber ribbon
  - slight larger ribbon cable as cladding is most of the material
  - can't reuse current 8-channel fiber ribbons
  - current pixel system uses ~ 6.4 channels/ribbon!

  ⇨ ~ 1.5 × more links per unit volume
- total: ~ 3 × more links per unit volume

Optical Link/MCC Connections

- pixel: connect MCC to opto-link via 1 m of 100/60 μm wires
- can these wires transmit signal at ~ 320 Mb/s?
  - if not, what is the minimum radius?
  - what is the minimum radius for various possible upgrade transmission speeds?
  - ⇨ OSU has started on the testing program

Requirements for Fibers

- single mode fiber (ϕ 6 μm):
  - no modal dispersion: high bandwidth
  - × require precise alignment to VCSEL
- multi-mode fiber (ϕ 50/62.5 μm):
  - SIMM: rad-hard pure silica core, low bandwidth
  - GRIN: rad-tolerant, medium bandwidth
- present pixel: spliced several meters of SIMM with GRIN
  - what is the maximum bandwidth?
    - ⇨ OSU has started on this testing
  - radiation hardness of the SIMM fiber
    - ⇨ Oxford/Taiwan/SMU plans to irradiate various fibers

Radiation Hardness of VCSEL/PIN

- VCSEL/PIN from several vendors can operate at Gb/s
  - can it survive SLHC dosage?
    - what is the optical power of VCSEL after irradiation?
    - can VCSEL be annealed after irradiation?
      - what is the VCSEL current needed for annealing?
    - OSU plans to characterize VCSEL/PIN from various vendors
    - Oxford/Taiwan has started irradiation at Ljubljana
    - OSU/Siegen/Oklahoma plan to do irradiation at PS in 2006

Opto Driver/Receiver for SLHC

- pixel VDC/DORIC were fabricated using 0.25 μm technology
  - VDC needs to operate at > 320 Mb/s
    - should design VDC to operate as fast as possible
  - convert to 0.13 μm as planned for FE?
- producing enough voltage to driver VCSEL is a challenge:
  - Truelight VCSEL needs ~1.9 V to produce 10 mA
    - higher current is needed for efficient annealing
  - operating voltage of 0.13 μm chip is 1.2 V
    - thick oxide can operate at 2.5 V
    - ⇨ need to test irradiation hardness of thick oxide chip
- OSU/Siege plan to design/prototype/irradiate the chips

Summary

- upgrade based on current pixel system is a natural path:
  - use “MCC” to serialize 8 modules for SCT
  - operating at ~ 8 × faster (320 Mb/s per link)
  - ease of construction with opto-link mounted off modules
  - common solution for pixel and strip
- silicon-on-sapphire provides an alternative which integrates chips and optical devices together operating at 3-10 Gb/s
- several groups already started on R&D
- modular of 6 and 7 is wasteful in space and bandwidth
  - let’s don’t it again!