Status of Optical Electronics

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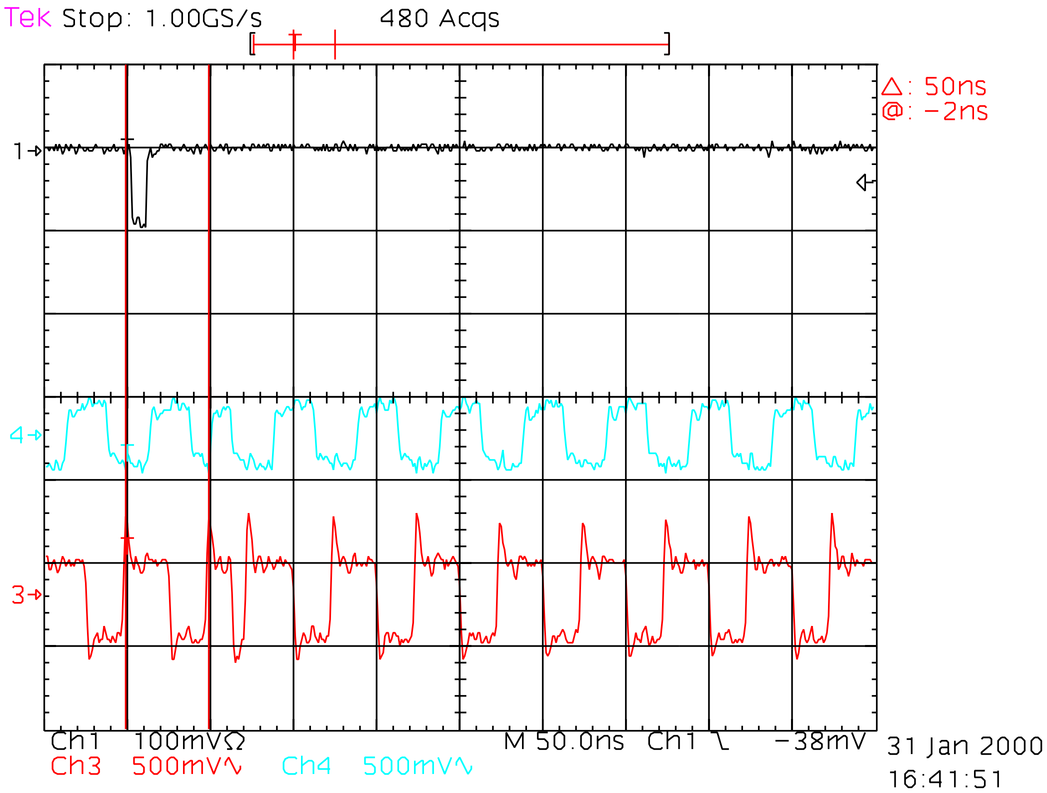
ATLAS Pixel Week

VCSEL Driver Chip

- VDC converts LVDS signal into appropriate signal to drive VCSEL
- VDC work!
- more detailed investigation in progress...

VDC


Tek Stop: 1.00GS/s
480 Acqs
Δ: 50ns
@: −2ns
Ch1 100mVΩ
M 50.0ns Ch1 ∖ −38mV
Ch3 500mV∿ Ch4 500mV∿
31 Jan 2000
16:41:51

Status

- V_{bias} generating circuit oscillates
  - ◇ 320 mV @ 1.6 MHz on 1.5 V
- simulation shows RESET is low when powered up
  - → should RESET be high when powered up?
  - → design error in start-up circuit?

Status

- oscillation can be cured by connecting RESET to VDD or ground
  - ◇ much time lost (include 2 ion beam surgeries)
    due to drawings received at OSU has no RESET
- clock can be decoded at 40 MHz but not stable
- data also get decoded occasionally
- currently comparing test points with simulation
  - ◇ outputs from initial stages (*preamp* and *edge_detector*) looks ok
  - ◇ investigation continue...