Status of Optical Electronics

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Opto-electronics Team

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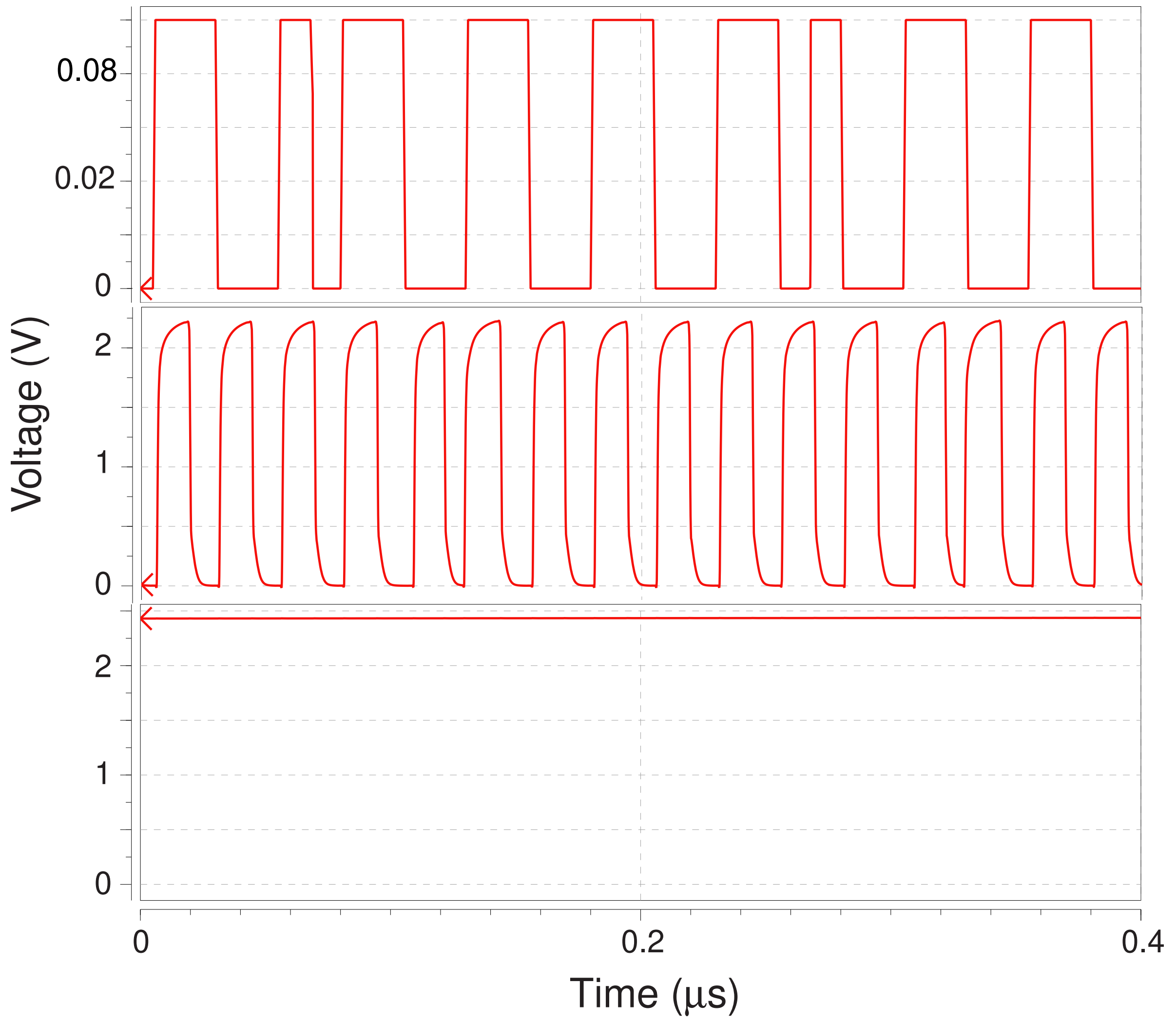
Original Simulation of DORIC-P1

- DORIC-P1 failed to simultaneously decode data and clock
- simulation predicted proper working of DORIC-P1
- simulation was based on schematic

New Simulation of DORIC-P1

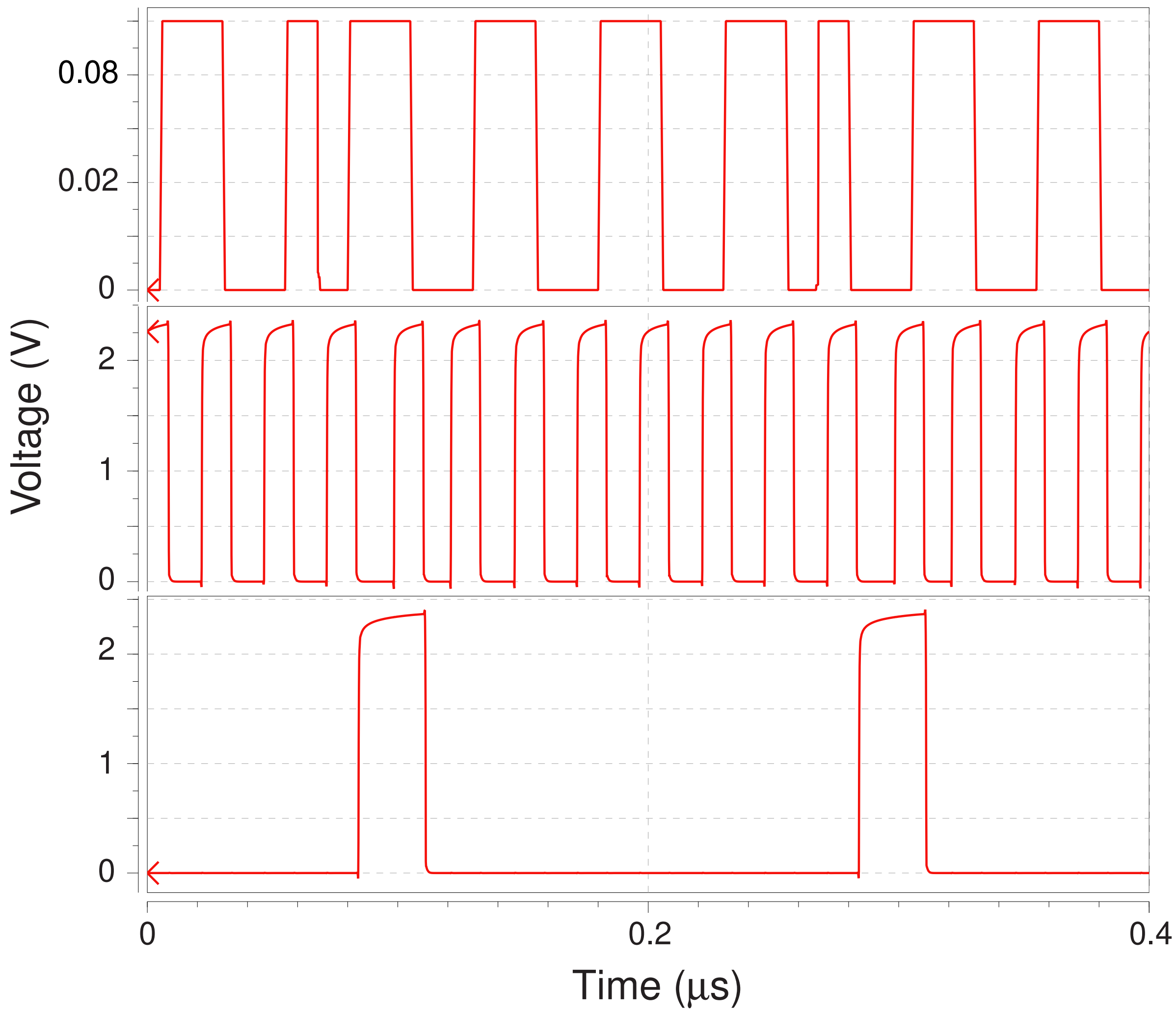
- simulation is based on netlist extractions from layout
- simulation includes following parasitics:
  - ◇ interconnect parasitics: metal 1 and 2 to substrate ($\sim$100 fF)
  - ◇ FET diode parasitics
  - ◇ stray capacitance of resistors

DORIC-P1 Simulation with Stray Capacitance



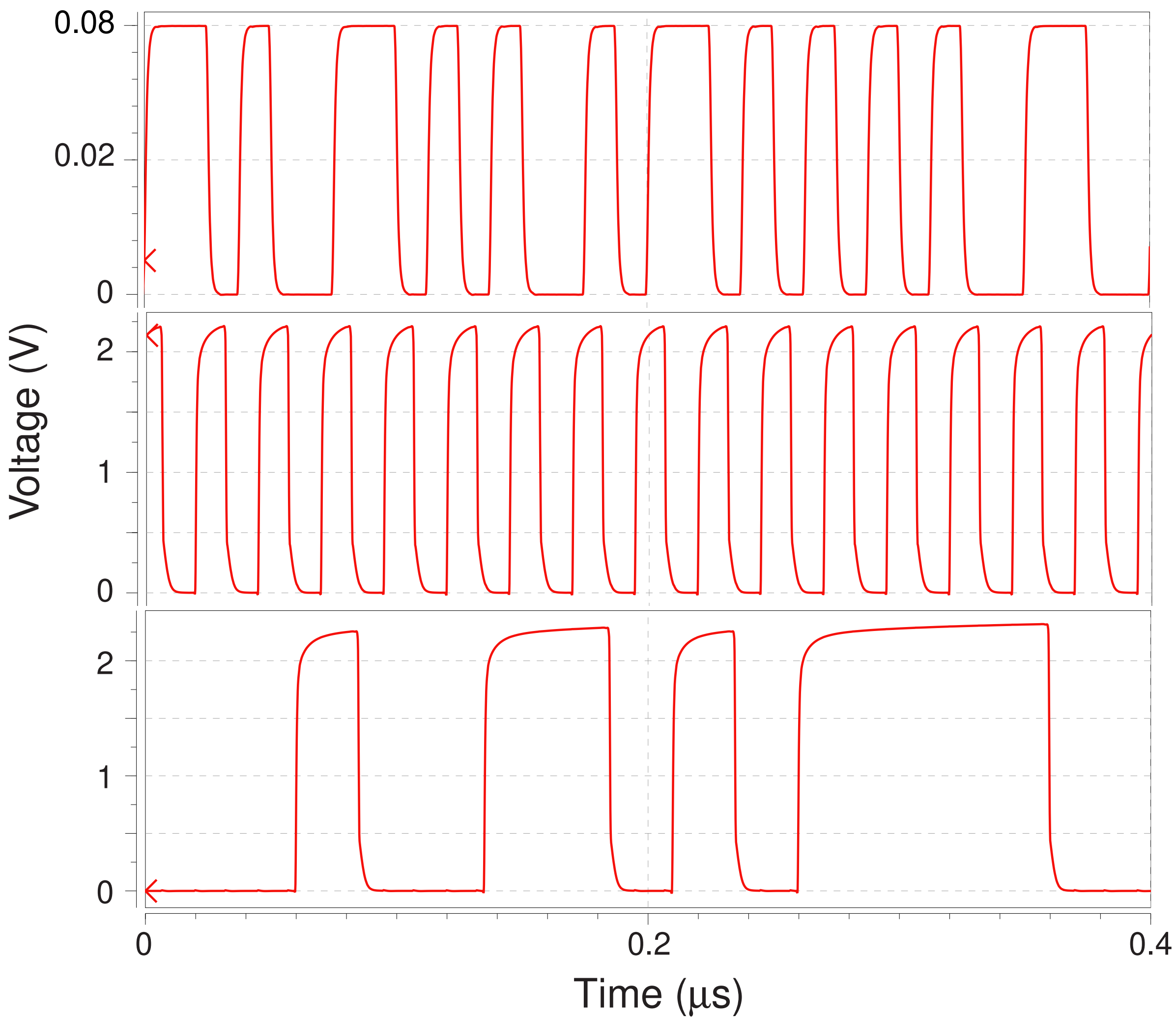
- DORIC-P1 cannot decode data

DORIC-P1 Simulation without Stray Capacitance



- DORIC-P1 without stray capacitance can decode clock and data simultaneously

DORIC-P2 Simulation with Stray Capacitance



- DORIC-P2 can decode clock and data simultaneously

Summary

- can now simulate failure of DORIC-P1 to decode clock and data simultaneously

→ give much needed confidence in simulation of DORIC-P2
which is predicted to work

→ simulation predicts DORIC-P2 will work with corner parameters