Preliminary Results on VDC-D2 and DORIC-D2

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Outline

- Introduction
- Results on VDC-D2
- Results on DORIC-D2
- Plans

Introduction

- VCSEL Driver Chip (VDC):
  - convert LVDS signal into single-ended signal appropriate to drive VCSEL
- Digital Opto-Receiver Integrated Circuit (DORIC):
  - decode clock and command signals from PIN diode

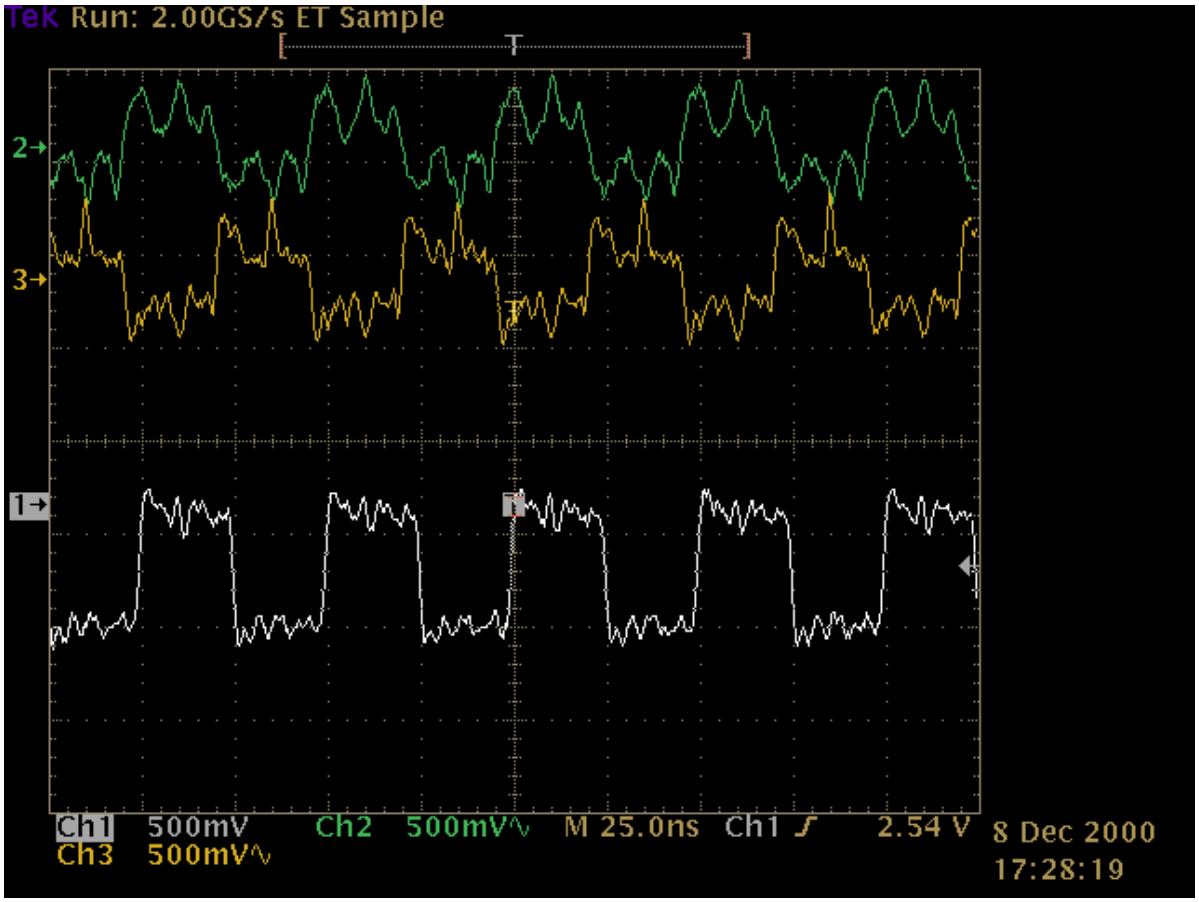
Opto-electronics Team

- Ohio State University:
  - ☆ K.K. Gan, Mark Johnson, Harris Kagan, Richard Kass, Chuck Rush, Michael Zoeller
- Siegen University:
  - ☆ Michael Kraemer, Joachim Hausmann, Martin Holder, Michal Ziolkowski

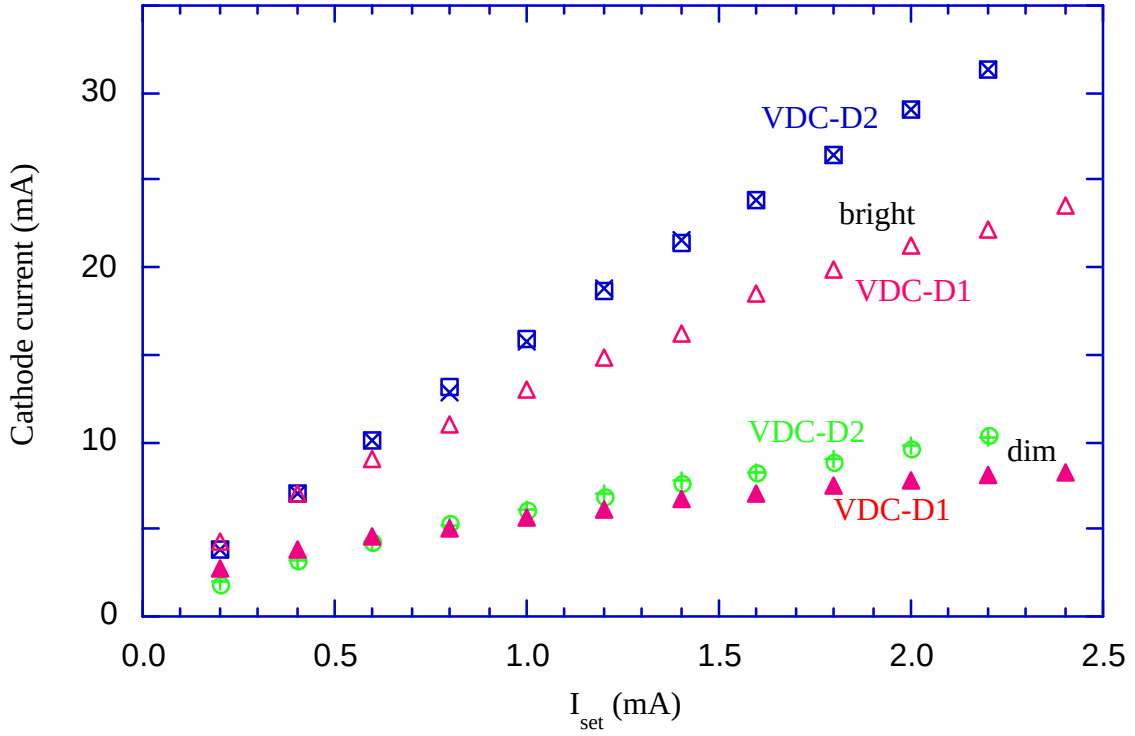
VDC

20 MHz
LVDS inputs

Output

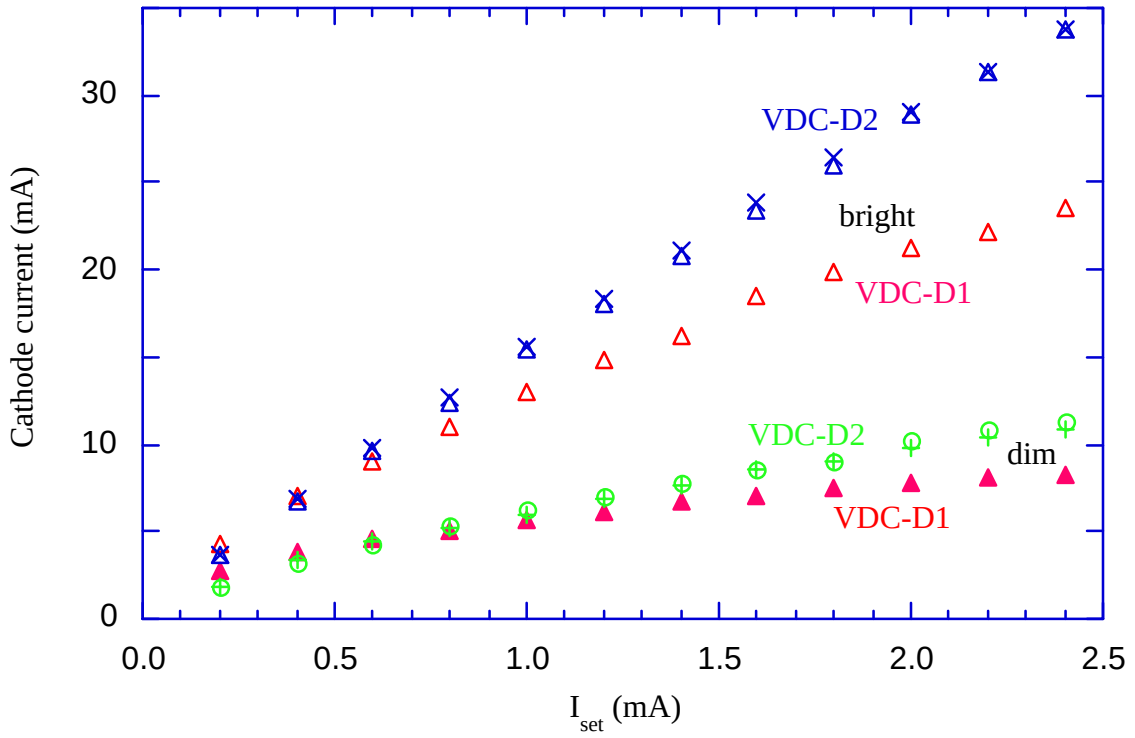


Bright/Dim Currents of VDC-D2 (Narrow)



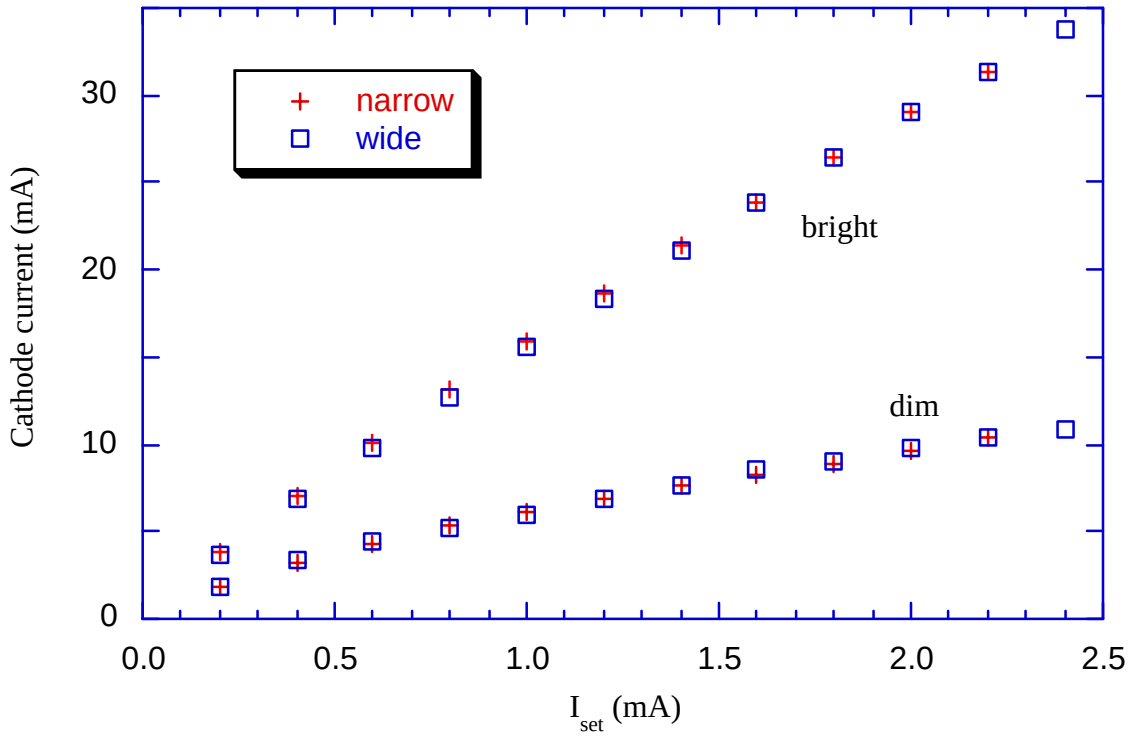
- two VDC-D2 have very similar gain but higher than VDC-D1

Bright/Dim Currents of VDC-D2 (Wide)



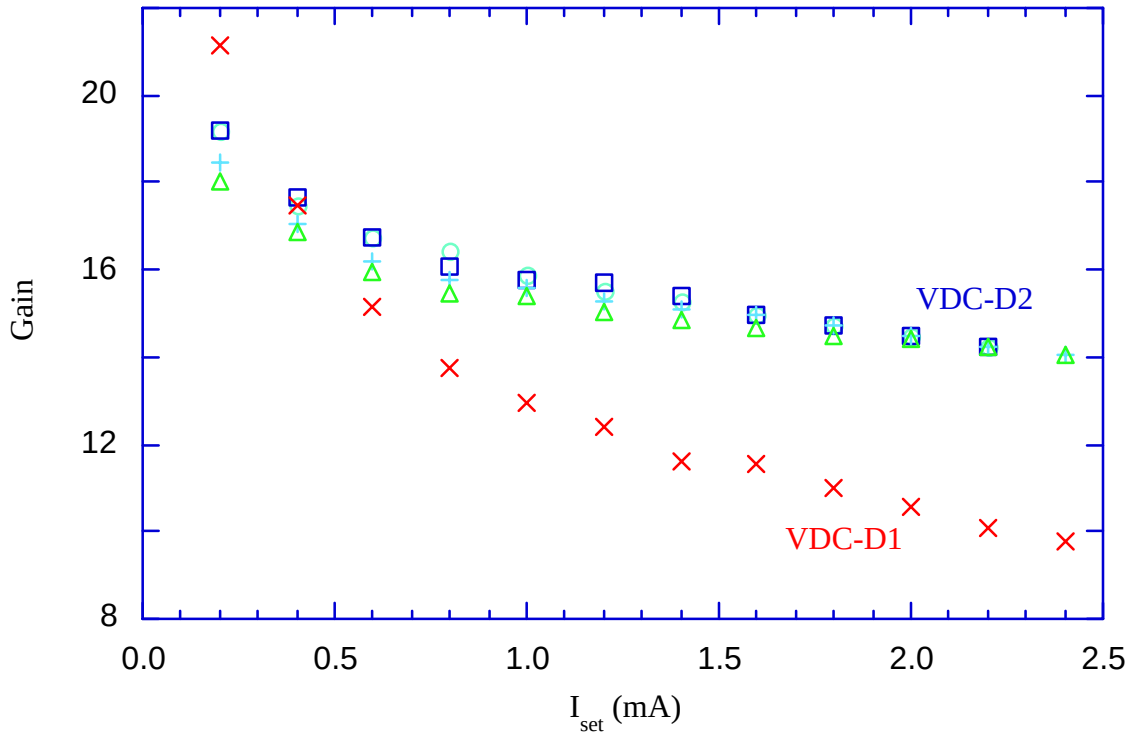
- two VDC-D2 have very similar gain but higher than VDC-D1

Narrow vs. Wide VDC-D2



- two VDC-D2 have very similar gain

Gain of VDC-D1 vs. VDC-D2



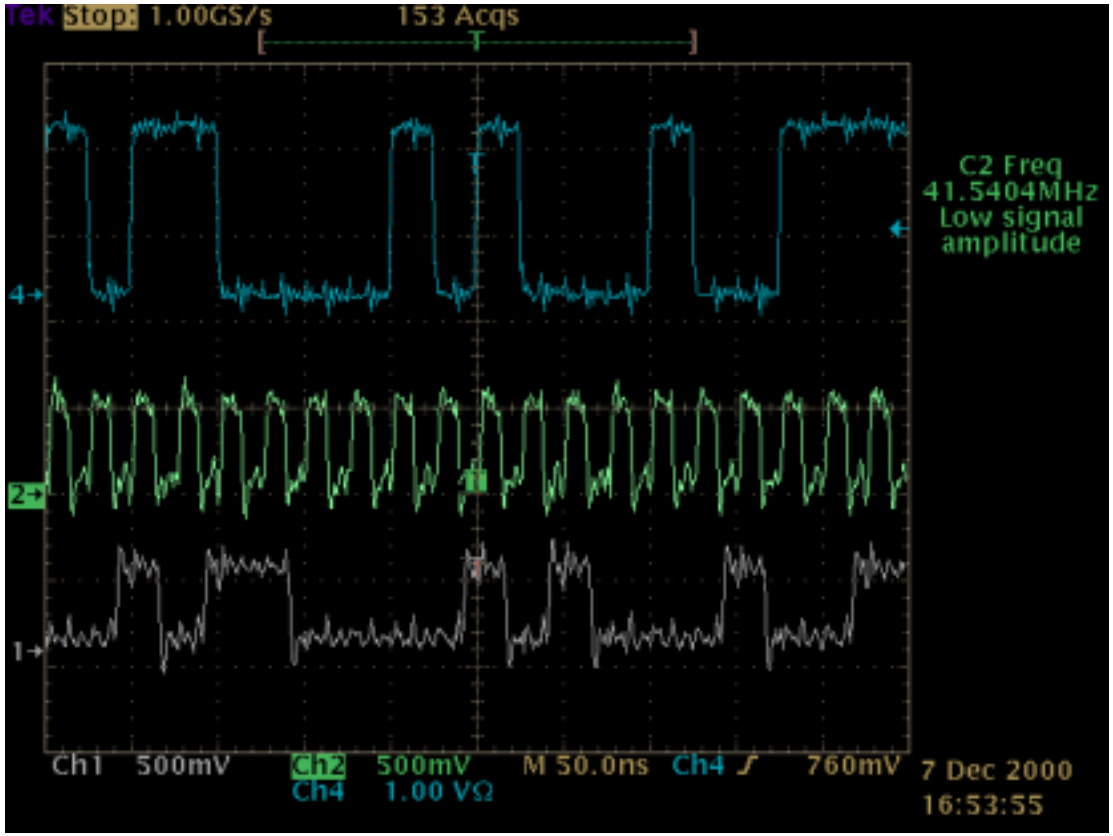
- All four VDC-D2 have similar gain but higher than VDC-D1

DORIC-D2 Data Decoding

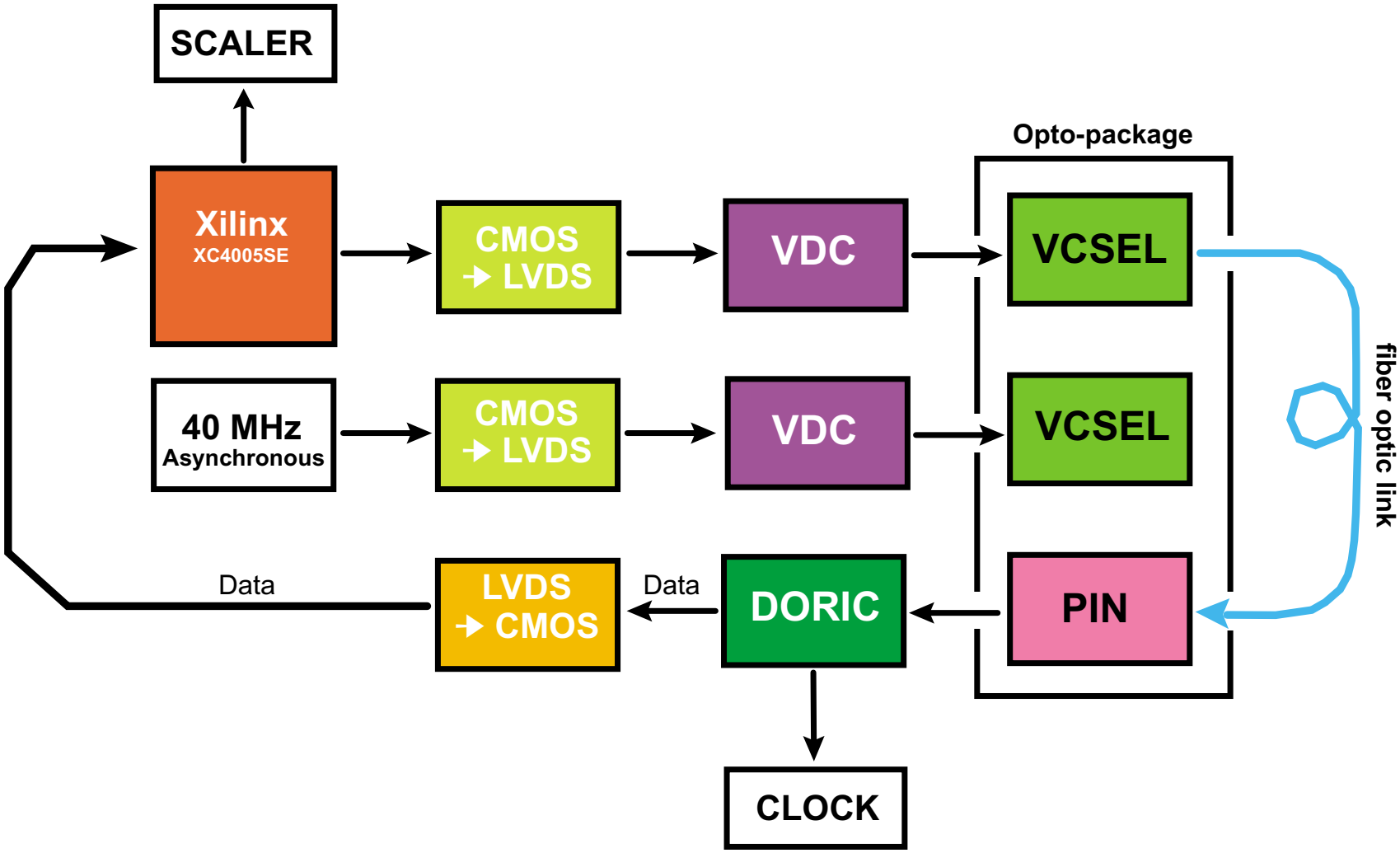
Input data

Decoded clock

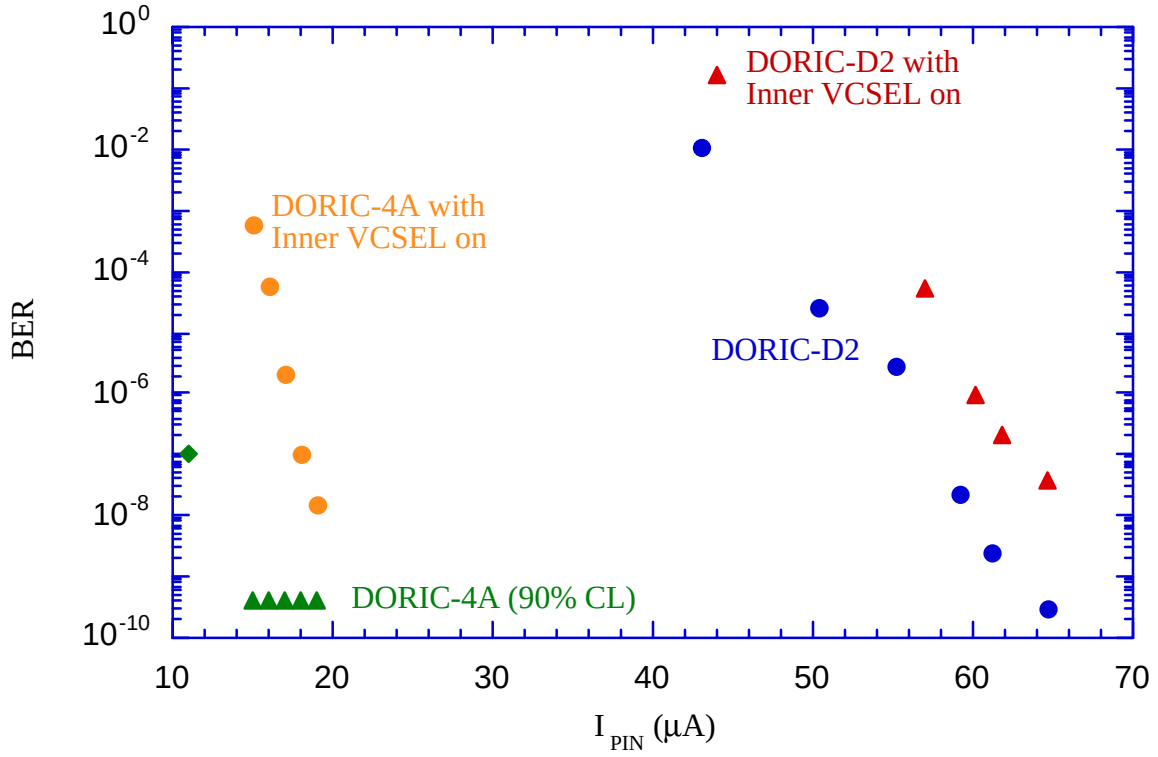
Decoded data



BER/Crosstalk Measurement with DORIC and VDC

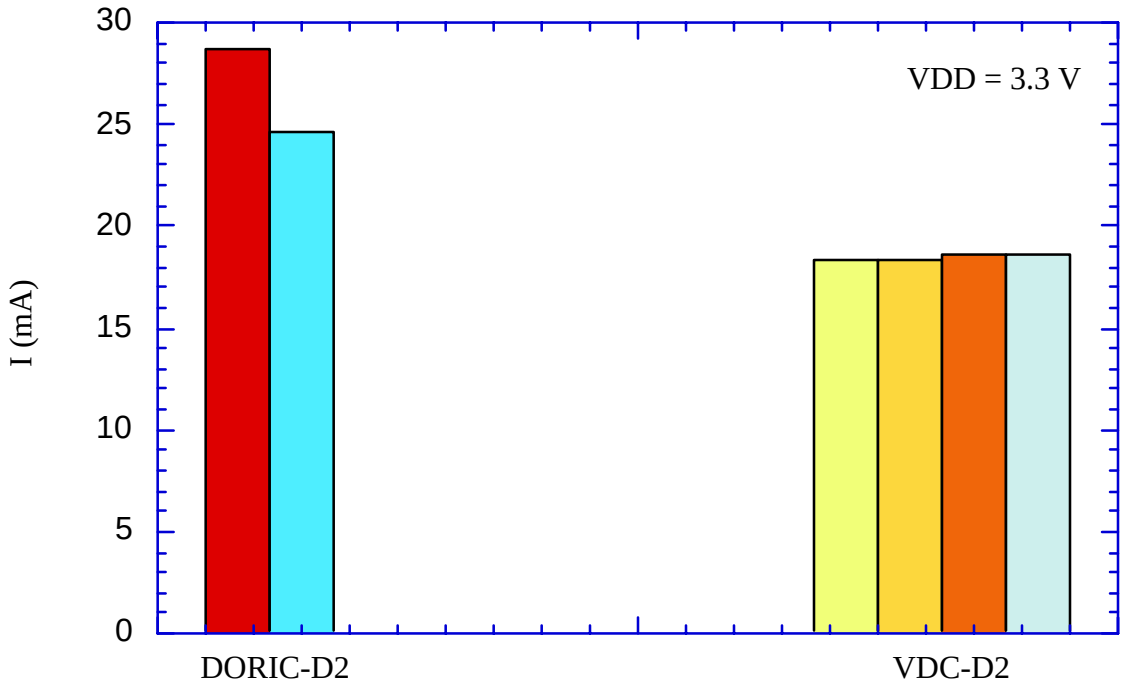


Binary Error Rate



- DORIC-D2 has significantly more cross talk than DORIC-4A?

Power Consumption



- a module with six channels consumes 0.9 W

Plans

- VDC-D2 and DORIC-D2 work!
  - ☆ comparison of test points with simulation in progress
- will emphasize irradiation of DORIC-D2 in April
  - ☆ a new rad-hard bias circuit without requiring a reset is needed for next DMILL submission