New Results on Opto-electronics

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Outline

- Introduction
- Result on Opto-Board/DORIC-D2
- Improvement in DORIC-I2/DORIC-D3
- Result on New Opto-Board
- Result on Opto-Board Irradiation
- Plans

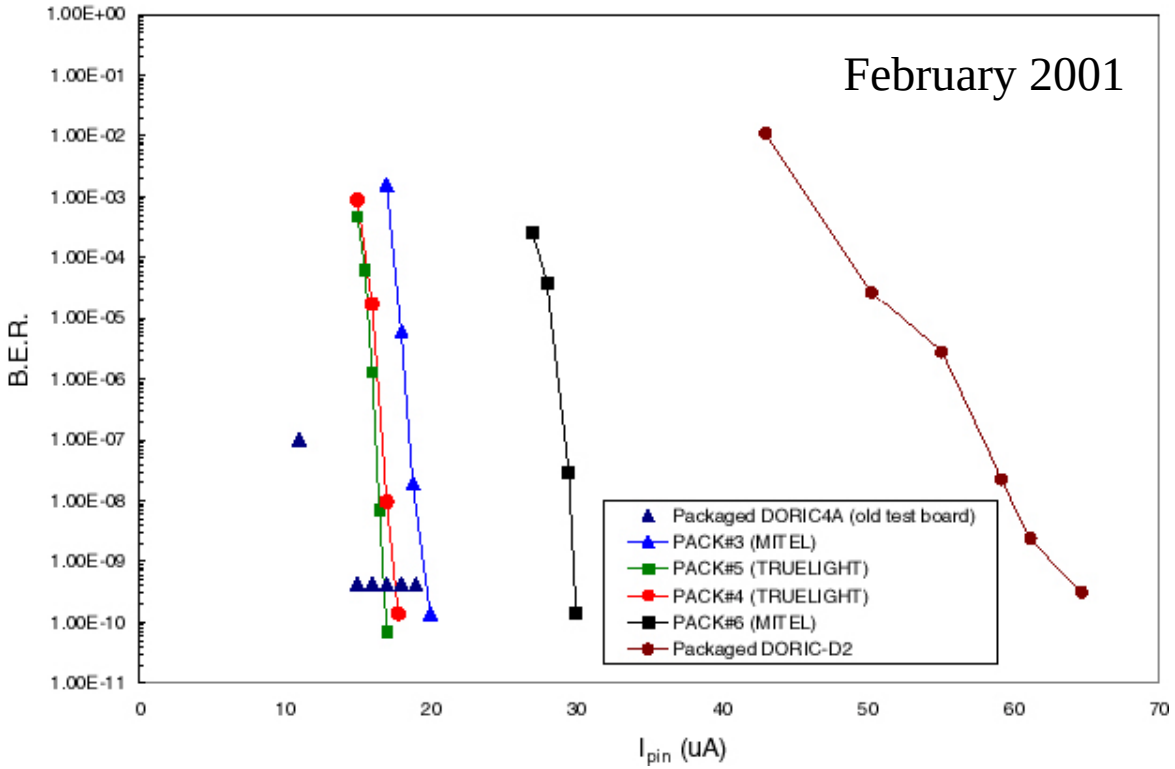
Introduction

- VCSEL Driver Chip (VDC):
  - convert LVDS signal into single-ended signal appropriate to drive VCSEL
- Digital Opto-Receiver Integrated Circuit (DORIC):
  - decode clock and command signals from PIN diode

Opto-electronics Team

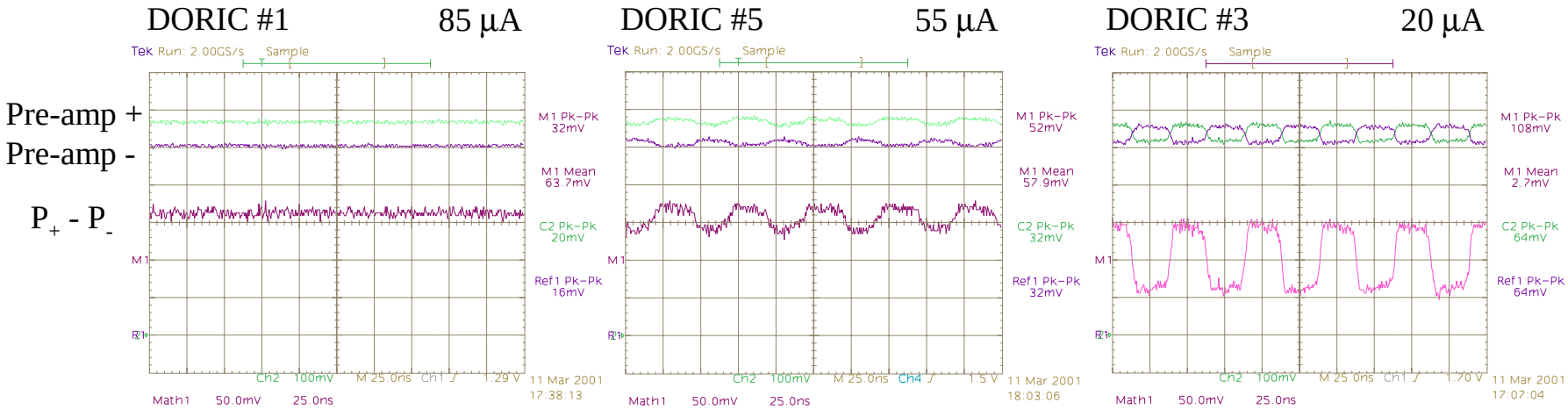
- Ohio State University:
  - Kregg Arms, K.K. Gan, Mark Johnson, Harris Kagan, Richard Kass, Chuck Rush, Michael Zoeller
- Siegen University:
  - Michael Kraemer, Joachim Hausmann, Martin Holder, Michal Ziolkowski

Bit Error Rate of DORIC



- some DORIC-D2 can run at low PIN current but some need to be ran at high current

Pre-amp Signal @ I_{PIN} = 20 μA vs BER Threshold



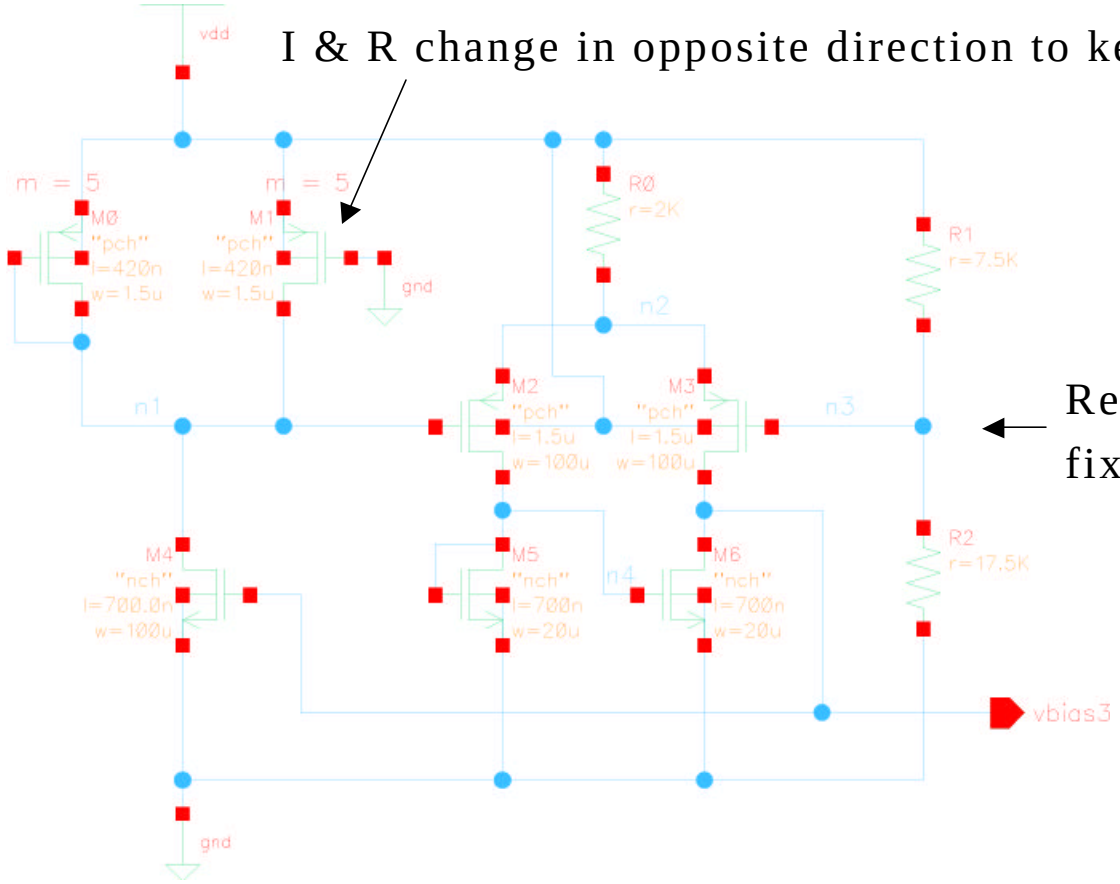
DORIC	#1	#5	#3
BER threshold (μA)	85	55	20
Pre-amp signal @ 20 μA	flat	poor	good

- high BER threshold of some DORICs is due to large pre-amp offset

Simulation of DORIC-I1 Response to Pre-amp Offset

- use dc-feedback with RC = 0.8 μs to cancel pre-amp offset
- simulated with parasitic capacitance extracted from layout
  - ☆ can handle ±7.5 mV offset
  - ☆ work with transistor parameters between -3.0σ and +2.0σ
  - ☆ pre-amp signal too small at +2.0σ to trigger edge-detector
    - ◆ decrease in bias current
    - ◆ decrease in effective resistance (5 K) of p-mos transistor
  - ⇨ new bias circuit in DORIC-I2 that keeps I and R change in opposite direction
  - ⇨ increase RC to 20 μs
  - ⇨ new feedback scheme

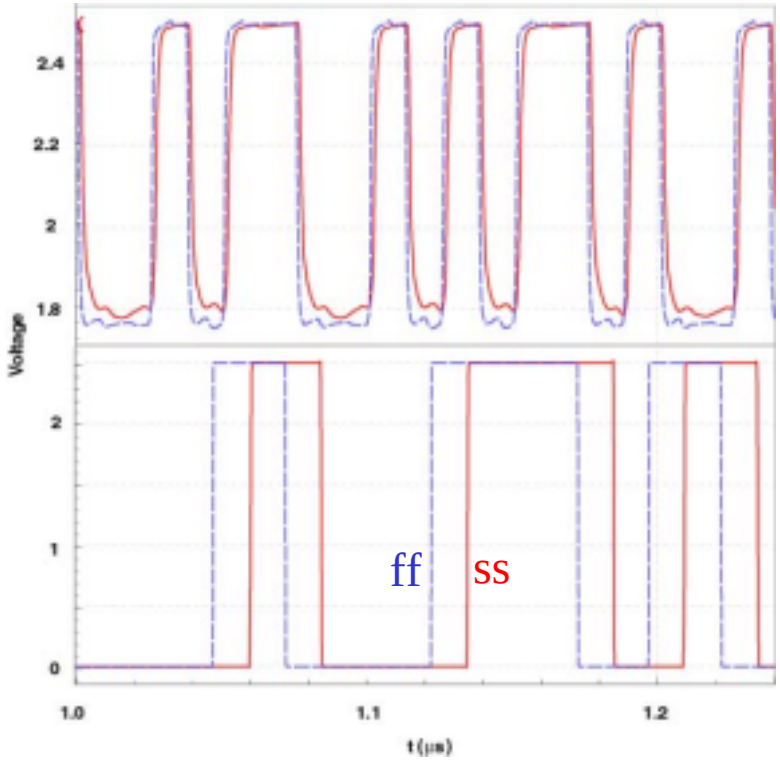
New Bias Circuit for DORIC-I2



Simulation of DORIC-I2

Pre-amp output

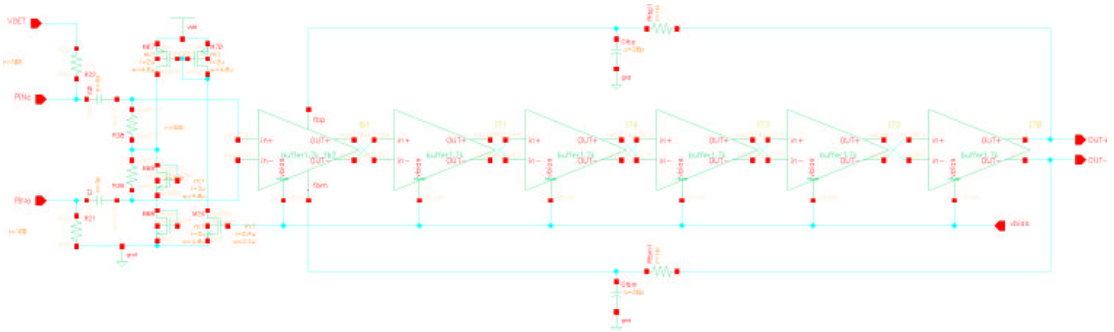
Decoded data



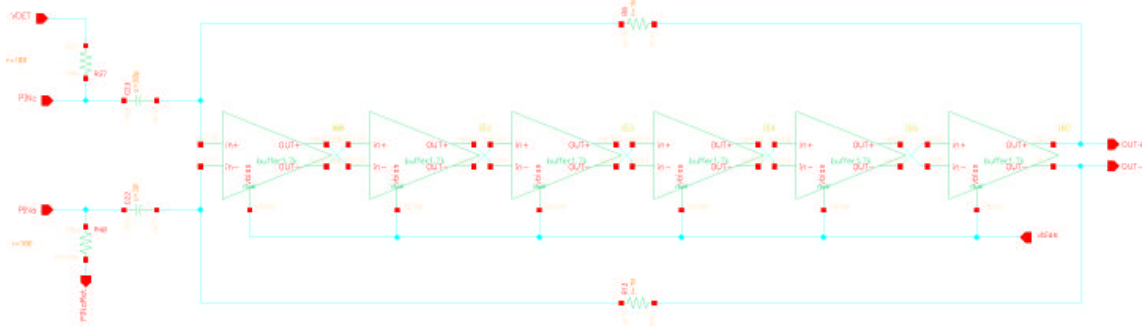
- DORIC-I2 can decode data with 50 mV pre-amp offset for both slow-slow and fast-fast transistor parameters

Improvement in Pre-amp Feedback

old



new

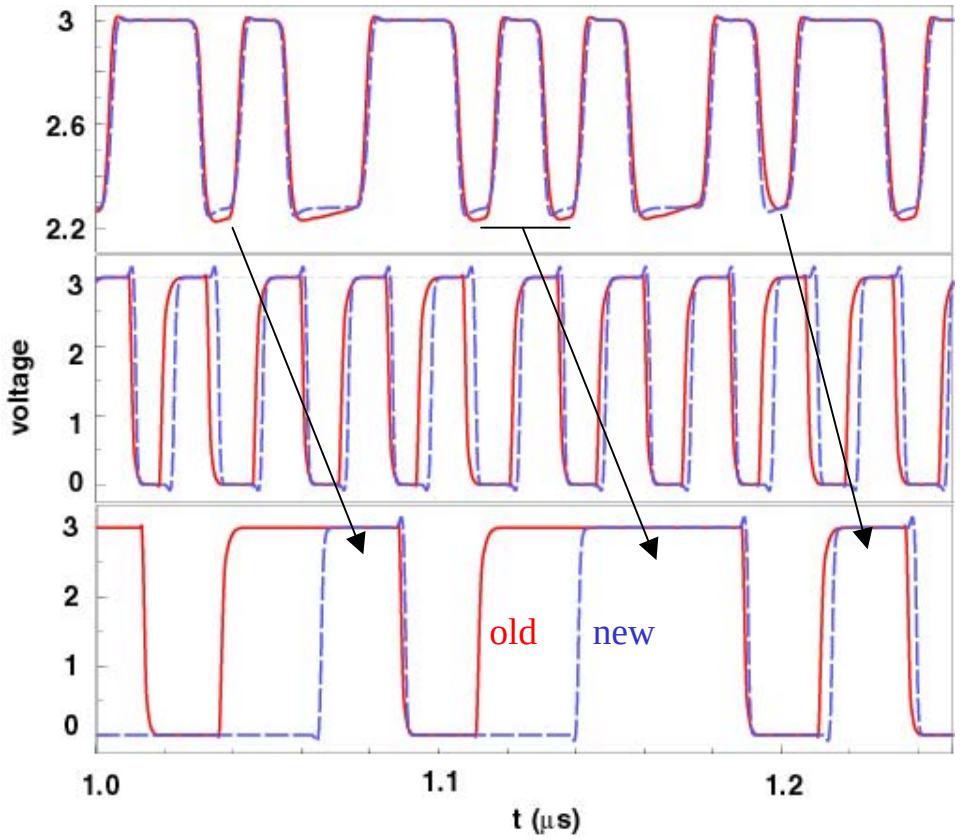


Simulation of DORIC-D3 with Slow-Slow Transistor Parameter

Pre-amp output

Recovered clock

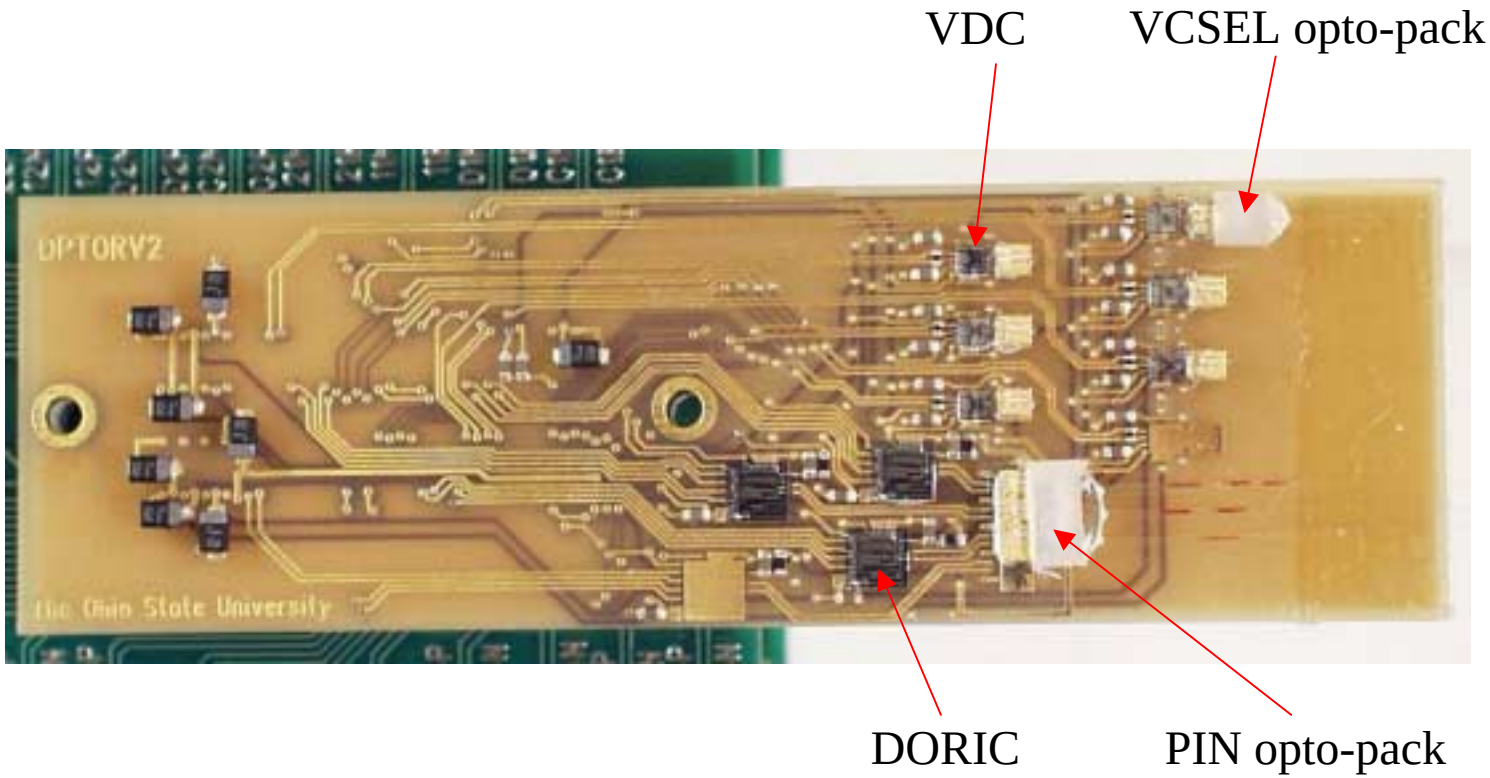
Recovered data



new design (blue)
has better duty cycle

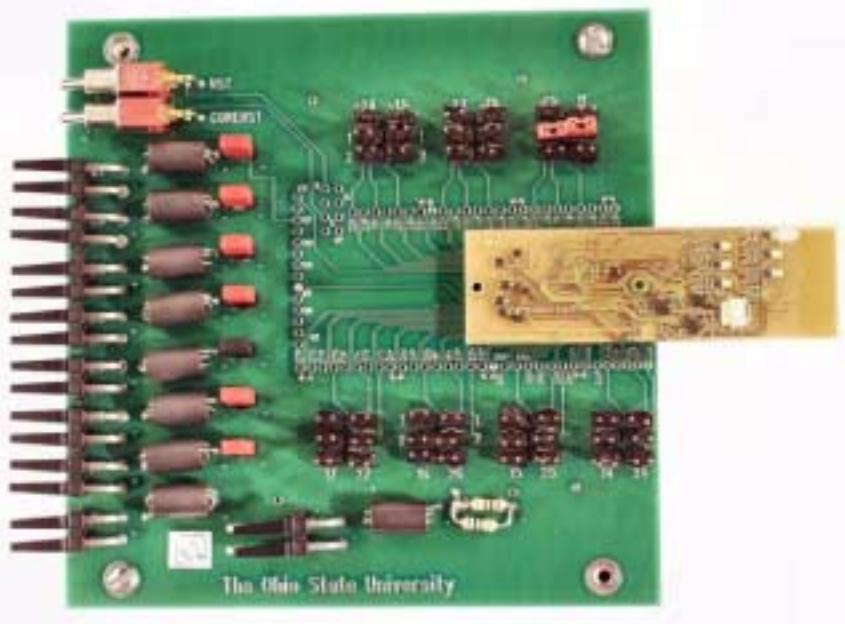
- DORIC-D3 can decode data with 50 mV pre-amp offset for all corner transistor parameters

New Opto-board with 7 Links



- new 80-pin connector is much sturdier

New Opto-board Tester

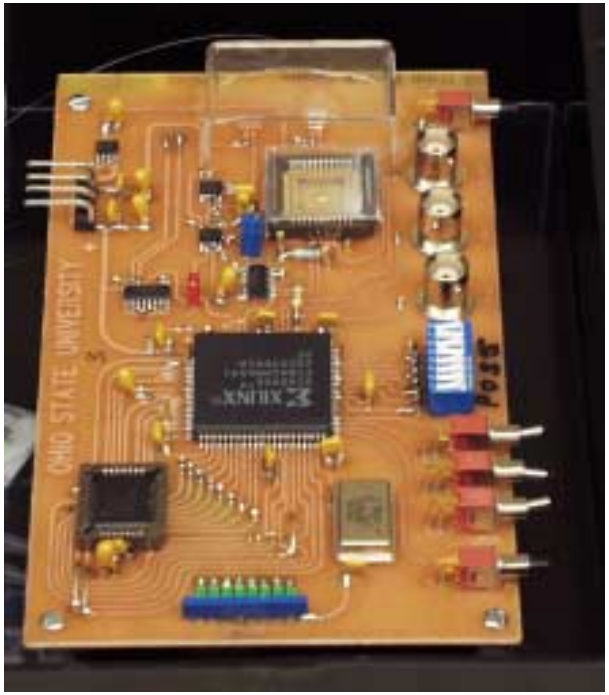


Bi-phase marked signal

fibers

Decoded data

Bit error test board



April Irradiation of Opto-Electronics

- use 24 GeV proton test beam at T7
- cold box: purely electrical testing of VDC-D2 and DORIC-D2
- shuttle system: testing of 4 optical links on opto-board

- test beam team:
  Kregg Arms, K.K. Gan, Ingrid Gregor, Harris Kagan,
  Richard Kass, Michael Kraemer, Clemens Ringpfeil,
  Petr Sicho, Michal Ziolkowski

Test Boards for Irradiation in Cold Box

3 VDC and 5 DORIC boards in test beam

5 m cables

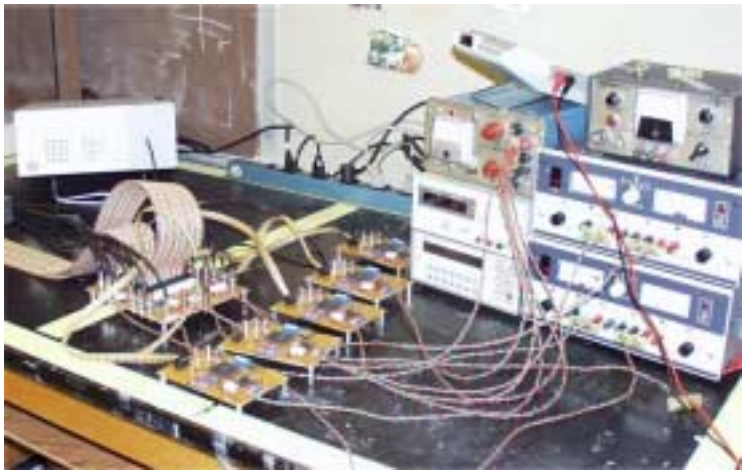
Repeater board for signal reshaping and routing

Bi-phase marked signal
40 MHz LVDS signal

20 m cables

Decoded LVDS data + clock
40 MHz signal

Bit error test board in control room



Test Boards for Irradiation in Shuttle

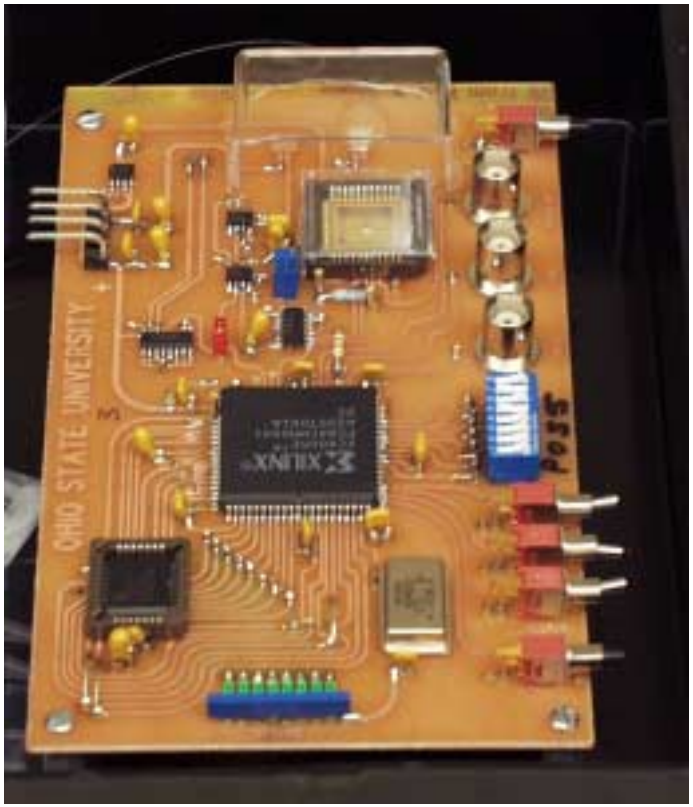
Bit error test board in control room
(4 boards)

Opto-board with 4 opto-links

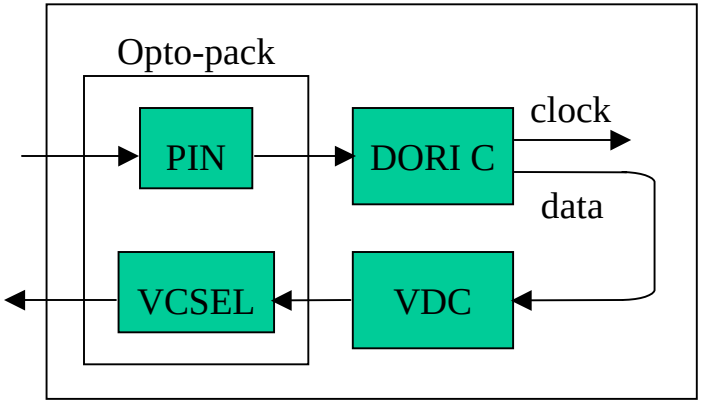
Bi-phase marked optical signal

15 m fibers/wires

Decoded data
(3 optical + 1 electrical)



Opto-link



Chronology of Opto-board Irradiation

- opto-board survived laborious packing/shipping/unpacking/dressing
  - ⇨ will replace 7-fiber (2.6 mm) + 2-wire bundle by custom cables with 14 fibers (250 μm) + 20 wires + spares
- need to run with reset low (higher gain) after installation
  - ⇨ noise in VVDC, VISET, or VPIN due to extra 20 m wires?
- after ~ 1 Mrad: two links needed to be ran at high PIN currents!
- after a few Mrad: Taiwan opto-pack produced bit error
  - ⇨ package damaged in extensive temperature cycling?

Chronology of Opto-board Irradiation Continued

- after ~ 5 Mrad: parked shuttle and annealed VCSEL
  - ⇨ more light from Truelight VCSEL and Mitel VCSEL
  - ⇨ no improvement in Truelight VCSEL of Taiwan opto-pack
  - ⇨ all links had bit errors but stopped when shuttle back in beam
  - ⇨ loose connector due to extensive handling?
- after ~ 8 Mrad: 3 good links produced bit errors
  - ⇨ light too low for receiver boards in control room
    - ☆ will design receiver board with more dynamic range
  - ⇨ unclear why electrical return produced bit errors
- At ~ 29 Mrad: irradiation stopped

Irradiation Post-Mortem

- all opto-links have bit errors
  - ⇨ isolated probles by implementing electrical returns
  - DORIC #2:
    - ☆ dosage: few Mrad
    - ☆ pre-irrad: 56 μA w/ reset high
    - ☆ post-irrad: 20 μA w/ reset high
      28 μA w/ reset low
  - DORIC #4:
    - ☆ dosage: 15 Mrad
    - ☆ pre-irrad: 12 μA w/ reset high
    - ☆ post-irrad: 16 μA w/ reset high @ 3.53 V
      31 μA w/ reset low @ 3.26 V
      >198 μA w/ reset low @ 3.20 V

Irradiation Post-Mortem Continued

- DORIC #5:
  - ☆ dosage: 0.6 Mrad
  - ☆ pre-irrad: 61 μA w/ reset high
  - ☆ post-irrad: >198 μA w/ only data returned
- DORIC #6:
  - ☆ dosage: 29 Mrad
  - ☆ pre-irrad: 30 μA w/ reset high
  - ☆ post-irrad: no PIN current ⇨ dead
- To do:
  - ☆ study VDC
  - ☆ remove caps to replace fibers

⇨ some DORIC on opto-board were damaged by irradiation

Summary/Plan

- high pin current threshold of some DORICs
  is due to pre-amp offset
  - ⇨ implemented dc feedback in DORIC-I1
  - ⇨ further improvements in dc feedback in DORIC-I2/D3
- some DORIC-D2 on opto-board were damaged by irradiation