New Results on Opto-electronics

K.K. Gan

The Ohio State University

October 9, 2001

Outline

- Introduction
- Result on VDC-I1/DORIC-I1
- Improvements in DORIC-I2
- Result on Opto-Board/D2 Irradiation
- Result on Opto-Board/I1 Irradiation
- Plans

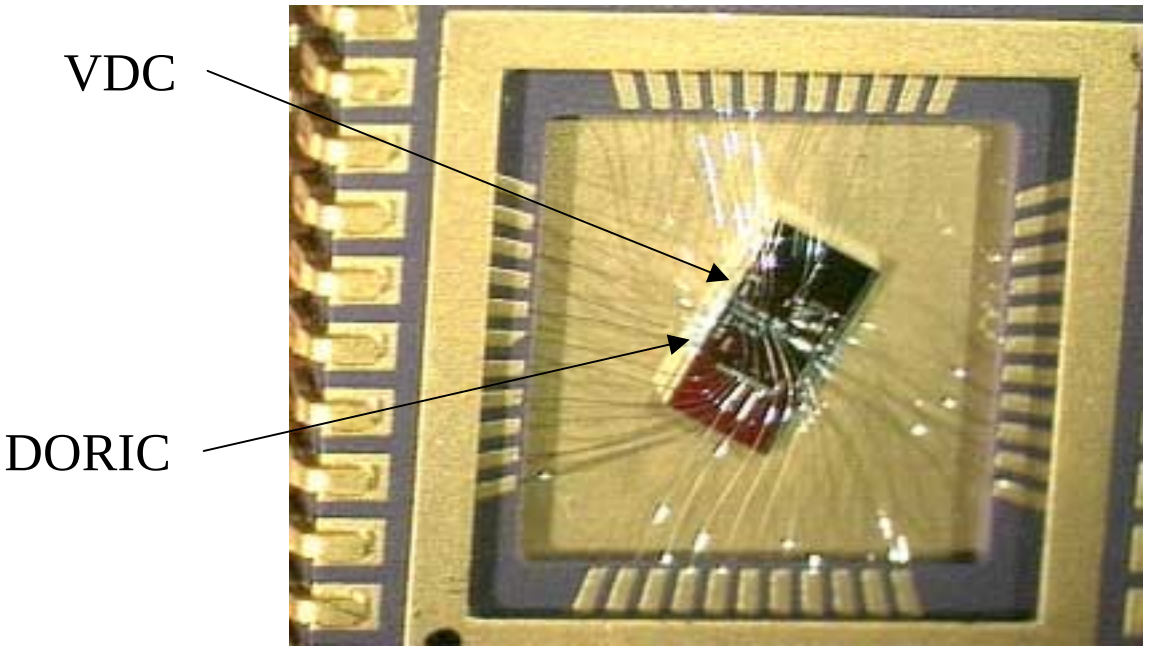
Introduction

- VCSEL Driver Chip (VDC):
  - convert LVDS signal into single-ended signal appropriate to drive VCSEL
- Digital Opto-Receiver Integrated Circuit (DORIC):
  - decode clock and command signals from PIN diode

Opto-electronics Team

- The Ohio State University:
  - Kregg Arms, K.K. Gan, Mark Johnson, Harris Kagan, Richard Kass, Chuck Rush, Michael Zoeller
- Siegen University:
  - Michael Kraemer, Joachim Hausmann, Martin Holder, Michal Ziolkowski

VDC-I1/DORIC-I1

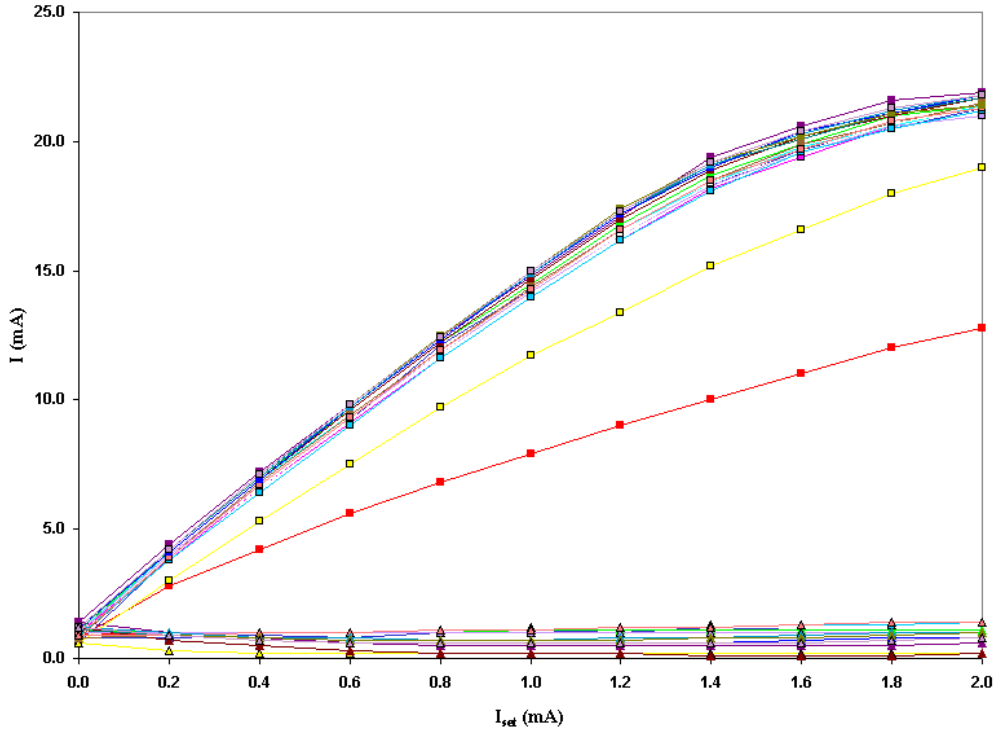


- VDC and DORIC are on same die
  - VDC operation introduces noise in DORIC

VDC-I1

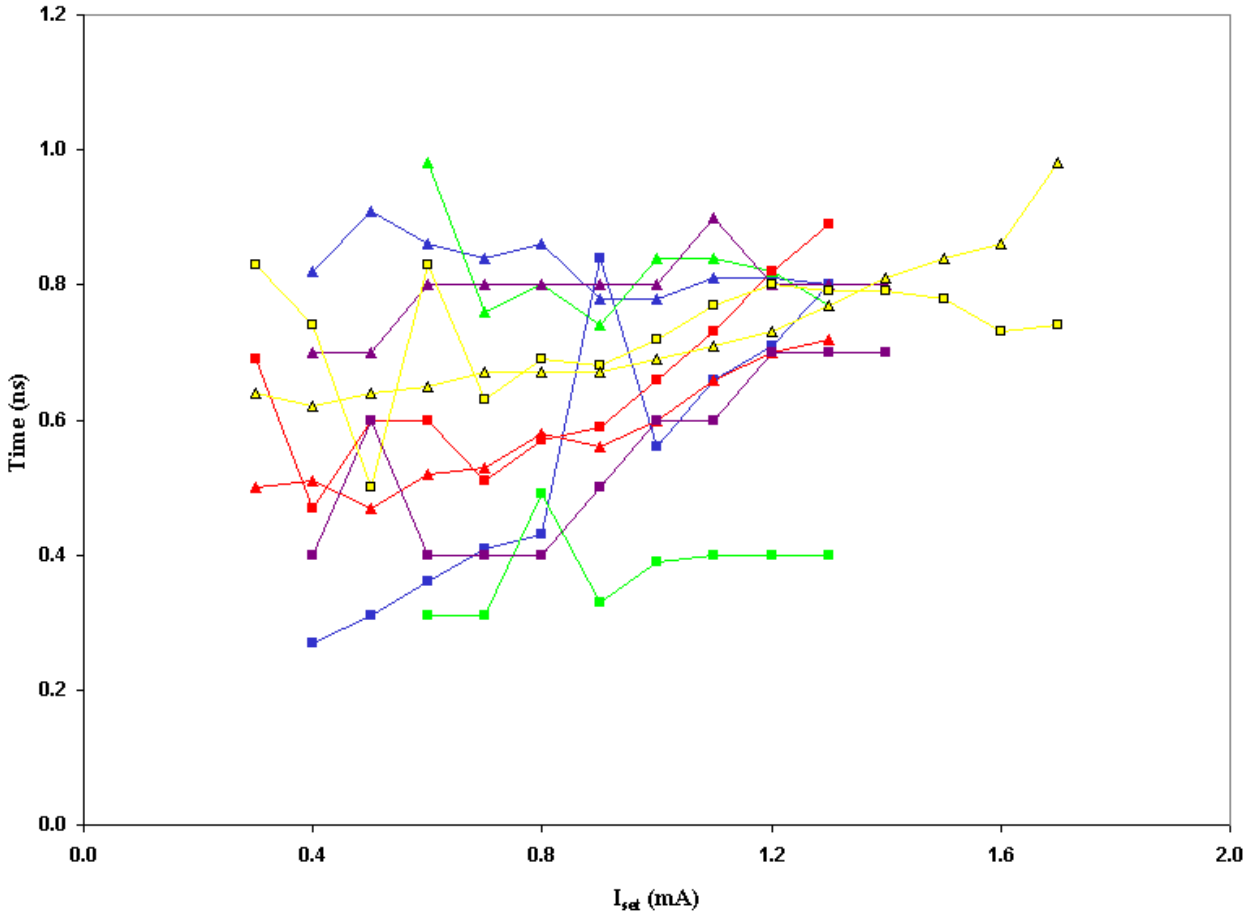
- 1st IBM version of VDC:
  - two designs were submitted
    - design 1: IBM adaptation of VDC-D2
    - design 2: new circuit that decouples adjustment of bright and dim currents

VCSEL Currents vs I_{set}



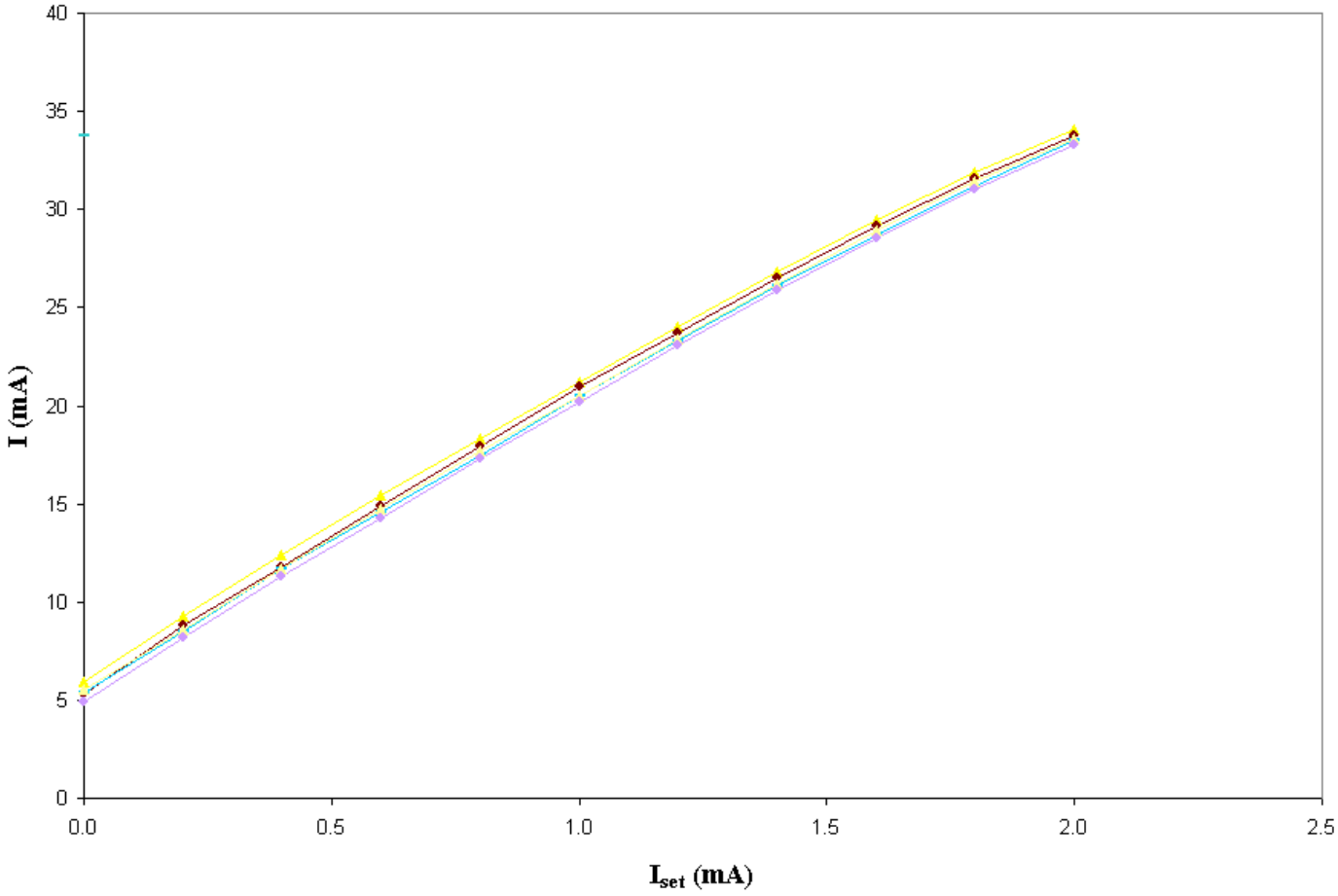
- 10 Ω in series with VCSEL for current measurement partially responsible for turn over of bright current at large I_{set}
- dependence of bright/dim currents on I_{set} is as expected
- 16/18 VDC works with 2.5V!

VDC Rise/Fall time vs I_{set}



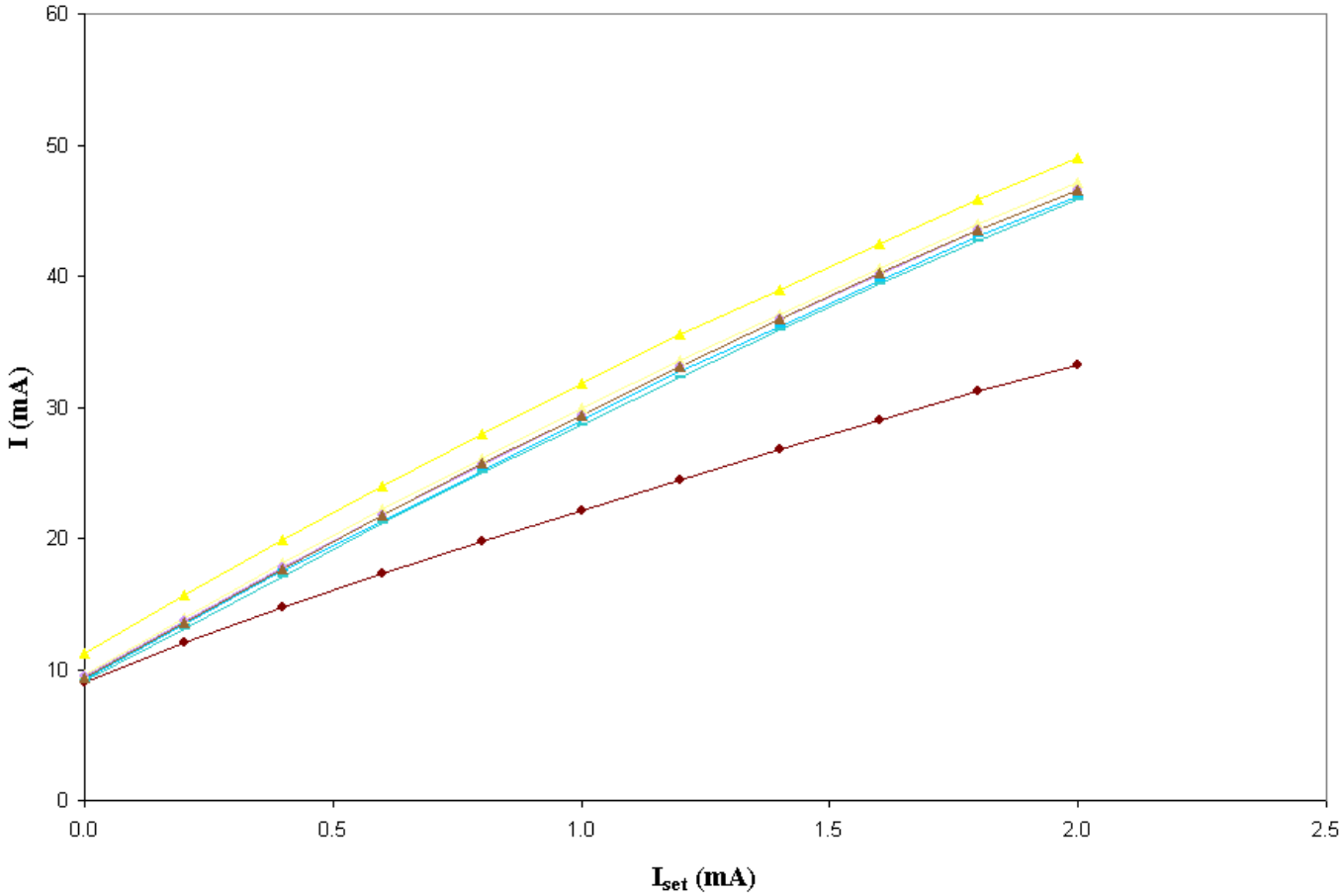
- rise and fall time are within spec. (< 1 ns)

Current Consumption of DMILL Version of VDC-I1



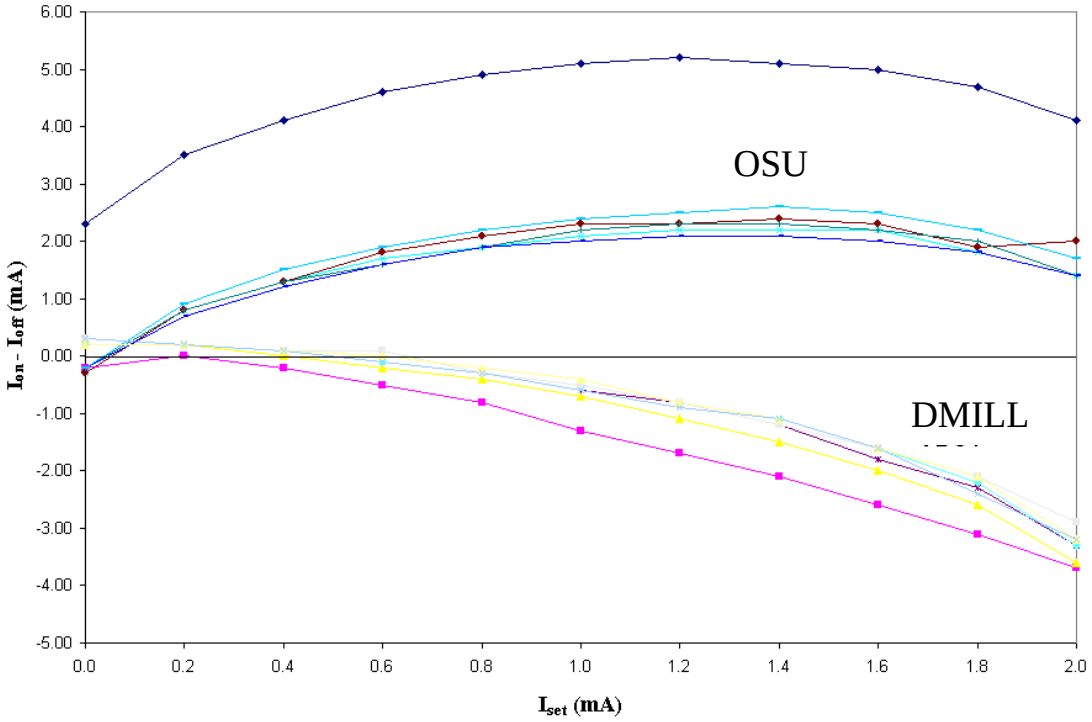
- VDC consumes ~ 15 mA for 10 mA VCSEL current

Current Consumption of OSU Version of VDC-I1



- VDC consumes ~ 22 mA for 10 mA VCSEL current
- plan to reduce current by a few mA in future design

Bright and Dim Current Consumption vs I_{set}

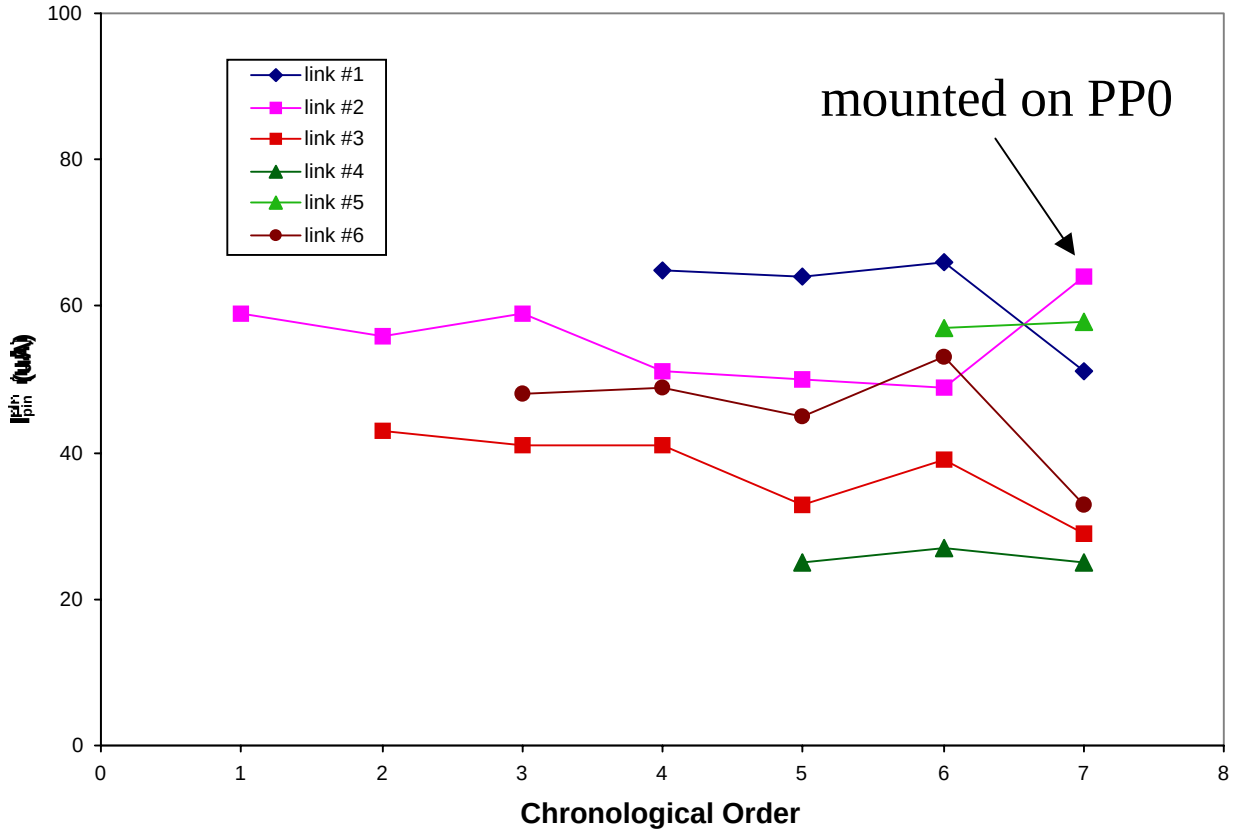


- VDC and DORIC use same power supply
  - ⇨ need no ripple in current consumption
- bright and dim current consumption are different
  - ⇨ ripple in current consumption
  - ⇨ new circuit in VDC-I2 with more balanced current consumption

DORIC-I1

- delay control circuit oscillates
  - ⇨ need 1.2 nF bypass
  - ⇨ DORIC-I1 works!
- PIN current threshold for no bit errors
  can be adjusted via pre-amp dc feedback circuit
  - ⇨ feedback circuit works!

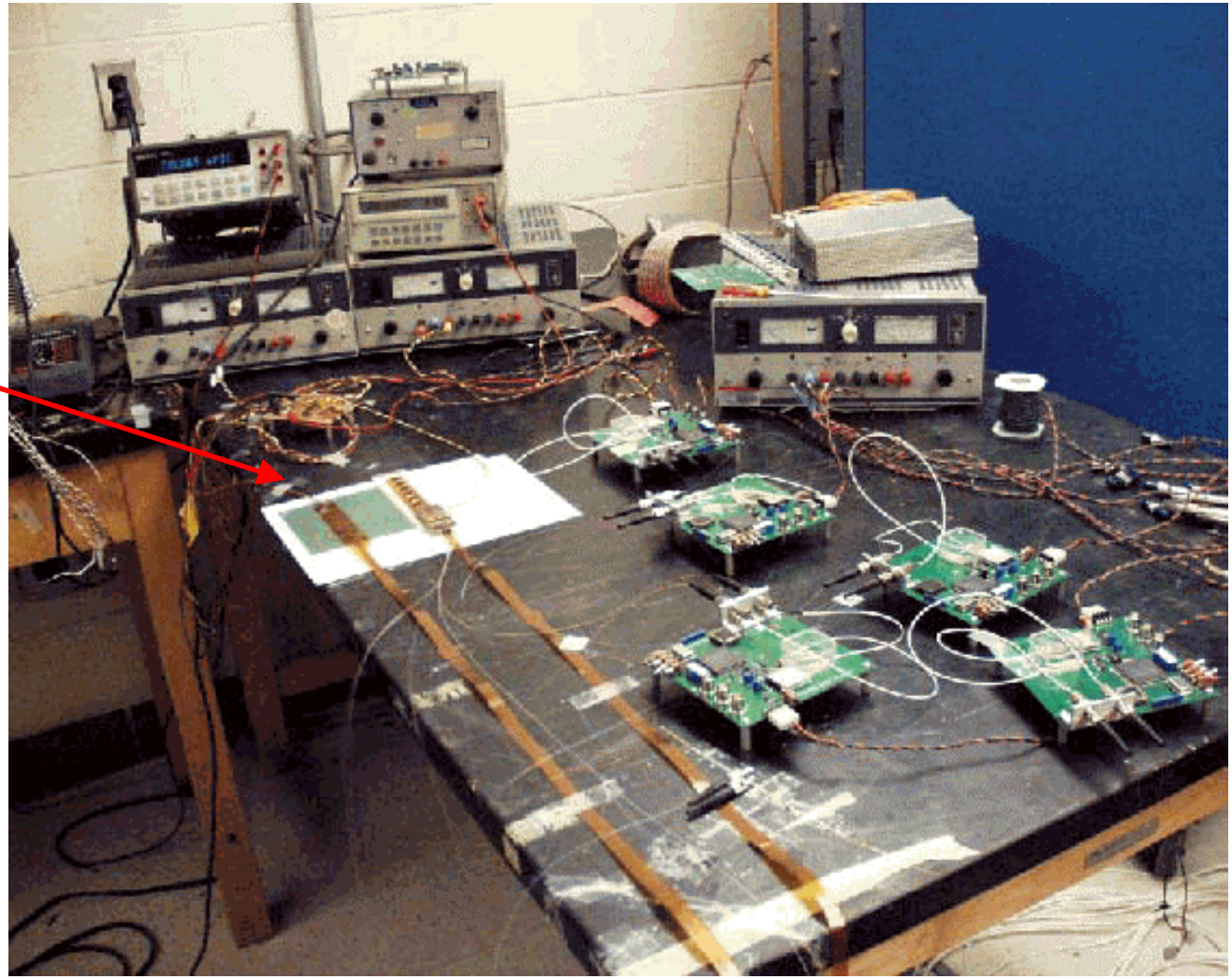
PIN Current Threshold of DORIC-I2



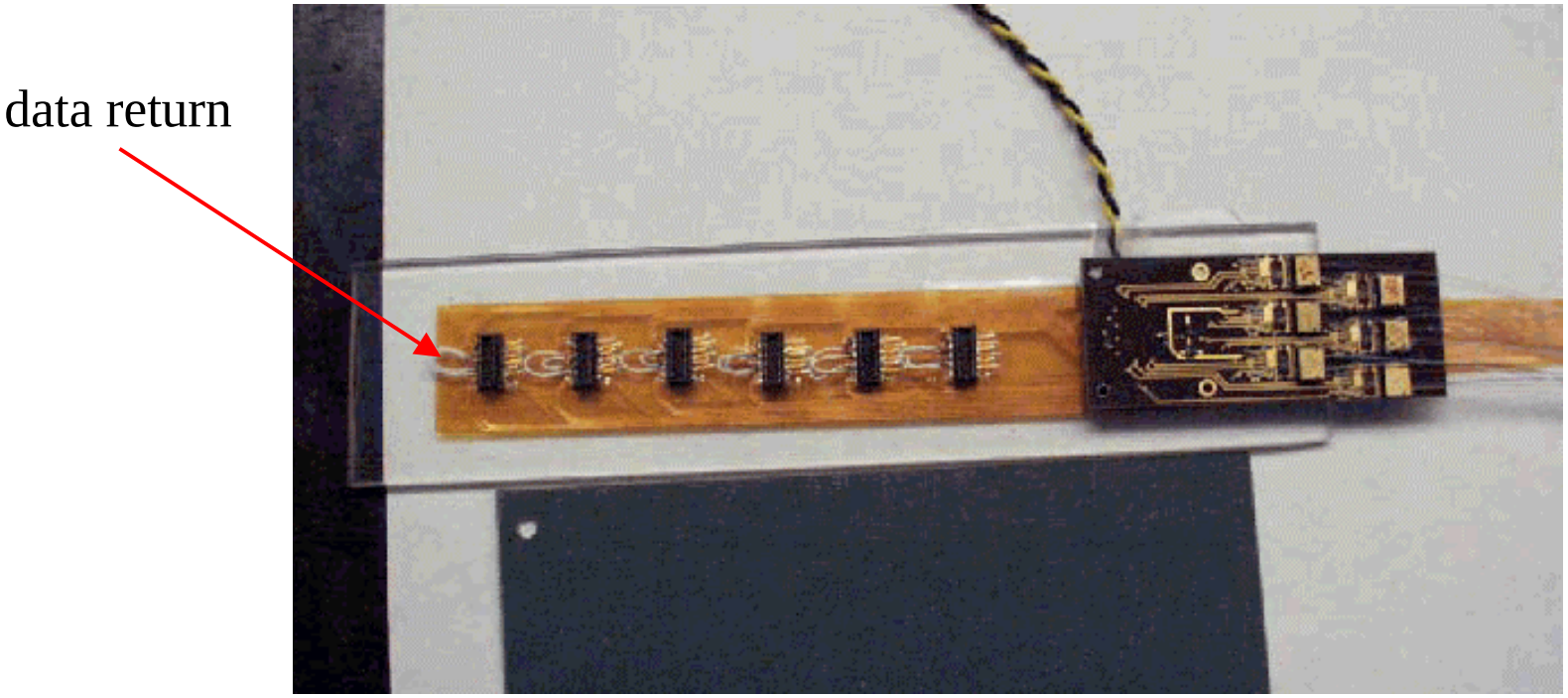
- no degradation of PIN current threshold for no bit errors as more links are added on opto-board and PP0

Setup with PP0

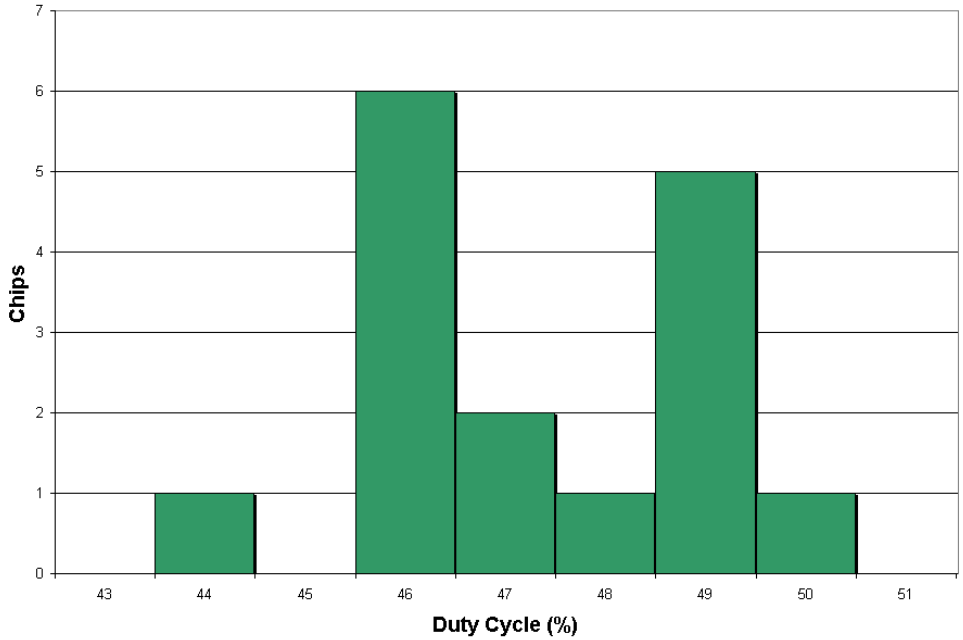
ISET + VPIN



Setup with PP0



Duty Cycle of Decoded Clock of DORIC-I1 for Random Input Data

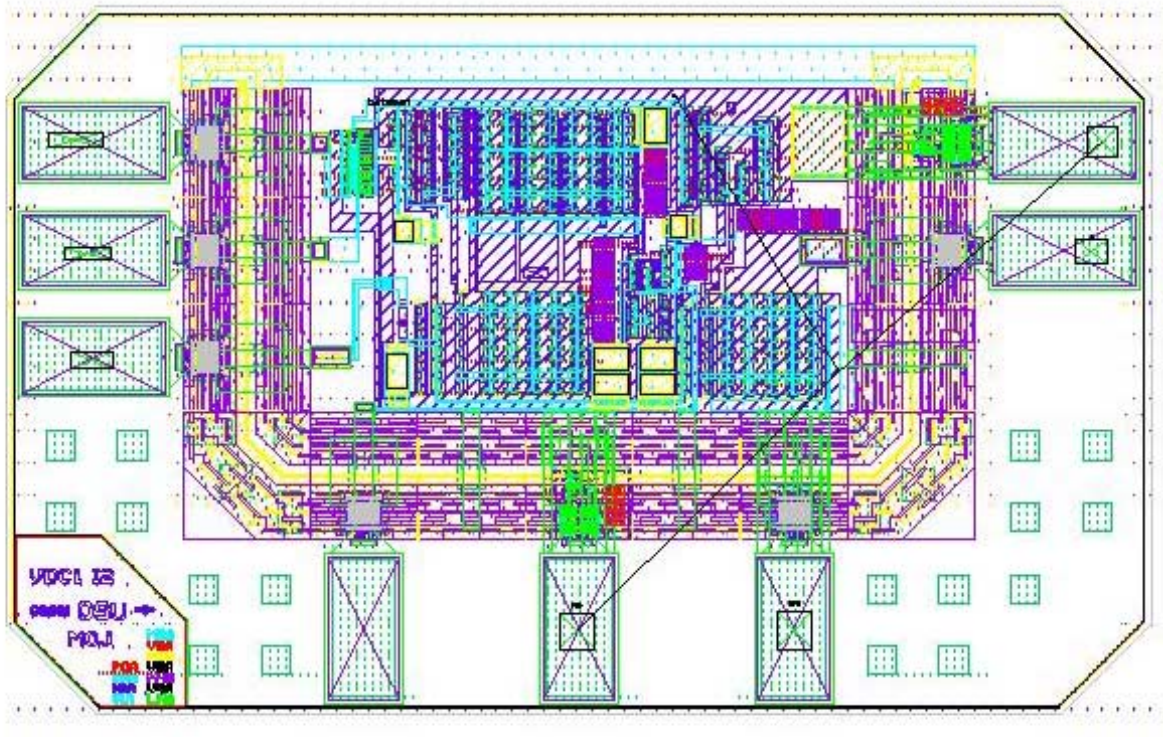


- 15 out of 16 DORIC-I1 within spec. (< 4%)
- ☆ expect better duty cycle with DORIC-I2 with longer dc feedback time constant

Improvements in VDC-I2

- keep OSU design that decouples adjustment of bright and dim currents
  - ☆ new circuit that equalizes bright and dim current consumption
  - ☆ new LBL pads
- submitted two design: single and four-channel VDC

Single-Channel VDC-I2



Four-channel VDC-I2

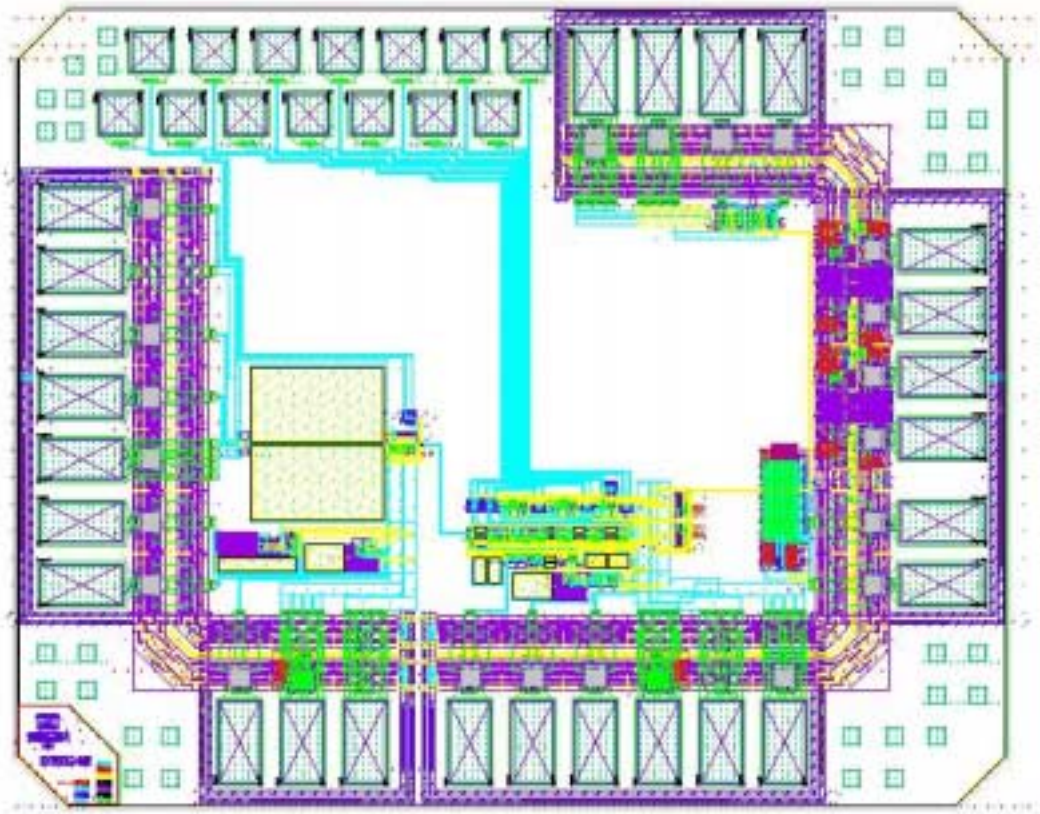
Improvements in DORIC-I2

- longer dc feedback time constant: 1.2 ⇨ 40 μs
  - ☆ cancel larger pre-amp offset
  - ☆ less clock jitter
- use OSU bias circuit which simulation predicts to work with all corner transistor parameters
- less amplification stages (gain) to reduce flicker and white noises:
  - ☆ total noise: 74 ⇨ 25 mV
- improve delay control circuit:
  - ☆ large integrating capacitor: 0.2 ⇨1.3 nF
  - ☆ 50% less start-up current for longer delay to ensure decoded clock has 50% duty cycle

Improvements in DORIC-I2 (Continued)

- improve grounding scheme:
  - ☆ analog and digital circuits enclosed in guard rings
  - ☆ source and bulk of analog grounds are tied together locally
  - ☆ source and bulk of digital grounds are individually accessible via pads
- well separated input (analog) and output (digital) circuits to avoid coupling of input and output signals
- use LBL pads

DORIC-I2



Packaged DORIC-D2 Irradiation Post-Mortem

DORIC	#4	#5
Dosage (Mrad)	37	34
Pre-irrad (μA)	71	76
Post-irrad (μA)	83	79
Anneal (μA)	63	82

- DORIC #1-3: need increasing supply voltage for no bit errors during irradiation. One died at ~37 Mrad.
- DORIC #4: no signal after installation.
- DORIC #5: continue to operate at 3.2 V with no bit errors.

☆ annealing gives no significant improvement in bit error threshold

Opto-Board Irradiation Post-Mortem

Link	2	4	5	6
Dosage (Mrad)	?	16	0.9	29
VDC ⇨ DORIC:				
Pre-irrad (μA)	13	17	65	30
Post-irrad (μA)	24	>170	>119	dead
Anneal (μA)	24	37	>74	dead
DORIC ⇨ VDC:				
Pre-irrad (μA)	56	12	61	30
DORIC ⇨ VDC4:				
Anneal (μA)	53	64	37	dead

- DORIC #4: threshold for no bit errors depends strongly on voltage
- VDC #5: light output depends on input data
- ☆ annealing gives no significant improvement in bit error threshold

VDC-D2/DORIC-D2 Irradiation Summary

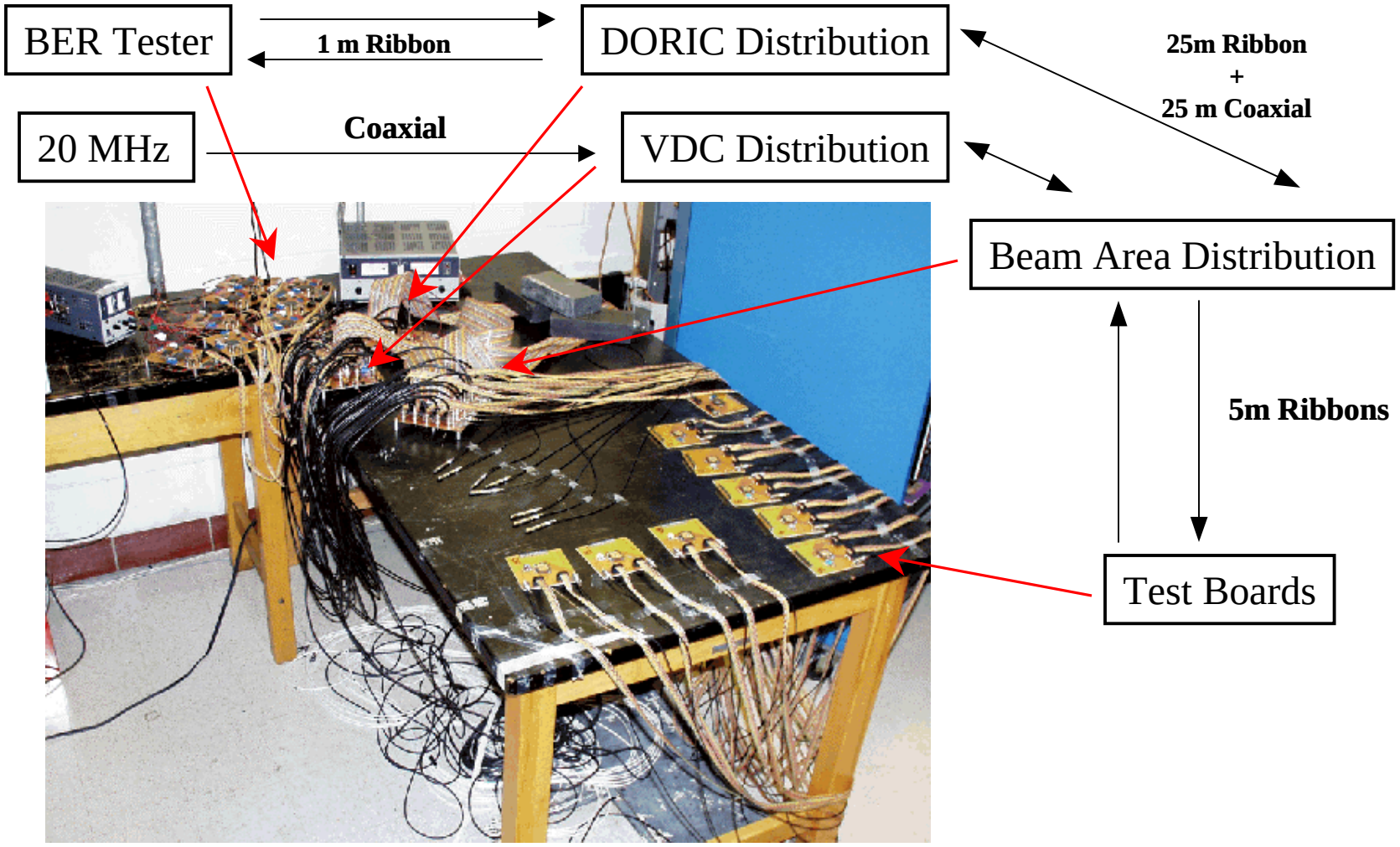
- degradation of some VDC/DORIC during irradiation
- some VDC/DORIC died during irradiation
- ☆ annealing gives no significant improvement in bit error threshold and failed to revive dead die
- ⇨ VDC-D2/DORIC-D2 appear to be not radiation hard enough for pixel detector

September Irradiation of Opto-Electronics

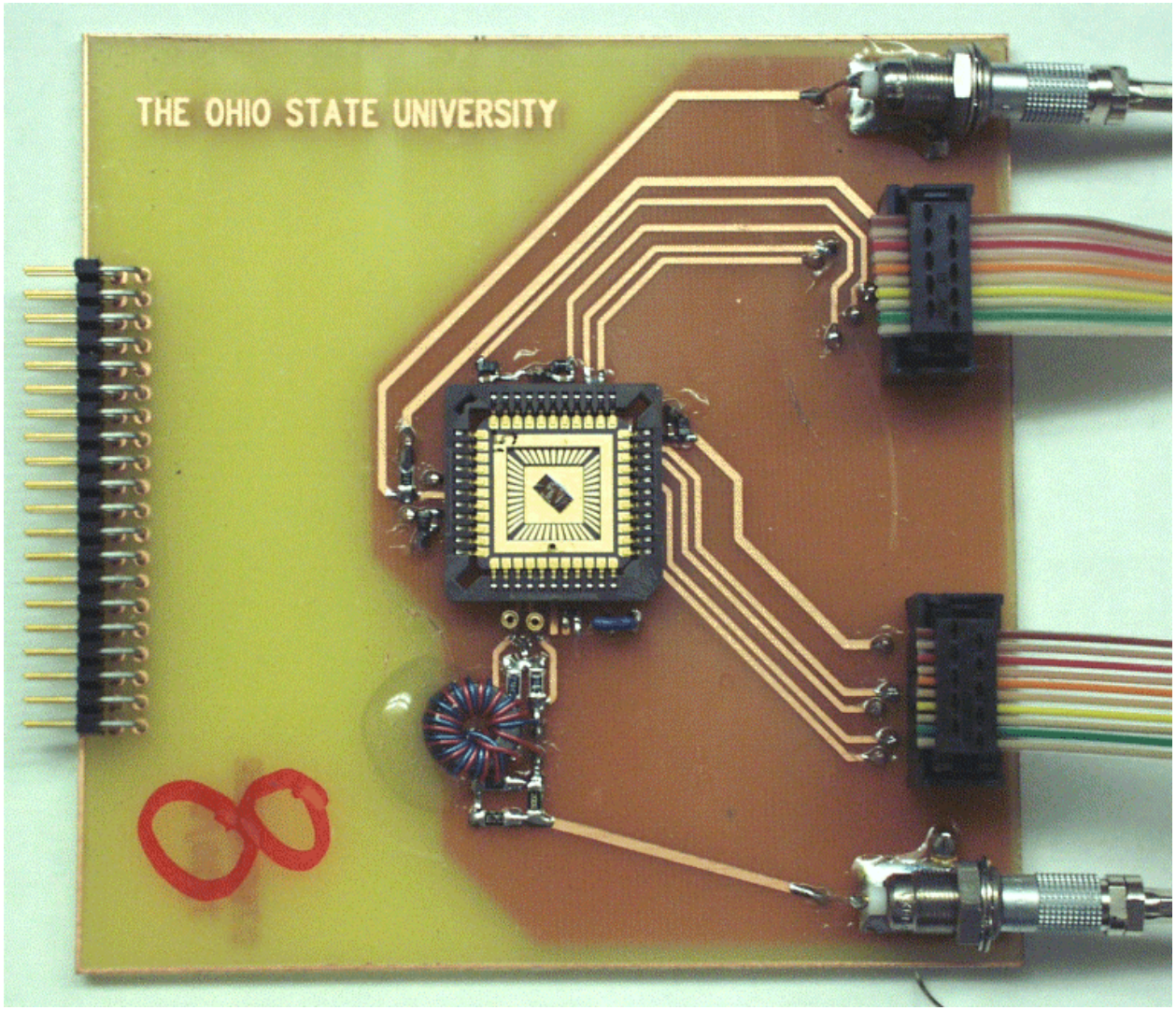
- use 24 GeV proton test beam at T7
- cold box: purely electrical testing of VDC-I1 and DORIC-I1
- shuttle system: testing of 5 optical links on opto-board

- test beam team:
  Kregg Arms, K.K. Gan, Clemens Ringpfeil,Shane Smith
  with special help from Petr Sicho

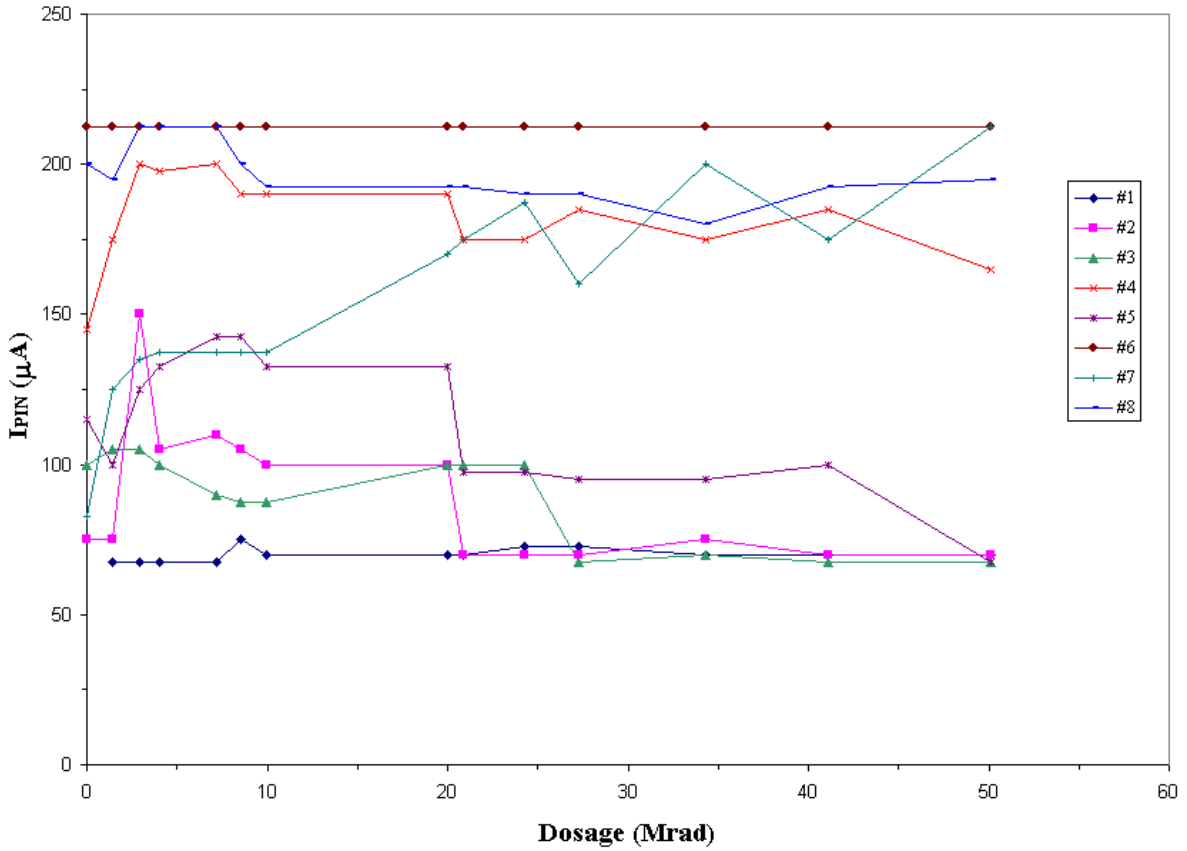
Test Boards for Irradiation in Cold Box



Close view of Cold Box Board

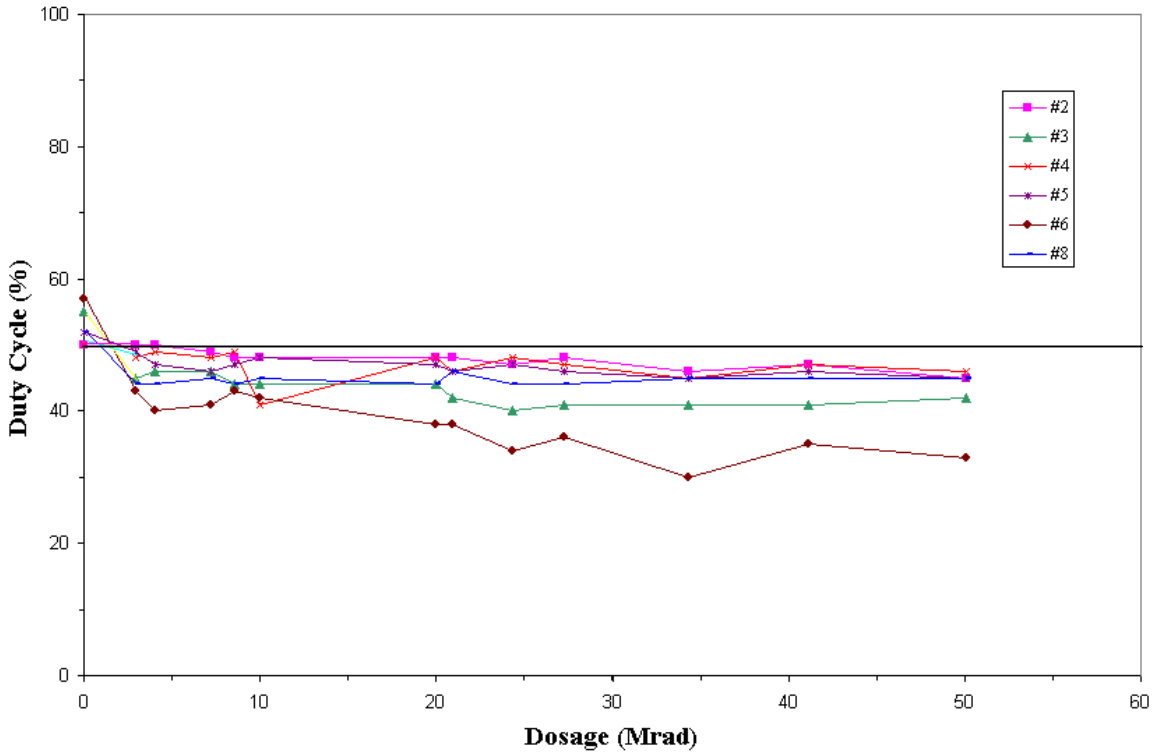


DORIC-I1 Bit Error Threshold vs Dosage



- PIN current thresholds for no bit errors remain constant up to 50 Mrad, except DORIC #7 which was damaged electrically.

Duty Cycle of Decoded Clock vs Dosage



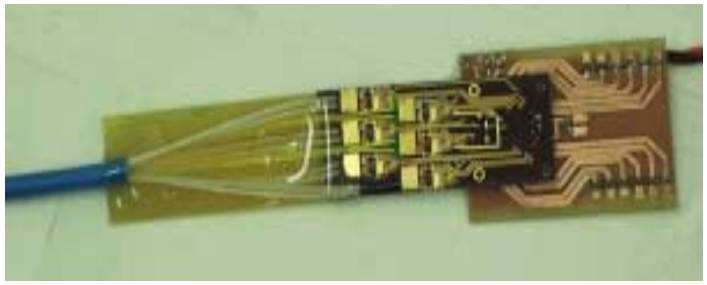
- duty cycle of clock decoded by DORIC-I1 remains constant up to 50 Mrad, except for die #6 which was untested before irradiation

Packaged DORIC-I1 Irradiation Post-Mortem

DORIC	#1	#2	#3	#4	#5
Pre-irrad BER Threshold (μA)	150	?	130	124	102
Post-irrad BER Threshold (μA)	150	240	129	60	174
Pre-irrad Duty Cycle (%)	48.8	?	45.6	47.4	49.2
Post-irrad Duty Cycle (%)	47.8	43.8	46.0	47.6	46.8

- DORIC #5: wire bonds crushed
  ⇨ die may be damaged
- ☆ no degradation in bit error threshold or clock duty cycle a month after irradiation

Test Boards for Irradiation in Shuttle



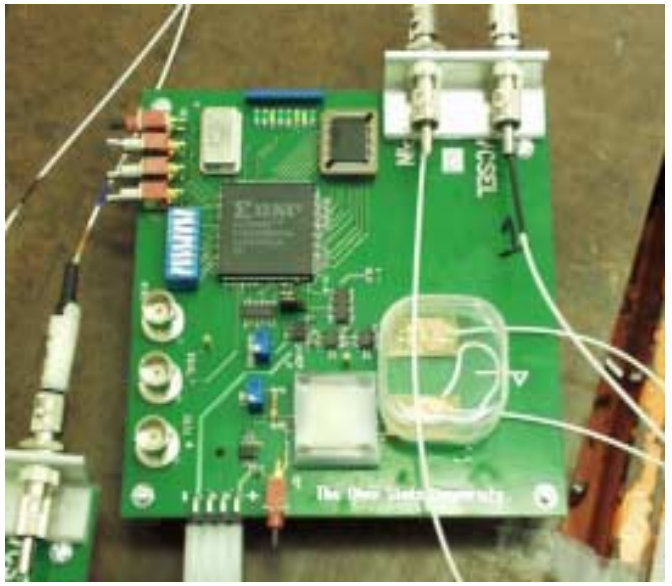
Opto-board with 6 opto-links

Bi-phase marked optical signal

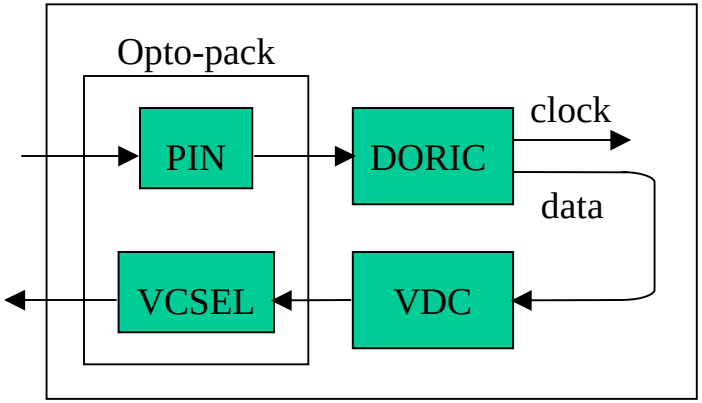
25 m fibers/wires

Decoded data

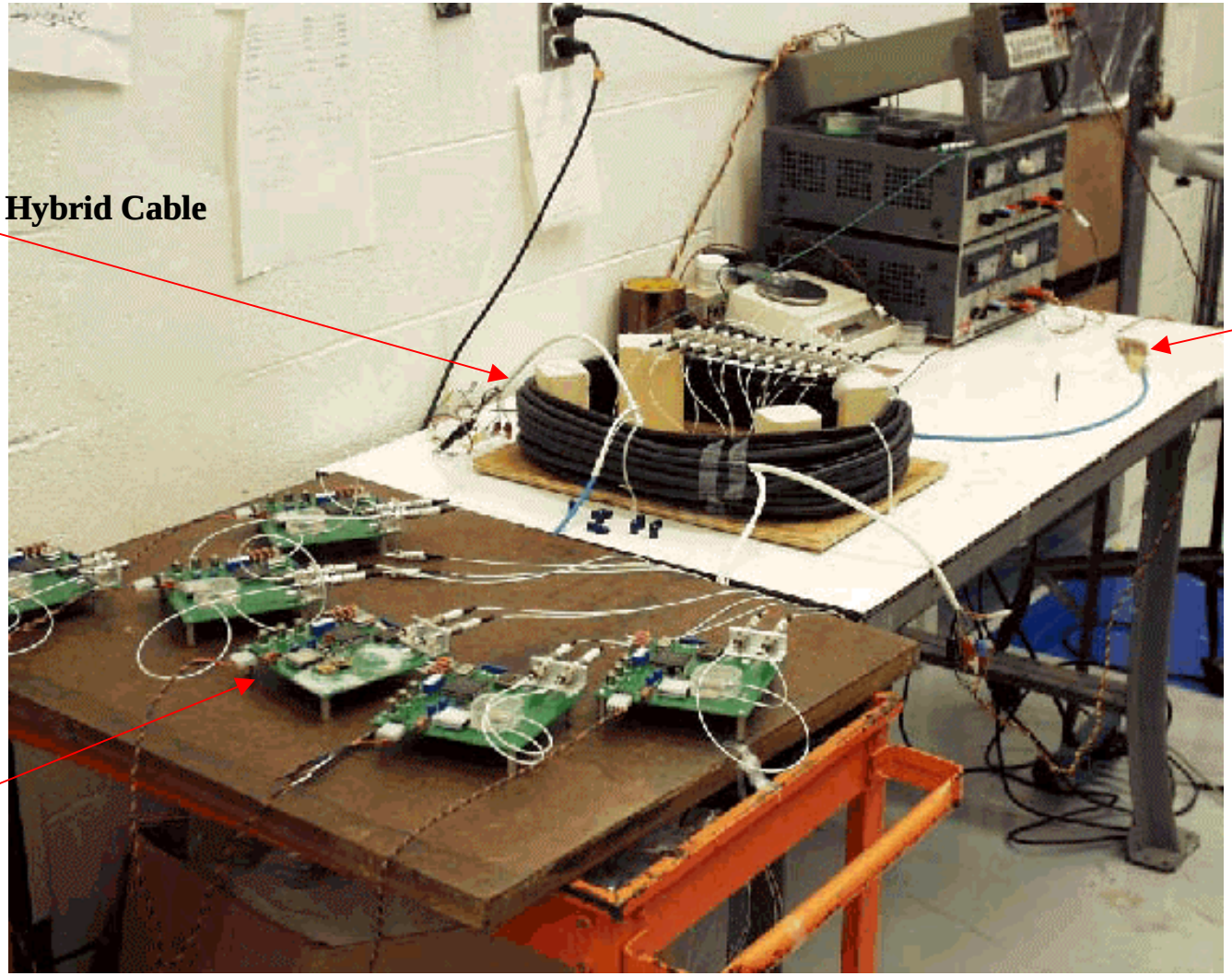
Bit error test board in control room
(6 boards)



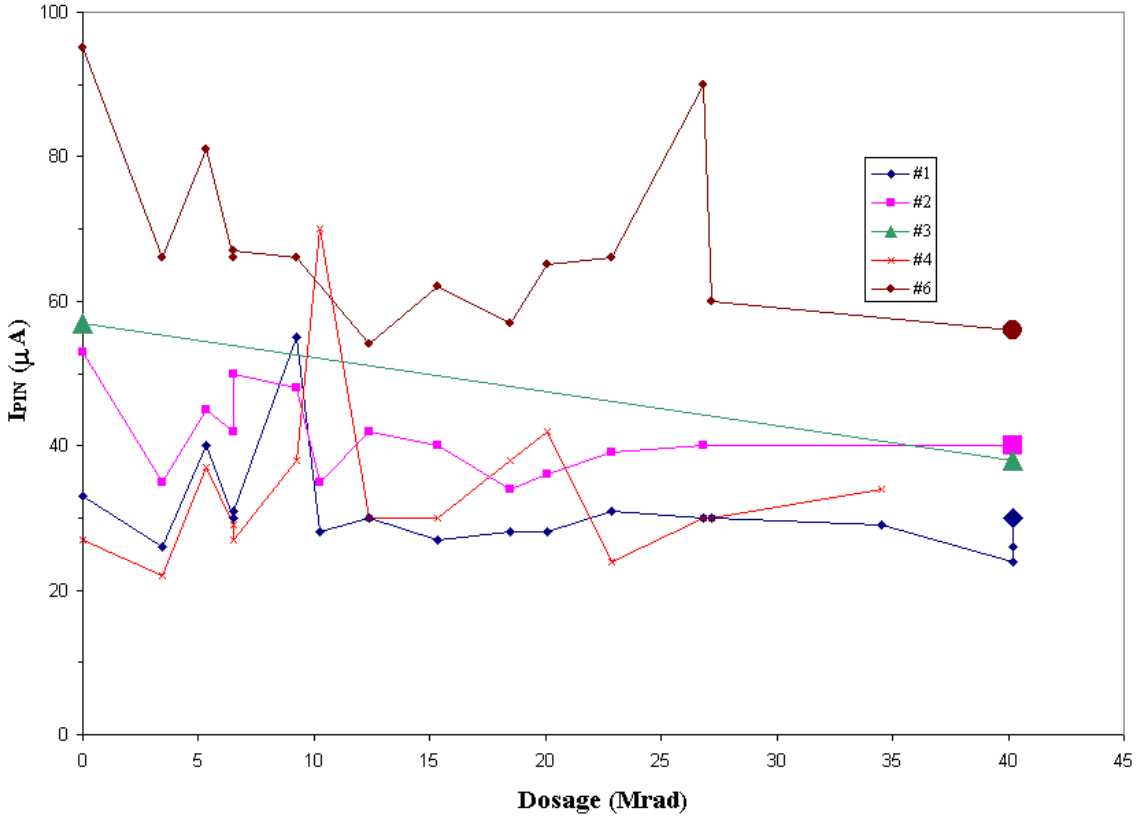
Opto-link



Opto-Board Test System for Shuttle

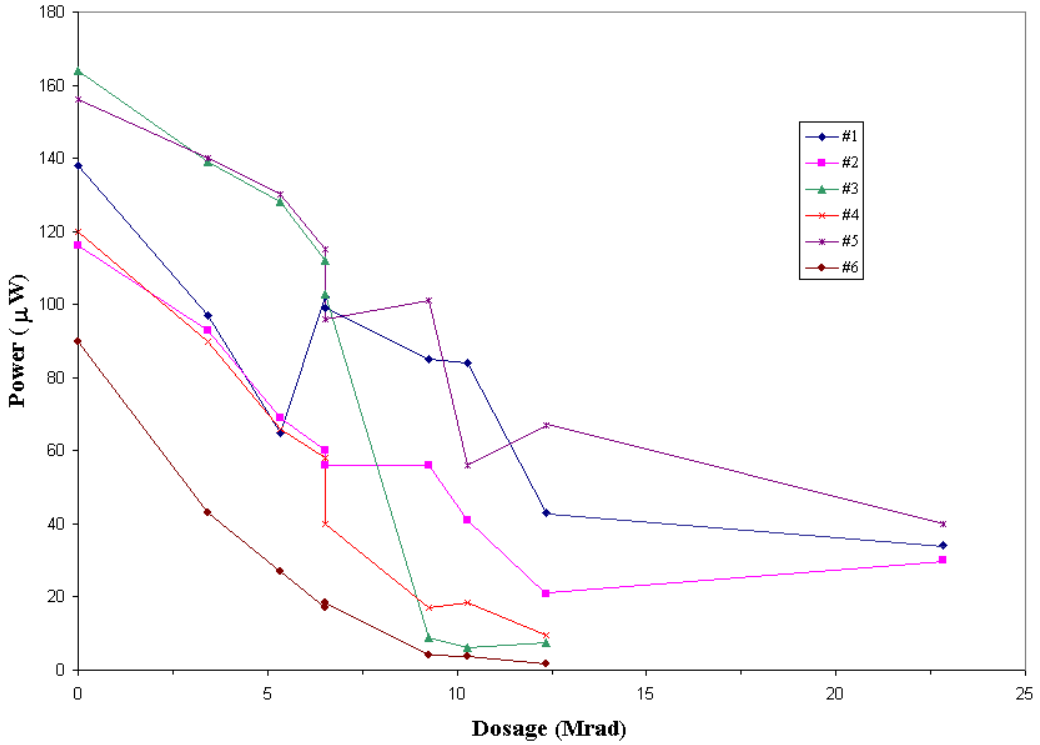


Opto-Board Bit Error Threshold vs Dosage



- bit error threshold for no bit errors remains constant up to 40 Mrad
- no further degradation a month after irradiation

Optical Power vs Dosage



- optical power decreases drastically with dosage:
  - ☆ annealing at ~ 3 Mrad failed to yield more light
    - ⇨ need longer annealing further away from beam

Summary of VDC-I1/DORIC-I1 Irradiation

- VDC-I1/DORIC-I1 continue to perform well after 40-50 Mrad
- ☆ new robust test system allows continuous monitoring with diminishing light return

Plans for DORIC-I3

- use single-end pre-amp to avoid large PIN voltage on die
- better delay control circuit
- will submit in November as MPW run

Summary/Plan

- VDC-I1/DORIC-I1 basically work!
- many improvements implemented in VDC-I2/DORIC-I2
- radiation hardness of VDC-D2/DORIC-D2 appears inadequate for pixel system
- radiation hardness of VDC-I1/DORIC-I1 appears adequate for pixel system!