New Results on Opto-Electronics

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December 4, 2001

Outline

- Introduction
- Preliminary Results on VDC-D3/DORIC-D3
- Results on VDC-I1/DORIC-I1 Irradiation
- Improvements in VDC-I2/DORIC-I2
- Improvements in VDC-I3/DORIC-I3
- Summary

Introduction

- VCSEL Driver Chip (VDC):
  - convert LVDS signal into single-ended signal appropriate to drive VCSEL
- Digital Opto-Receiver Integrated Circuit (DORIC):
  - decode clock and command signals from PIN diode

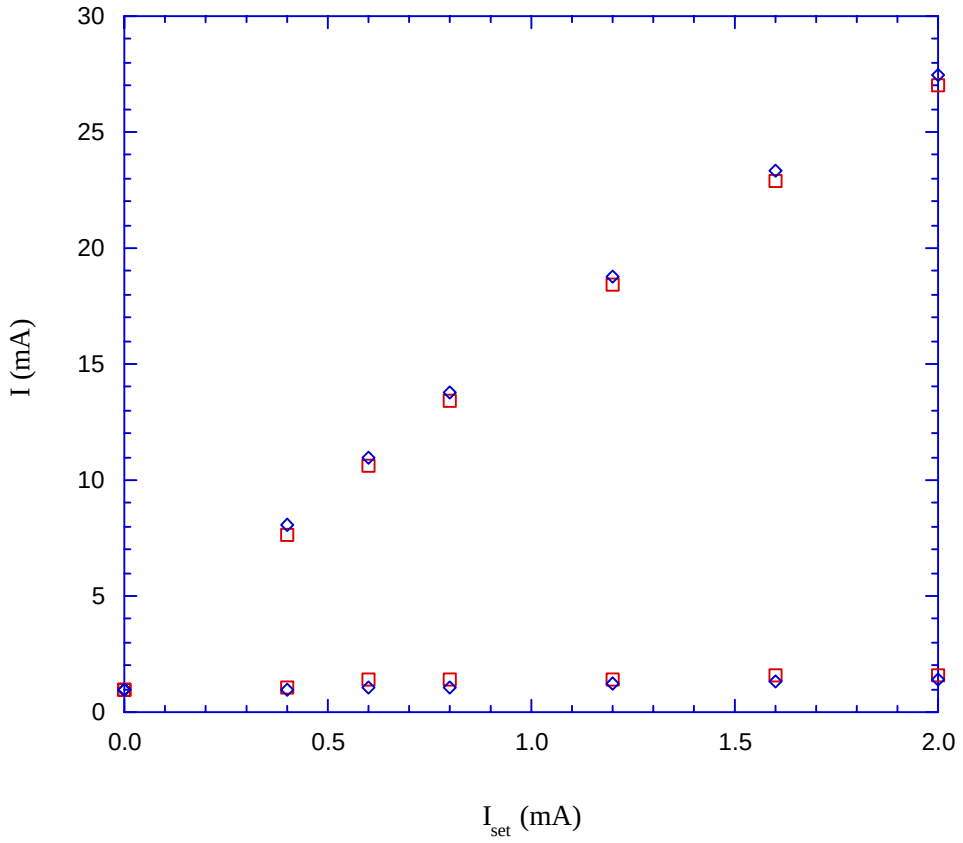
Opto-electronics Team

- The Ohio State University:
  - Kregg Arms, K.K. Gan, Mark Johnson, Harris Kagan, Richard Kass, Chuck Rush, Rouben Ter-Antonian, Michael Zoeller
- Siegen University:
  - Michael Kraemer, Joachim Hausmann, Martin Holder, Michal Ziolkowski

VDC-D3

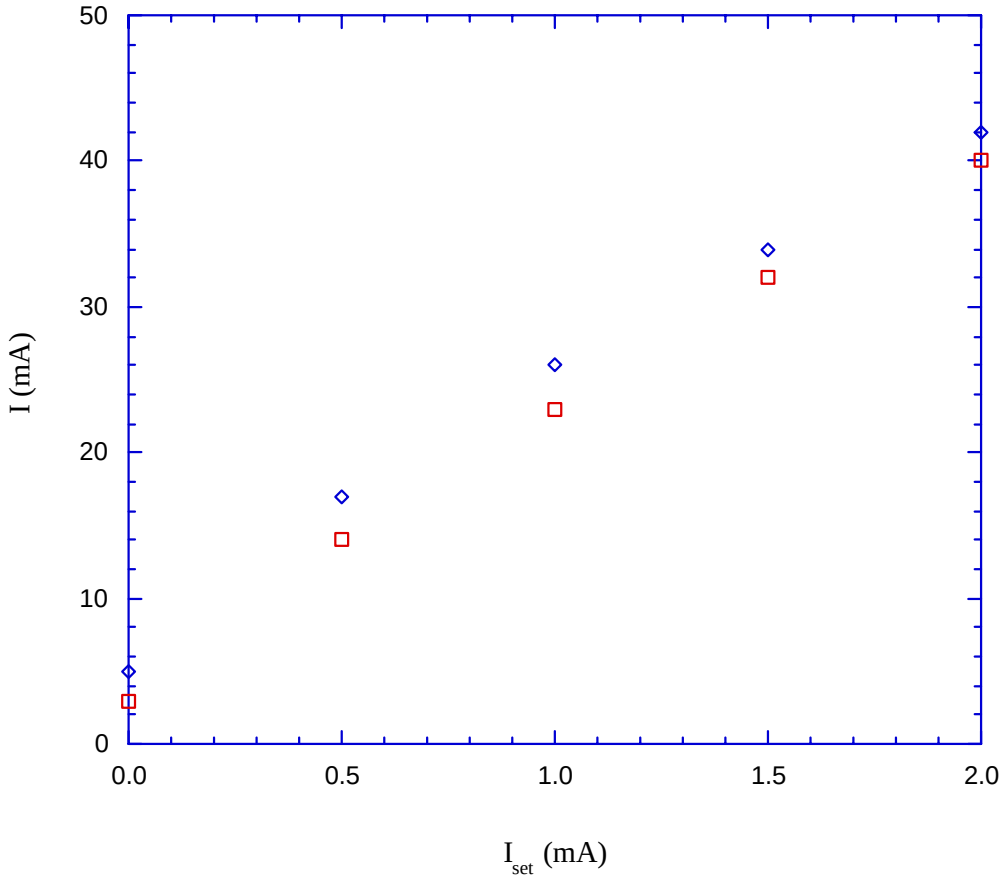
- two designs were submitted
  - VDC-D3:
    - new circuit to decouple bright/dim current adjustments
    - SCT bias circuit
  - VDC-D3P:
    - same as VDC-D3 but with poly resistor in bias circuit

VCSEL Currents vs I_{set}



- dependence of bright/dim currents on I_{set} is as expected

Current Consumption of VDC-D3



- VDC-D3 consumes ~ 17 mA for 10 mA VCSEL current @ 3.2 V
  - similar to VDC-D2

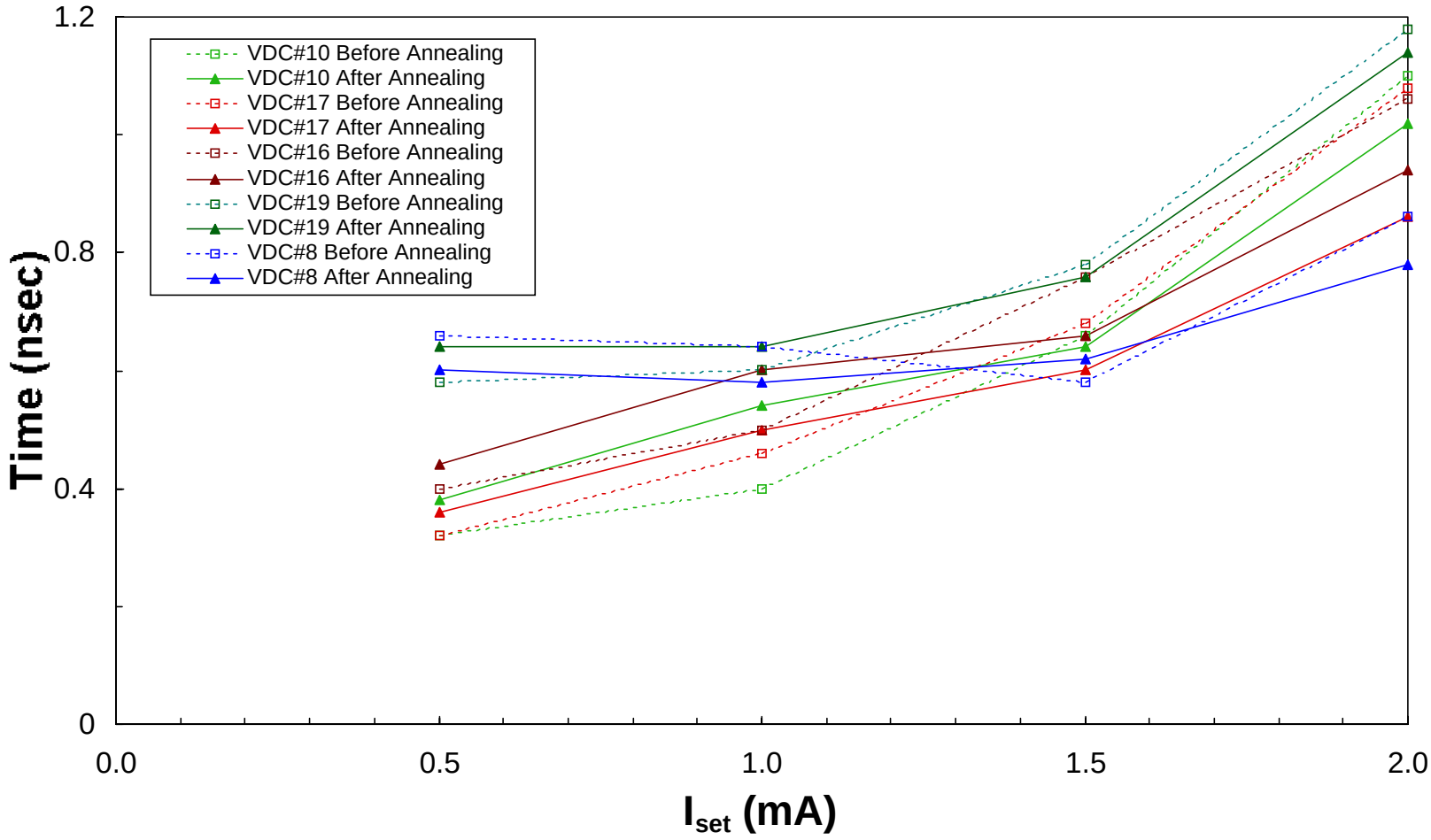
DORIC-D3

- changes:
  - new pre-amp with DC feedback to cancel offset at differential inputs
  - SCT LVDS driver
- preliminary results:
  - clock has 50% duty cycle at CMOS driver and before LVDS driver
  - clock has 40% duty cycle at LVDS driver
  - 100 mV clock-like ripple on 1.6 V delay control line
  - ☆ ~ 50 μA minimum PIN current for no bit errors for 2 dice in packages + one die on opto-board III
  - ⇨ DC feedback is working

September Irradiation of Opto-Electronics

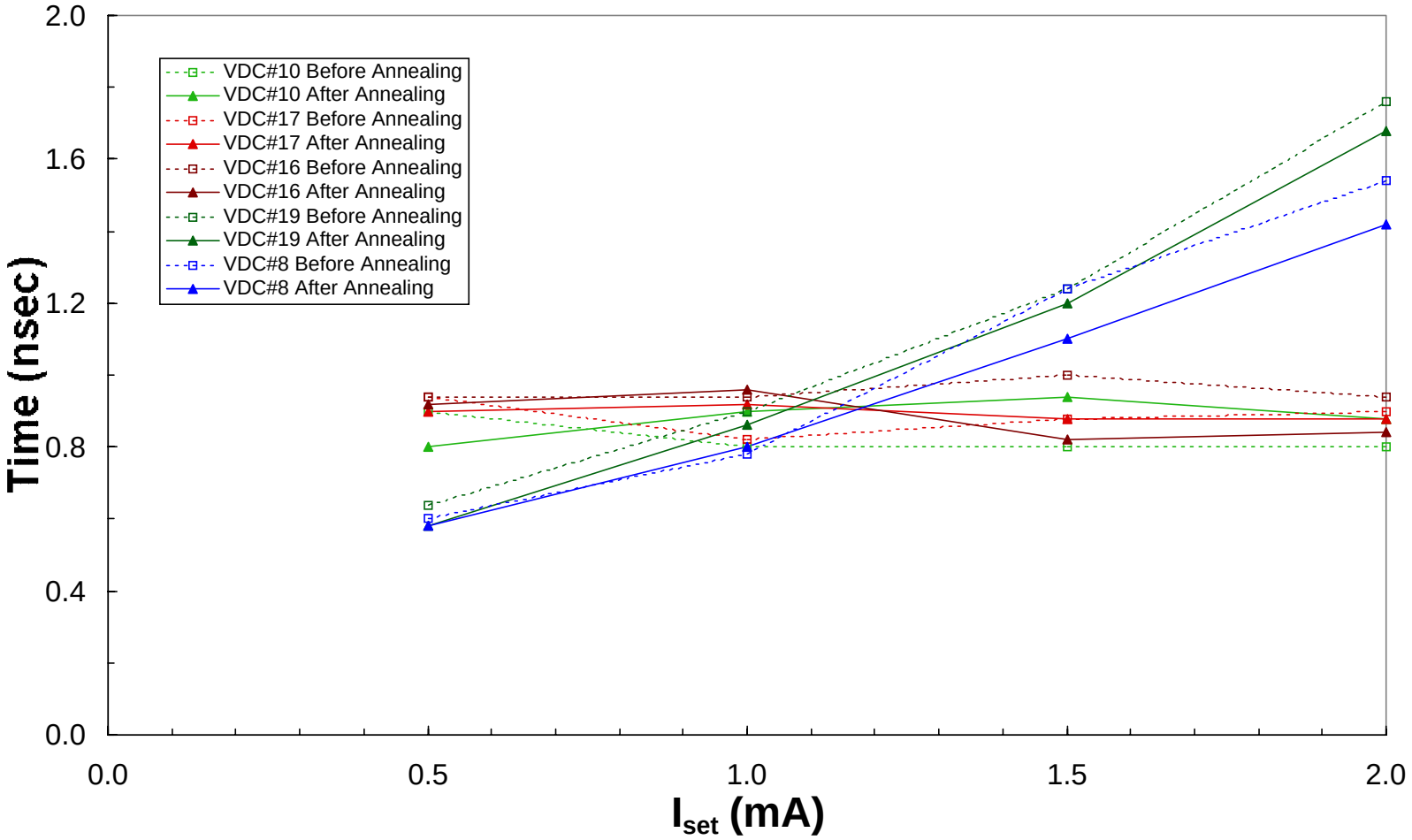
- use 24 GeV proton test beam at T7
- cold box: purely electrical testing of VDC-I1 and DORIC-I1
- shuttle system: testing of 5 optical links on opto-board

Rise Time of Irradiated VDCs Before and After Annealing



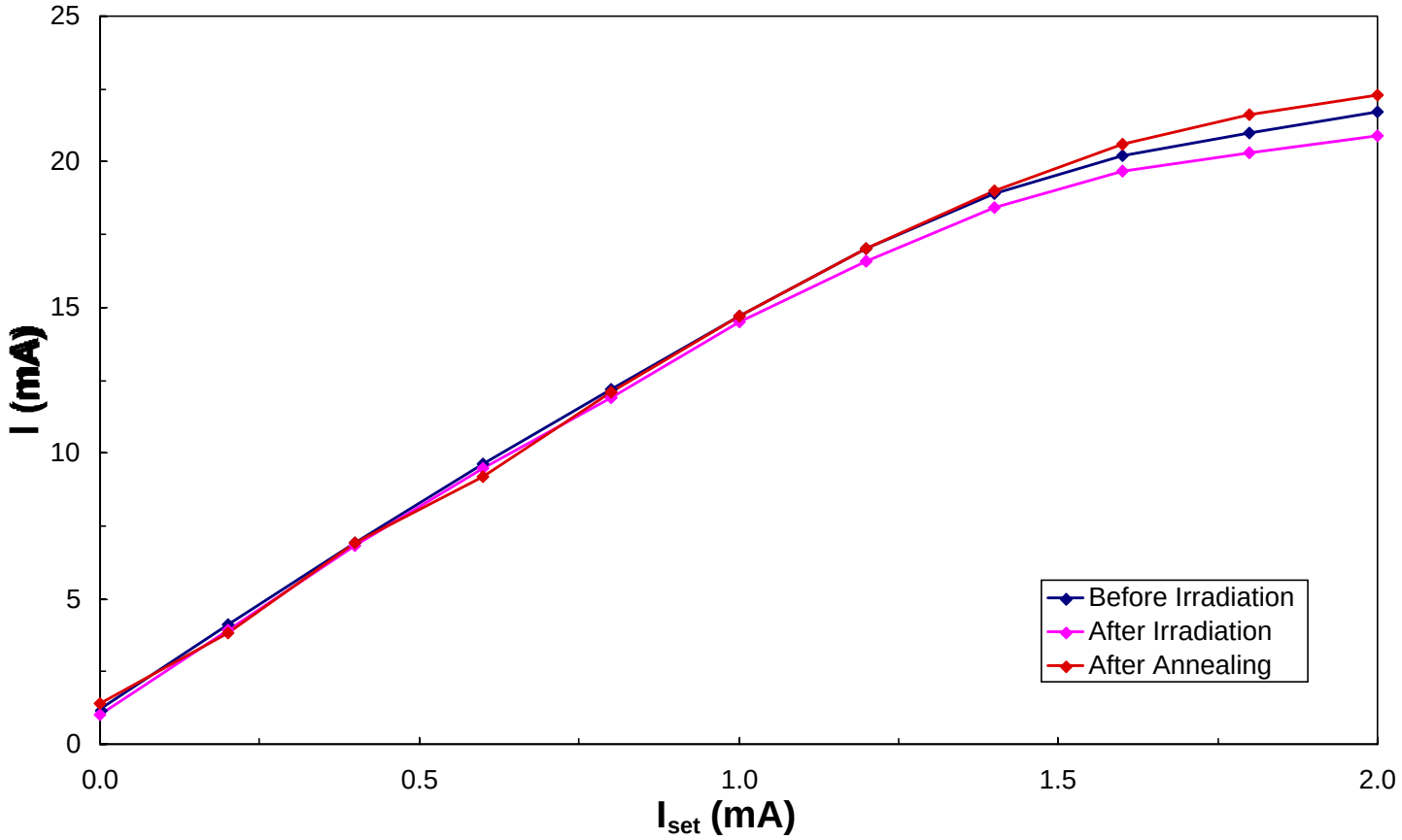
- annealing produces no significant change

Fall Time of Irradiated VDCs Before and After Annealing



- annealing produces no significant change

Bright Current of Irradiated VDCs Before and After Annealing



- irradiation slightly reduces light output
- annealing slightly increases light output

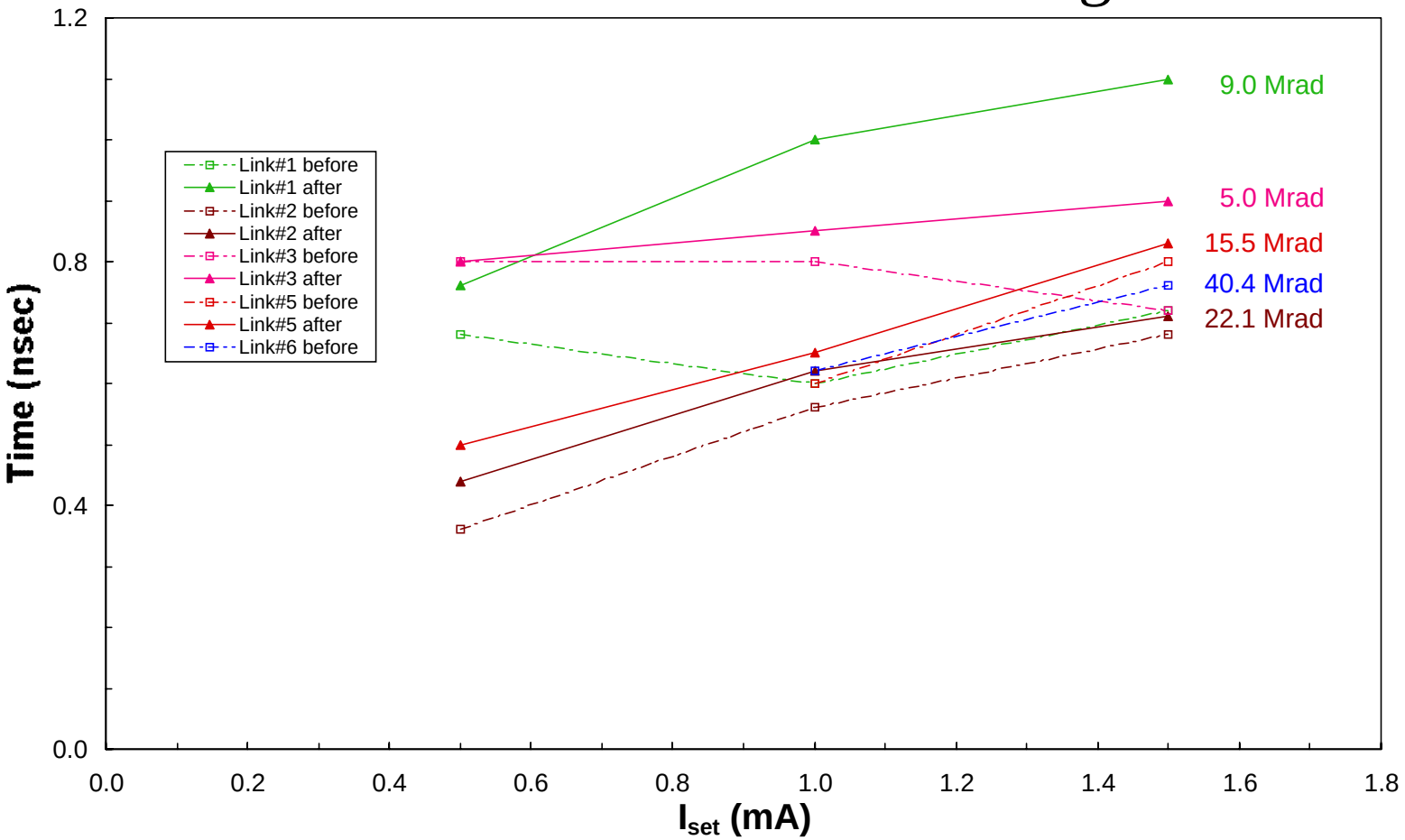
Packaged DORIC-I1 Irradiation

DORIC	#1	#2	#3	#4	#5
Pre-irrad BER Threshold (μA)	150	?	130	124	102
Post-irrad BER Threshold (μA)	150	240	129	174	60
Post-annealing BER Threshold (μA)	104	172	121	149	445
Pre-irrad Duty Cycle (%)	48.8	?	45.6	47.4	49.2
Post-irrad Duty Cycle (%)	47.8	43.8	46.0	46.8	47.6
Post-annealing Duty Cycle (%)	46.8	44.0	44.0	45.4	47.4

4

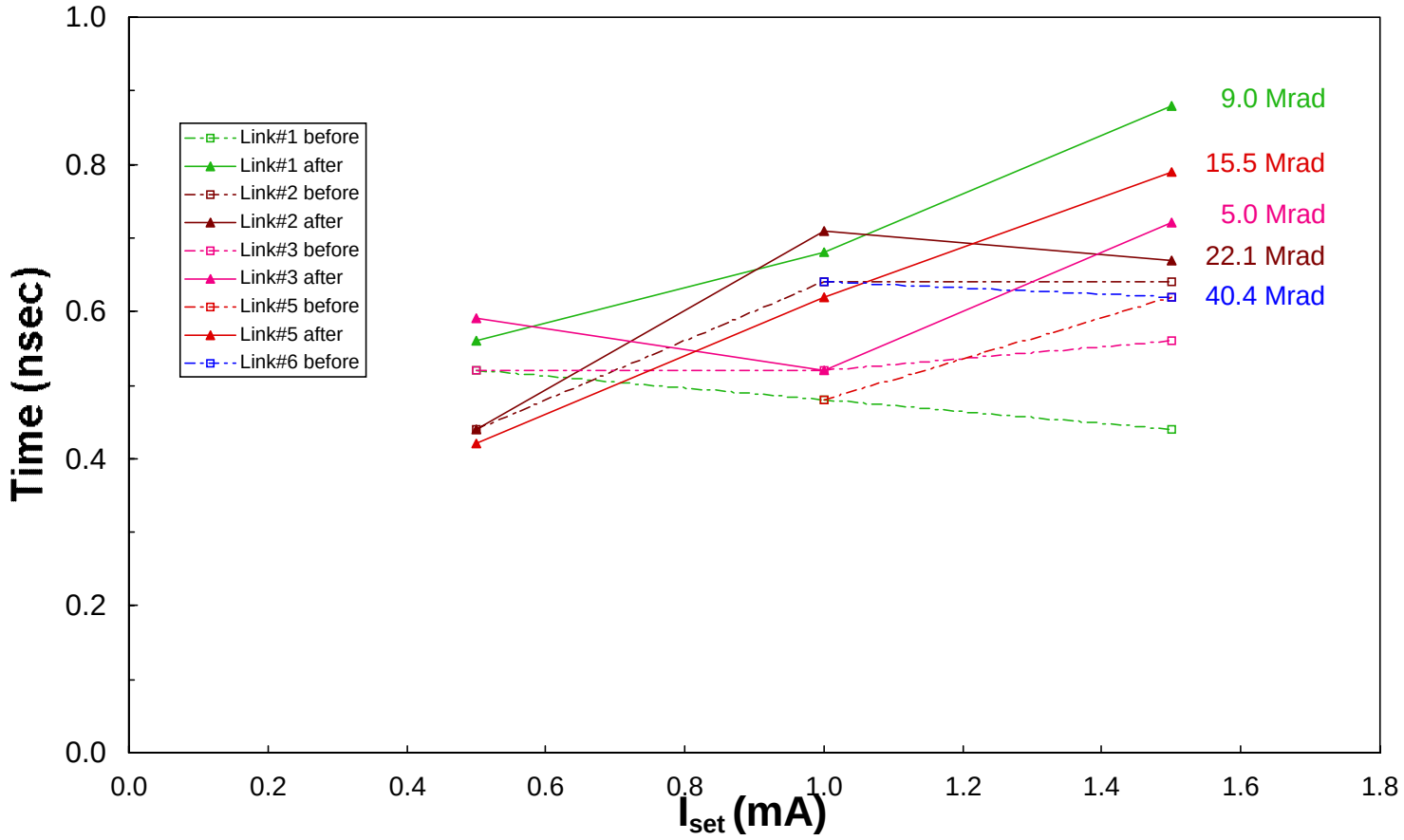
- DORIC #4: wire bonds crushed ⇨ die may be damaged
- after irradiation and annealing:
  - ☆ no degradation in bit error threshold except one die
  - ☆ no degradation in clock duty cycle

Rise Time of VDC/VCSEL on Irradiated Opto-board Before and After Annealing



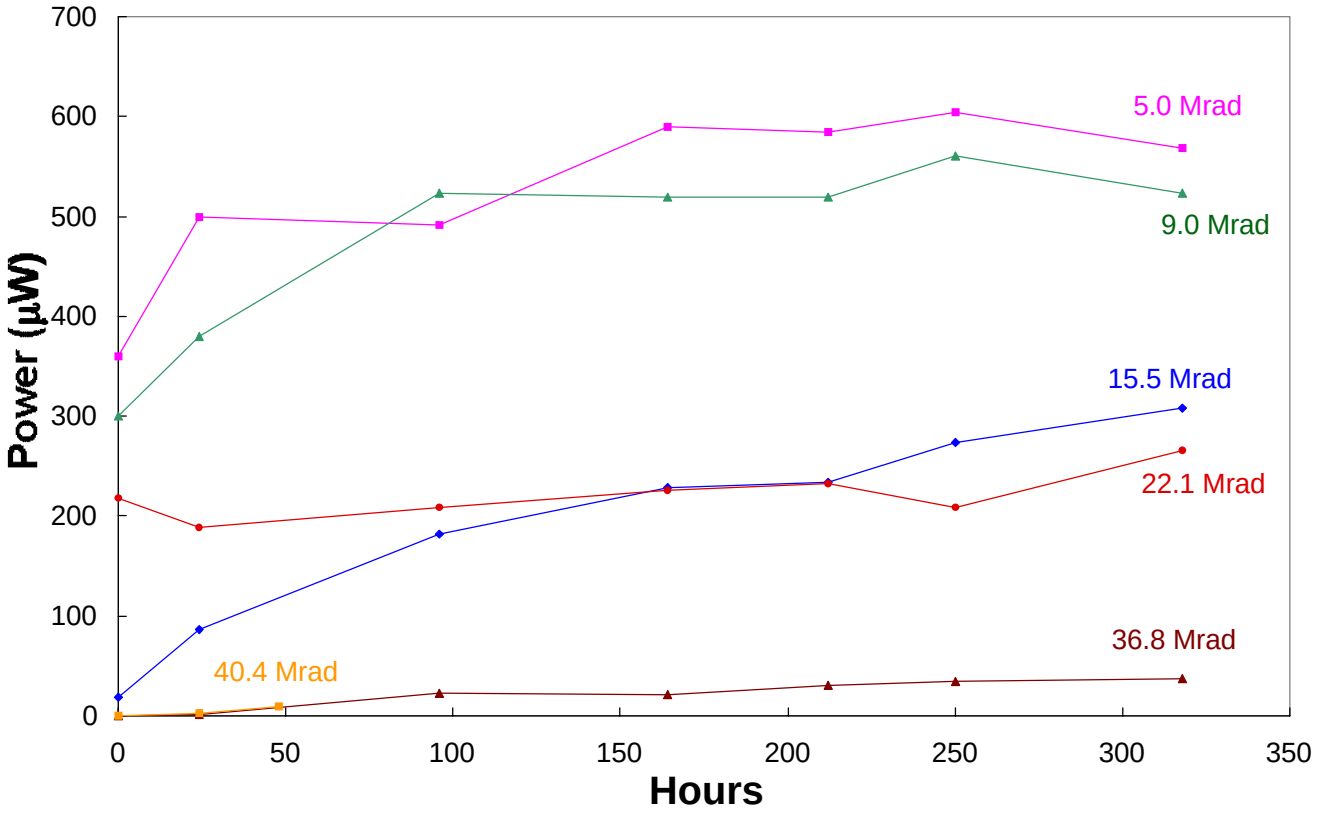
- VCSELs have slightly slower rise time after annealing

Fall Time of VDC/VCSEL on Irradiated Opto-board Before and After Annealing



- VCSELs have slightly slower rise time after annealing

Optical Power of Irradiated Opto-board Before and After Annealing



- VCSEL power reaches plateau after a week of annealing
- fibers with various dosages have same insertion lost: ~15%
  ⇨ failure for VCSEL to anneal is due to radiation damage

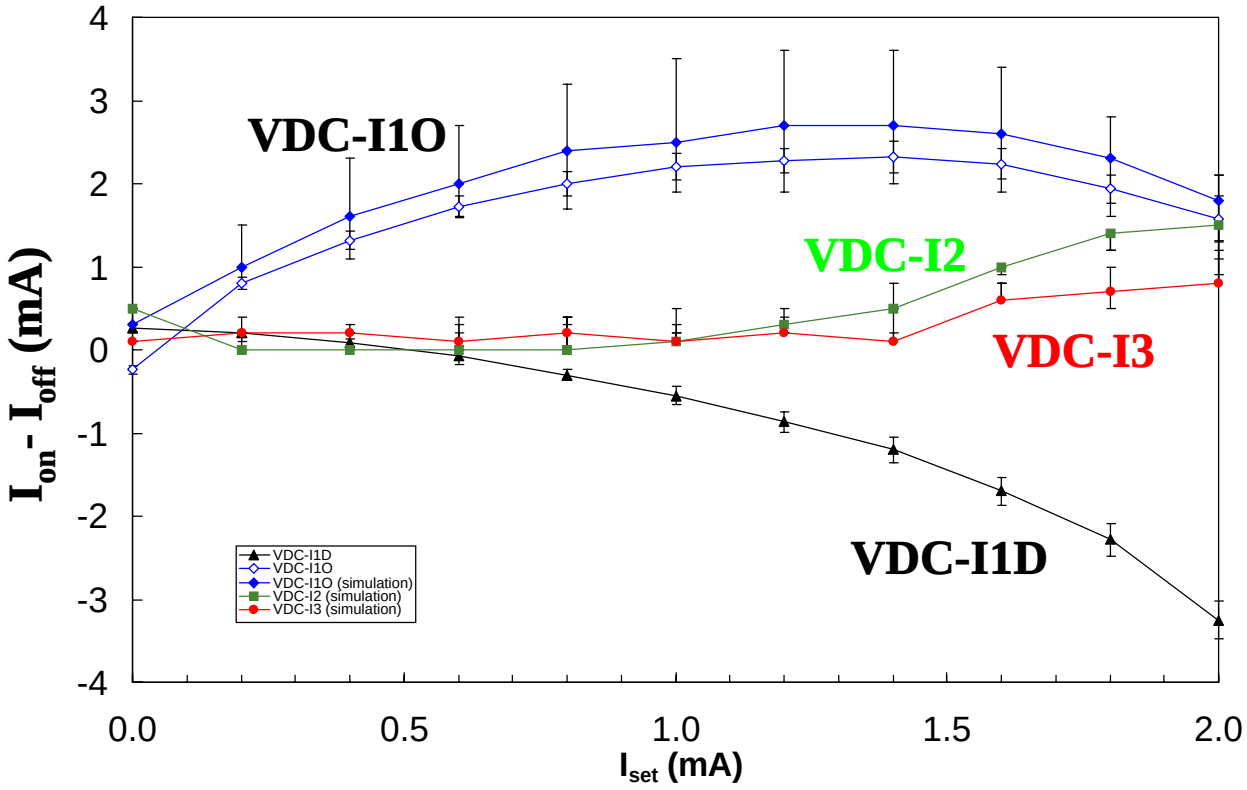
Summary of VDC-I1/DORIC-I1 Irradiation

- VDC-I1/DORIC-I1 continue to perform well after 40-50 Mrad
- changes after irradiation/annealing are small
  except one die which has much higher bit error threshold

Improvements in VDC-I2/VDC-I3

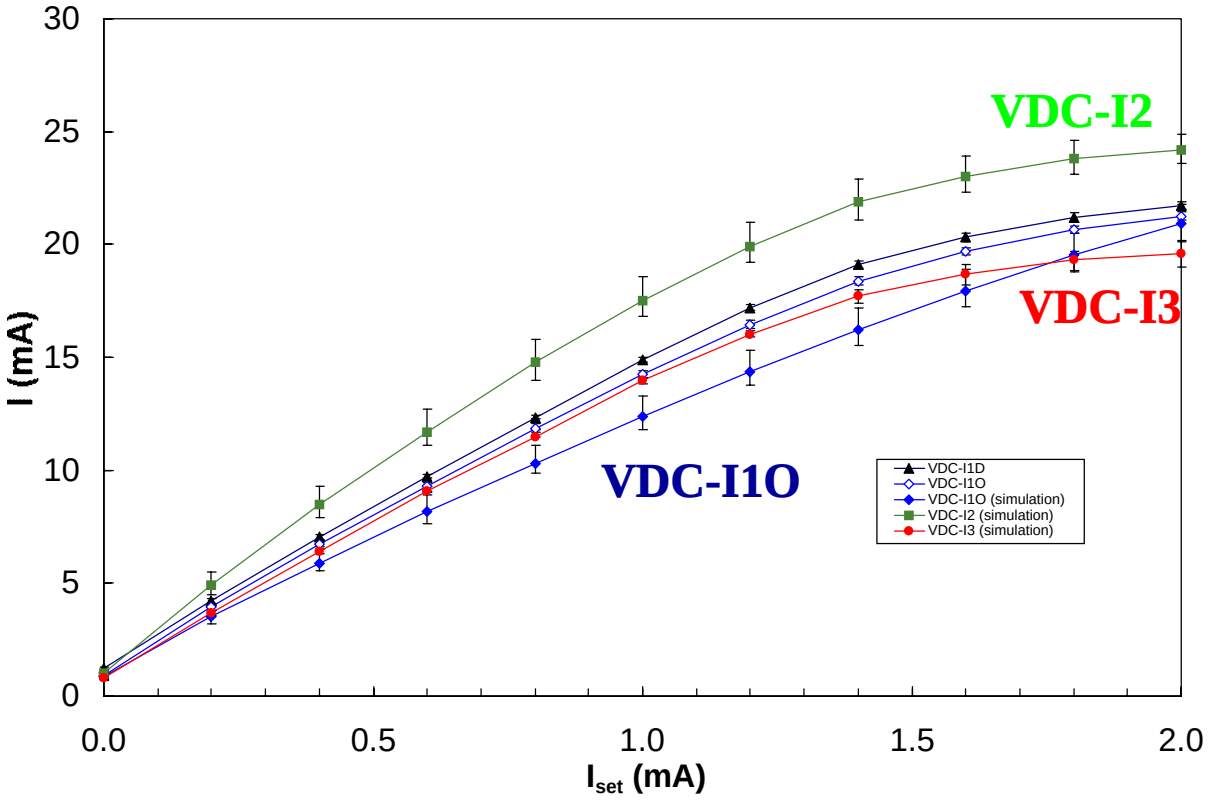
- VDC-I2:
  - keep OSU design that decouples adjustment of bright and dim currents
  - new circuit that equalizes bright and dim current consumption
  - new LBL pads
  - submitted two designs: single and four-channel VDC
- VDC-I3:
  - further equalize bright and dim current consumption
  - consume less current
  - submitted single channel VDC in MPW

Bright and Dim Current Consumption vs I_{set}



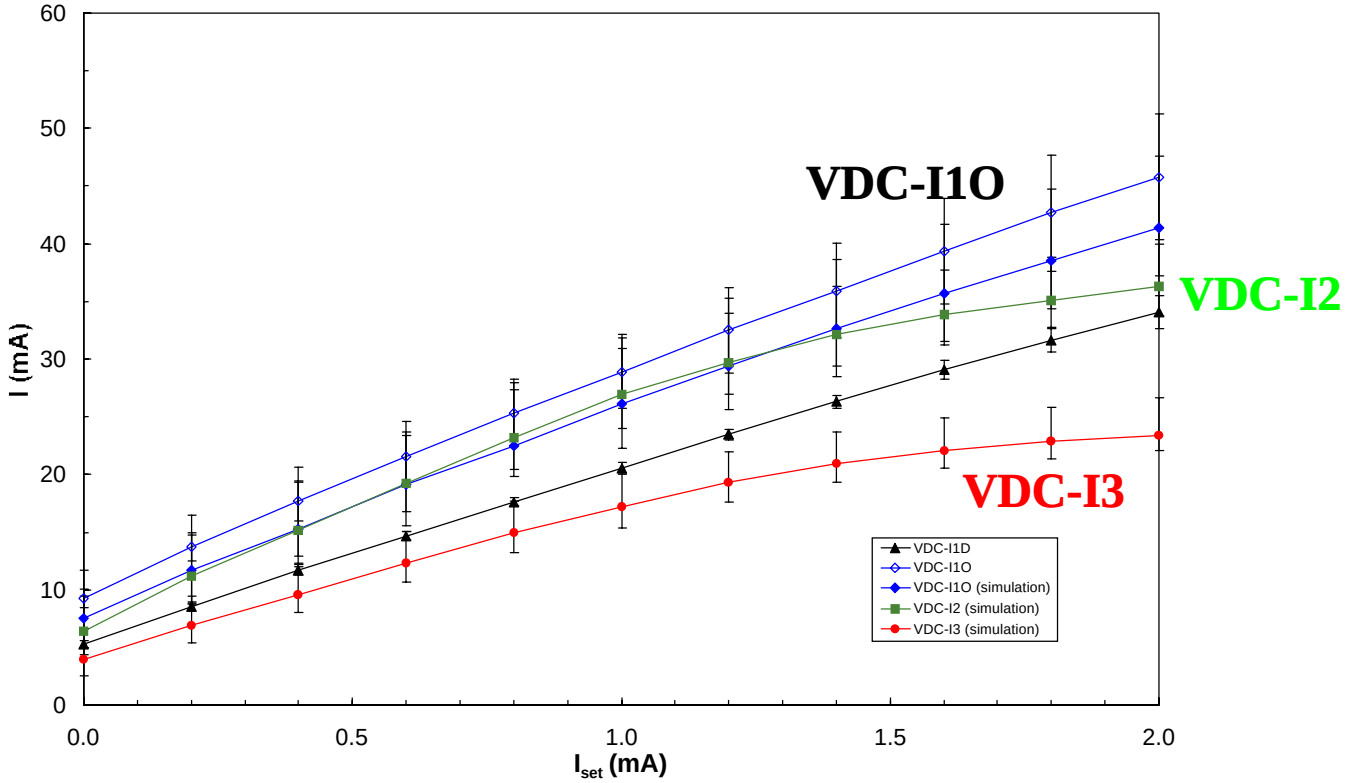
- simulation of VDC-I1O reproduces observation
- VDC-I2 has much more equal bright and dim current consumption
- VDC-I3 further equalizes the current consumption

Bright Current vs I_{set} with 10 Ω in Series



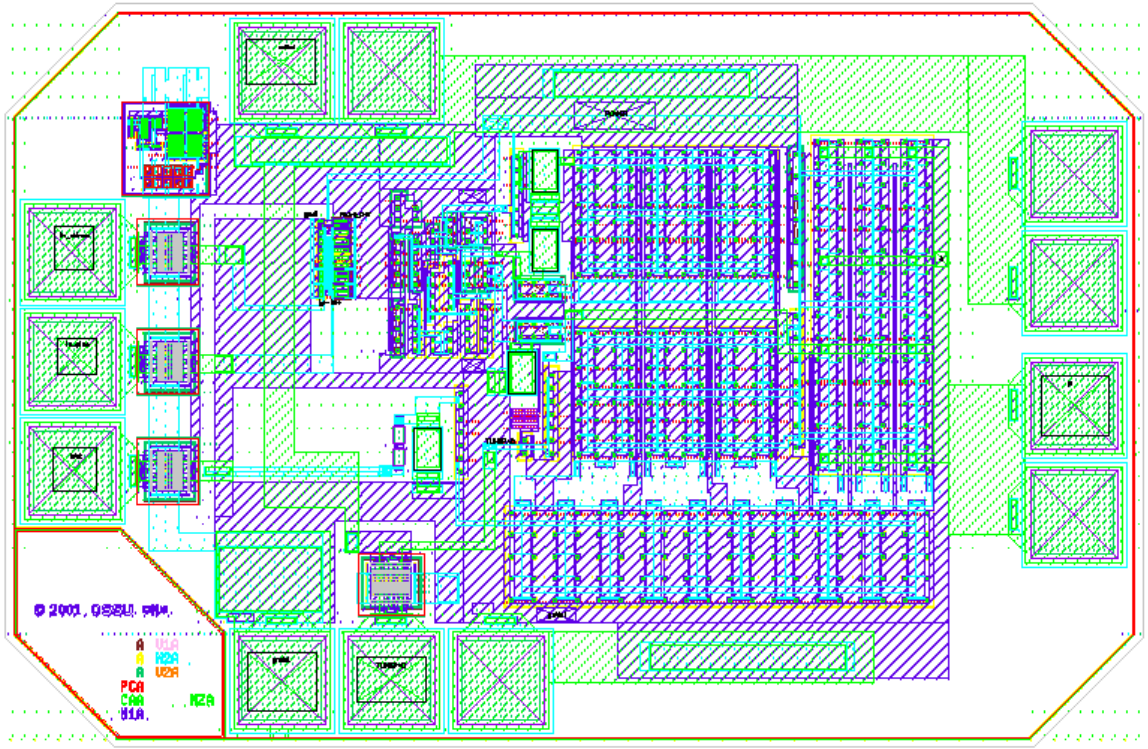
- simulation of VDC-I1O reproduces observation
- VDC-I3 has smaller bright current than VDC-I2
- VDC-I3 has a maximum of 22 mA without 10 Ω in series

VDC Current Consumption

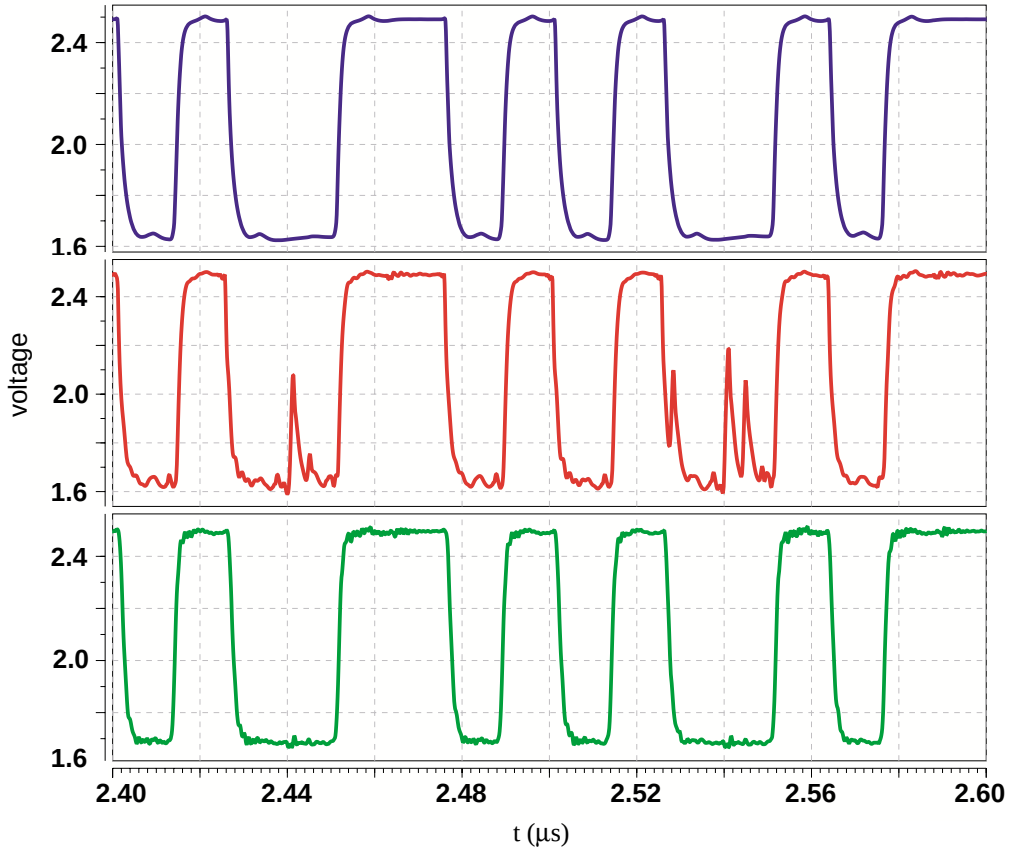


- simulation of VDC-I1O reproduces observation
- VDC-I3 consumes significantly less current

VDC-I3



Simulation of DORIC-I1/I2 from Extracted Layout with Stray Capacitance plus Wire Bonds



DORIC-I1
40 μA
No wire bonds

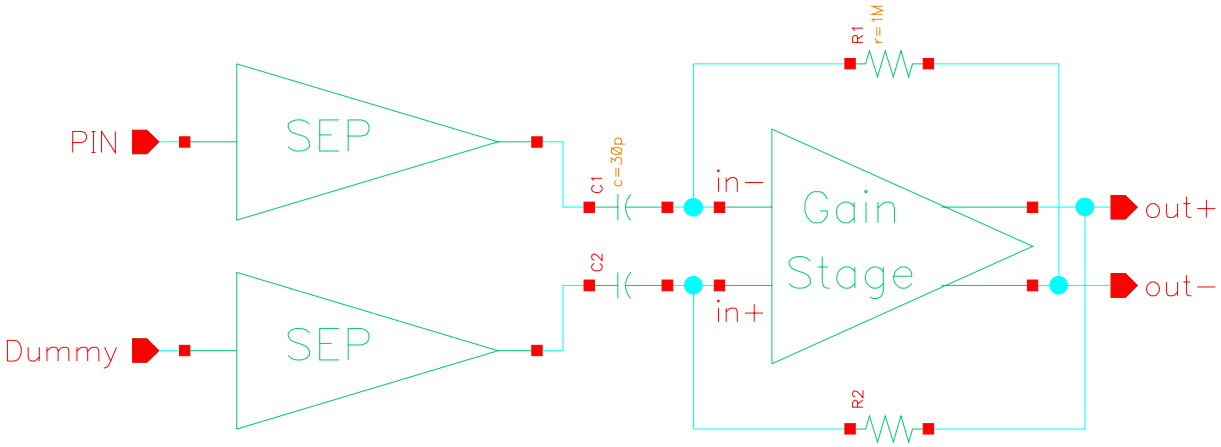
DORIC-I1
160 μA

DORIC-I2
40 μA

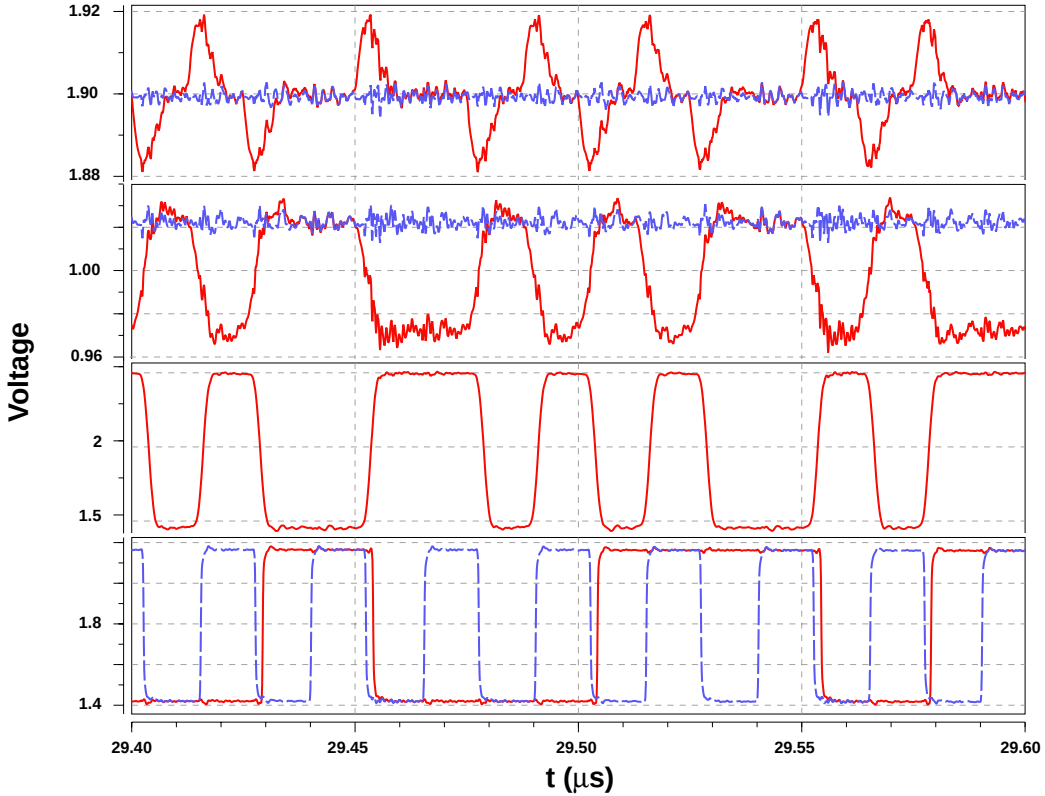
- DORIC-I1: needs large PIN current for no bit errors
  - ☆ predict spikes as observed in lab
- DORIC-I2: can run at low PIN current (12 μA) with no bit errors

Improvements in DORIC-I2/DORIC-I3

- DORIC-I2: differential pre-amp
  - ☆ numerous improvements
- DORIC-I3: single-ended pre-amp
  - ☆ add dummy channel to cancel noise
    except white noise which adds in quadrature
  - ☆ reduce maximum delay (2.0 ⇨ 1.5 x) in delay control loop
    to further reduce possibility of locking at half frequency



Simulation of DORIC-I3 from Extracted Layout with Stray Capacitance plus Wire Bonds



Pre-amp input

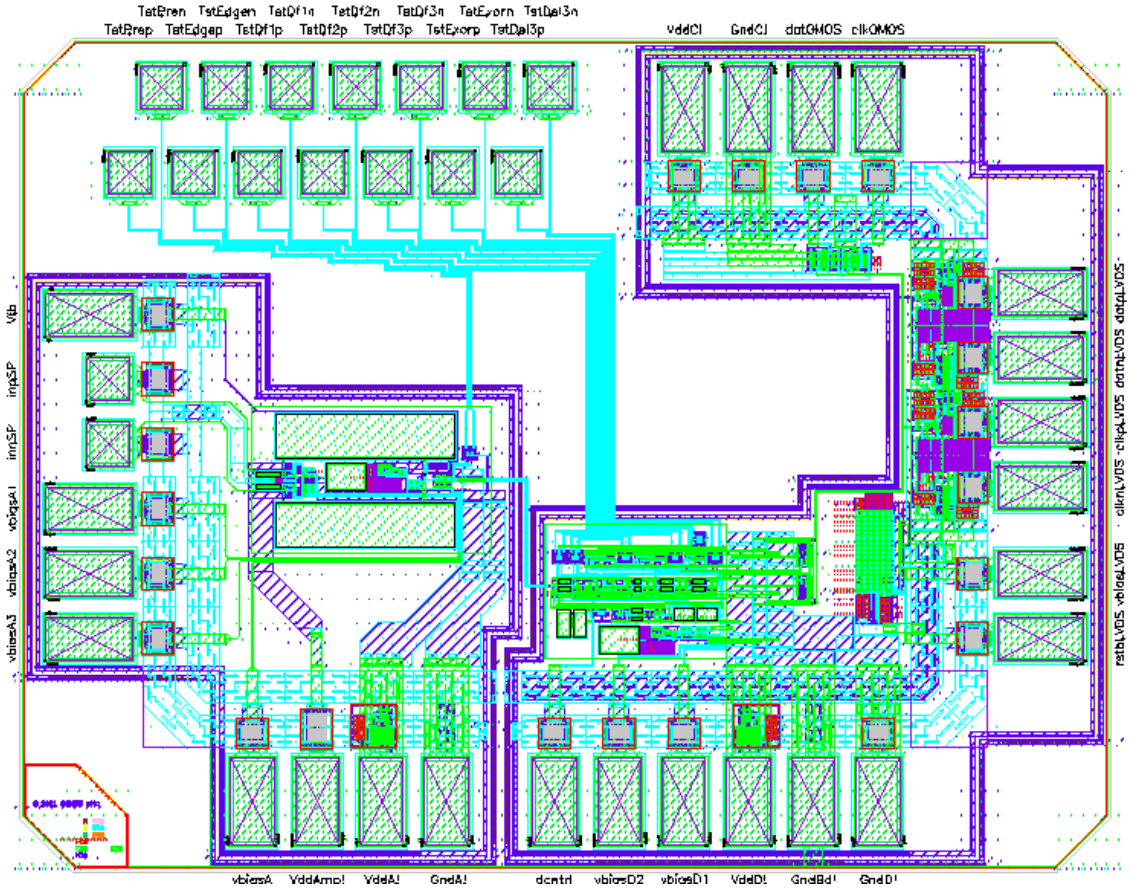
Pre-amp output

Gain Stage output

LVDS Clock & Data

- predict to decode signal correctly up to
  - ± 3σ process corners
  - ± 50 mV pre-amp offset

DORIC-I3


TstEpren TstEdgen TstQf1n TstQf2n TstQf3n TstExorn TstQal3n
TstEprep TstEdgep TstQf1p TstQf2p TstQf3p TstExorp TstQal3p
vddCl GndCl datCMOS clkCMOS
Vfb
inpSP
innSP
vbiasA3
vbiasA
VddAmpl
VddAl
GndAl
dcntrl
vbiasD2
vbiasD1
VddDl
GndBdl
GndDl

Summary

- VDC-D3/DORIC-D3 basically work!
- radiation hardness of VDC-I1/DORIC-I1 appears adequate for pixel system!
- many improvements implemented in VDC-I2/DORIC-I2
- expect VDC-I3 to consume significantly less current
- single-ended pre-amp implemented in DORIC-I3