

New Results on Opto-Electronics

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June 18, 2002

Outline

- Introduction
- VCSEL Annealing
- Plan for Opto-board IV
- Result on VDC/DORIC-I3
- Improvements in VDC/DORIC-I4
- Summary

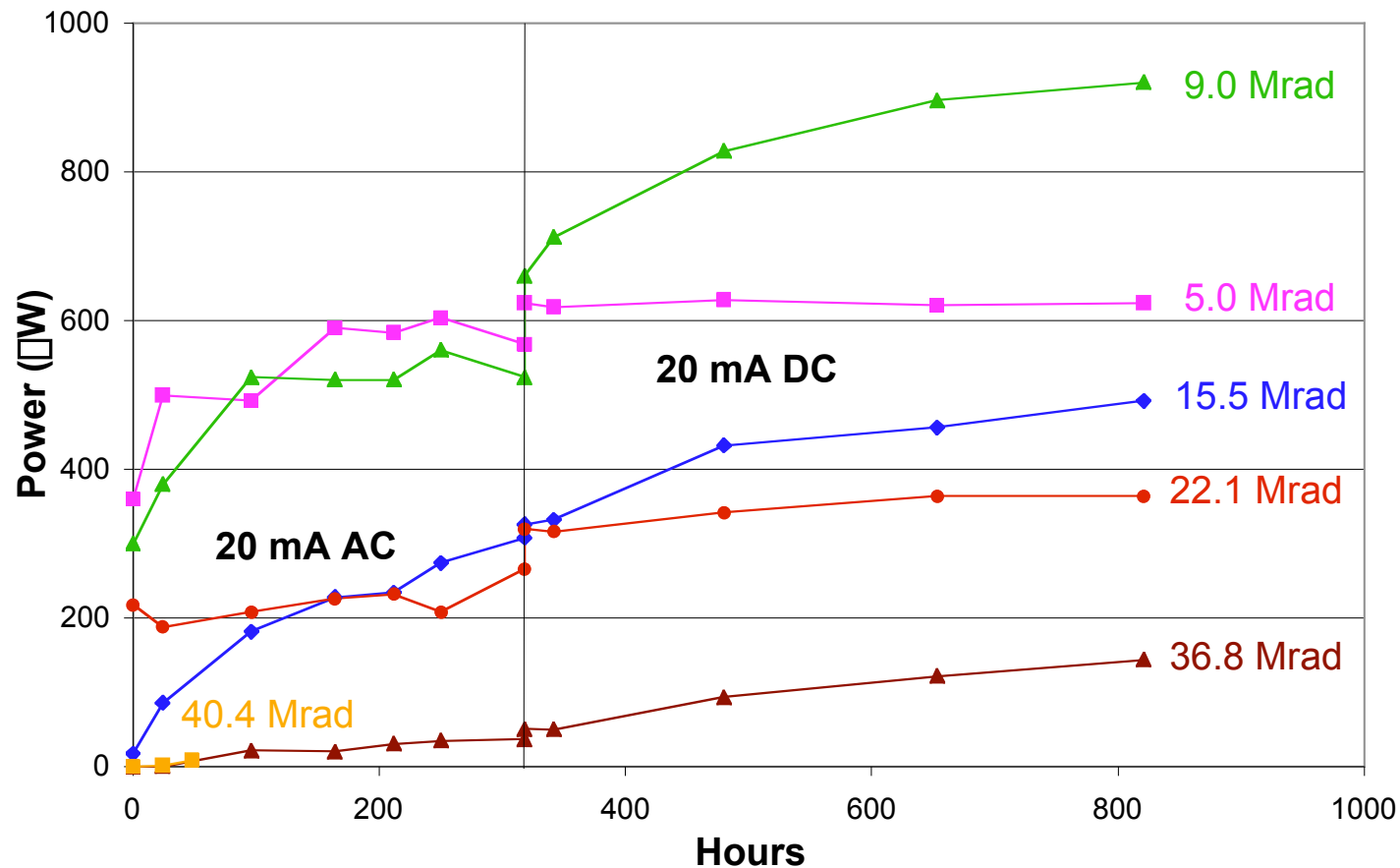
Introduction

- VCSEL Driver Chip (VDC):
 - ☆ convert LVDS signal into single-ended signal appropriate to drive VCSEL
- Digital Opto-Receiver Integrated Circuit (DORIC):
 - ☆ decode clock and command signals from PIN diode

Opto-electronics Team

- The Ohio State University:
 - ☆ Kregg Arms, K.K. Gan, Mark Johnson, Harris Kagan, Richard Kass, Chuck Rush, Rouben Ter-Antonian, Michael Zoeller
- Siegen University:
 - ☆ Adrian Niculae, Michael Kraemer, Joachim Hausmann, Martin Holder, Michal Ziolkowski

VCSEL Annealing of 20 mA AC vs DC

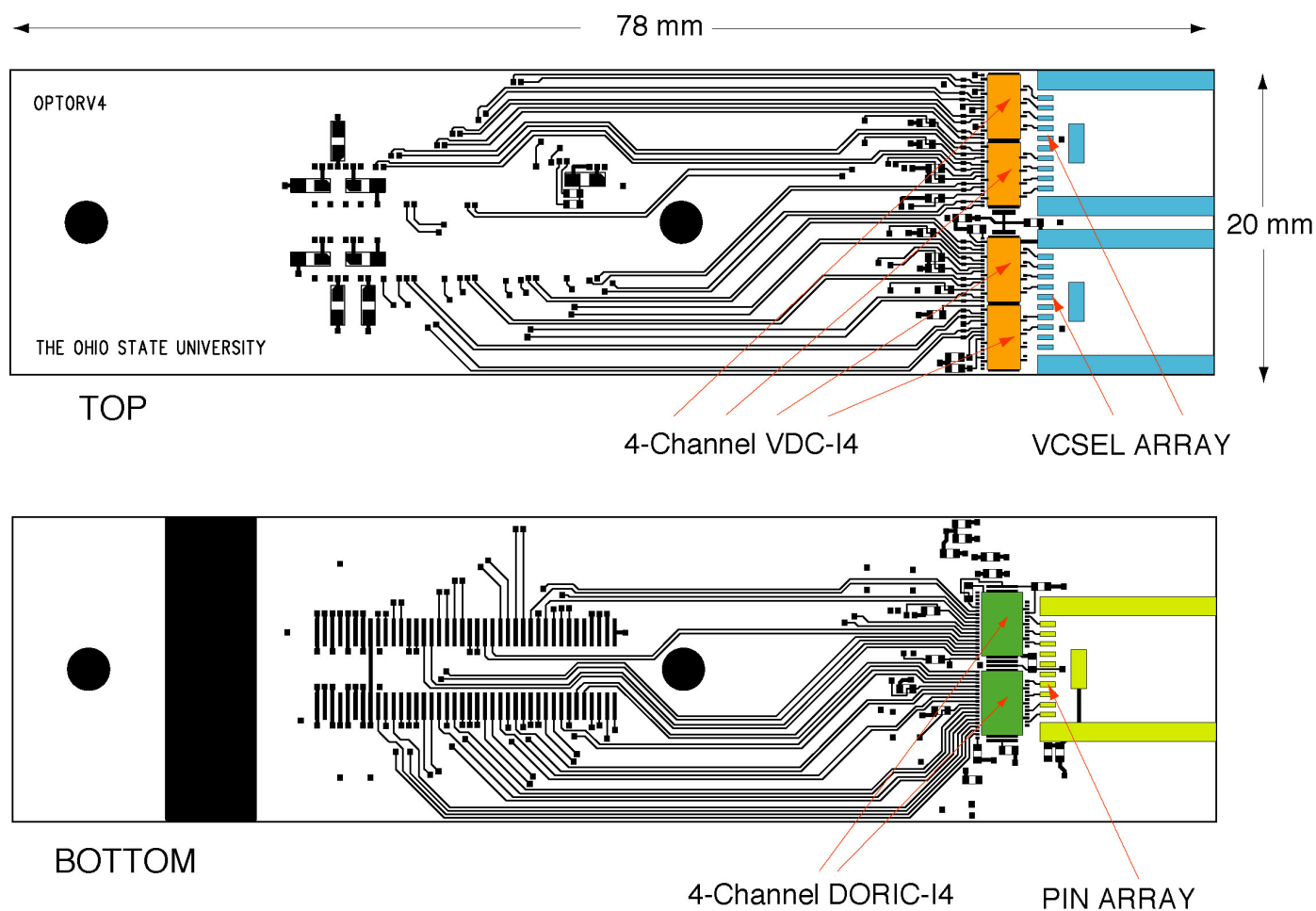


● AC and DC currents produce similar annealing

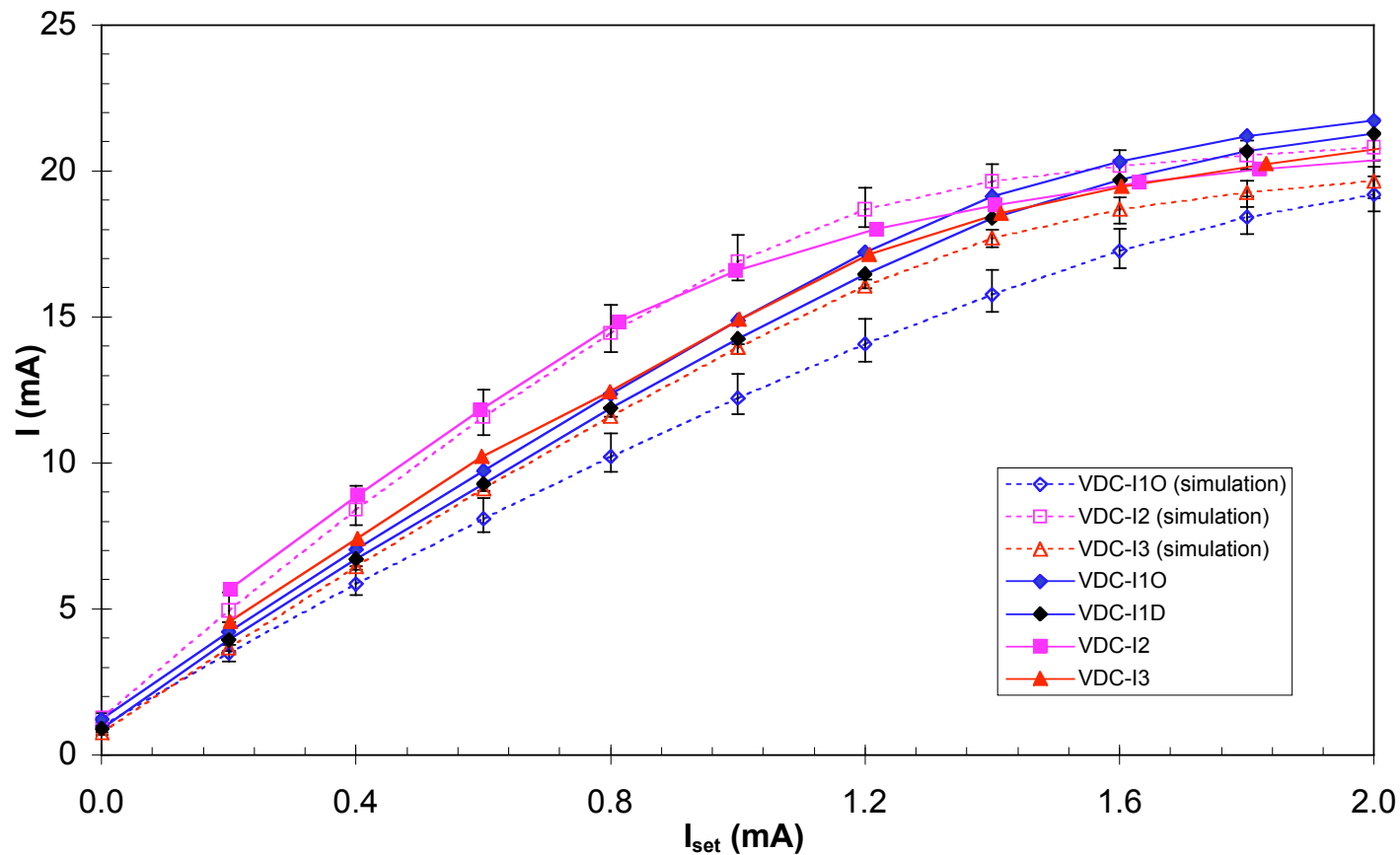
Opto-Board Prototype IV

- design for 4-channel VDC/DORIC-I4
- contain 7 opto-links for use in barrel and disk
- use 8-channel opto-packs
- use 80-pin connector
- satisfy PP0 constraints
- design for BeO but tested in FR4
 - ◆ FR4 submission next week
 - ◆ BeO submission in Fall 2002

Opto-Board Prototype IV

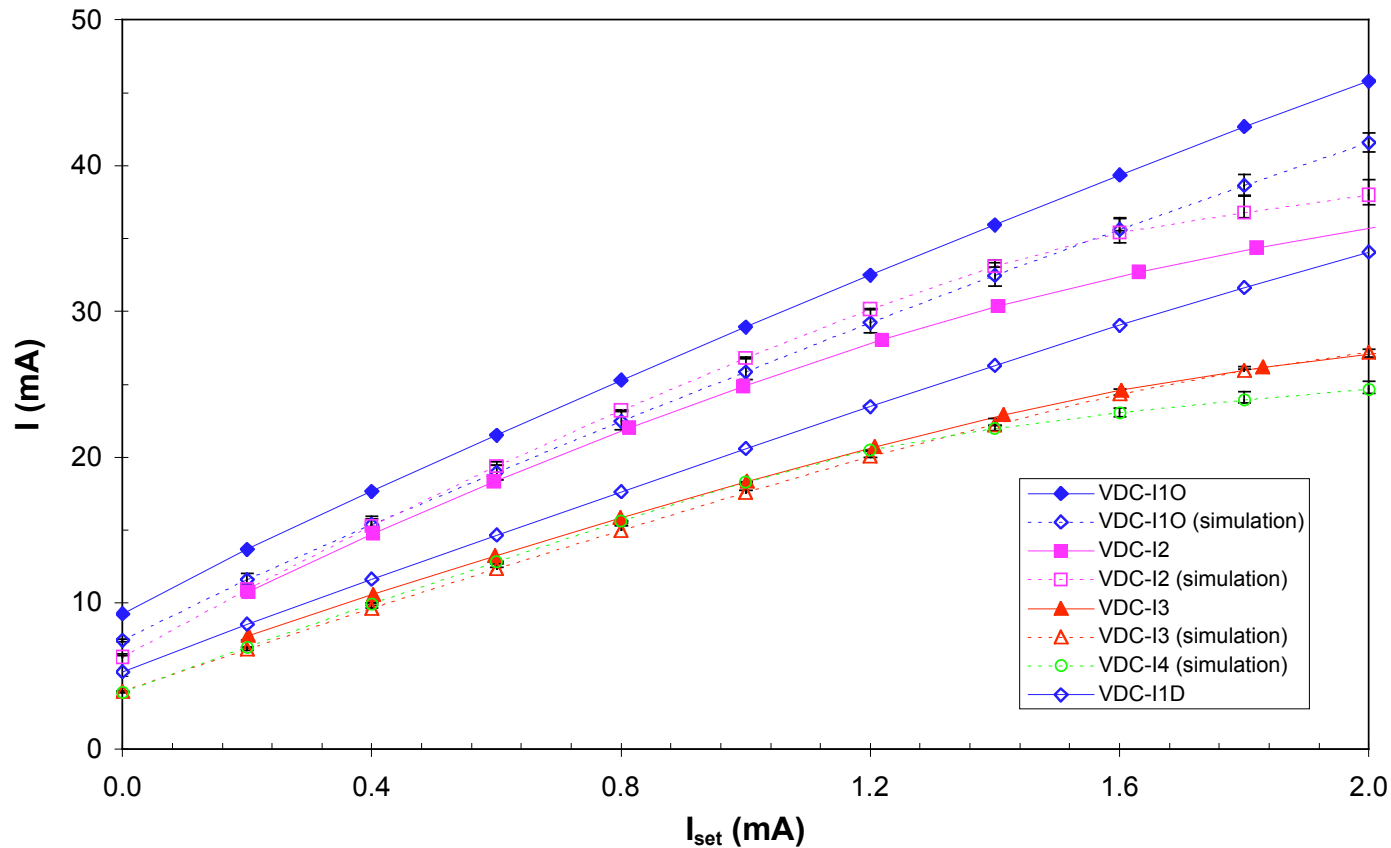


VDC-I3 Bright Currents vs I_{set}



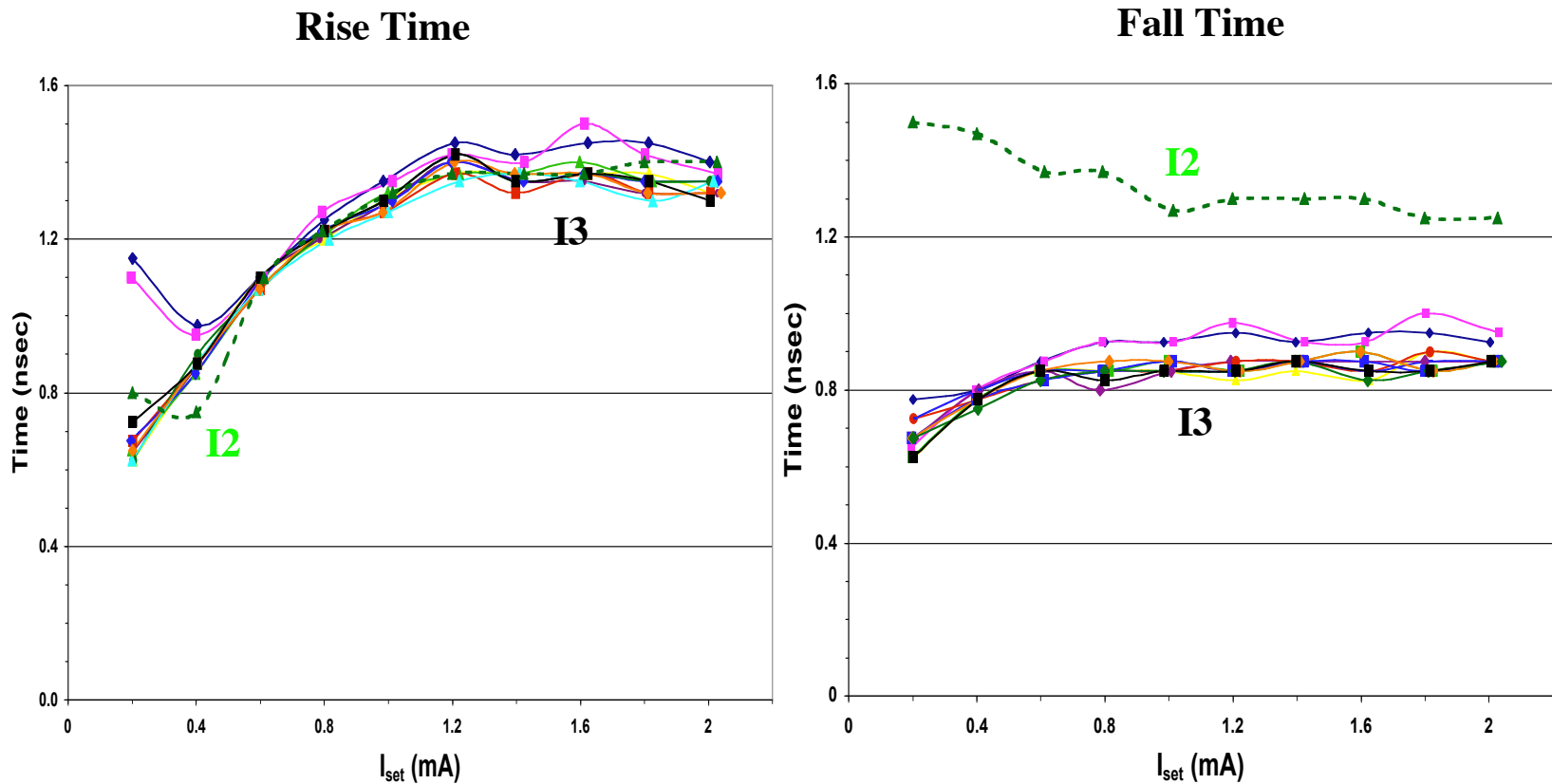
- turning over at high I_{set} is due to 10 Ω in series used in measurement
- dependence of bright current vs I_{set} is as expected

Current Consumption of VDC-I3



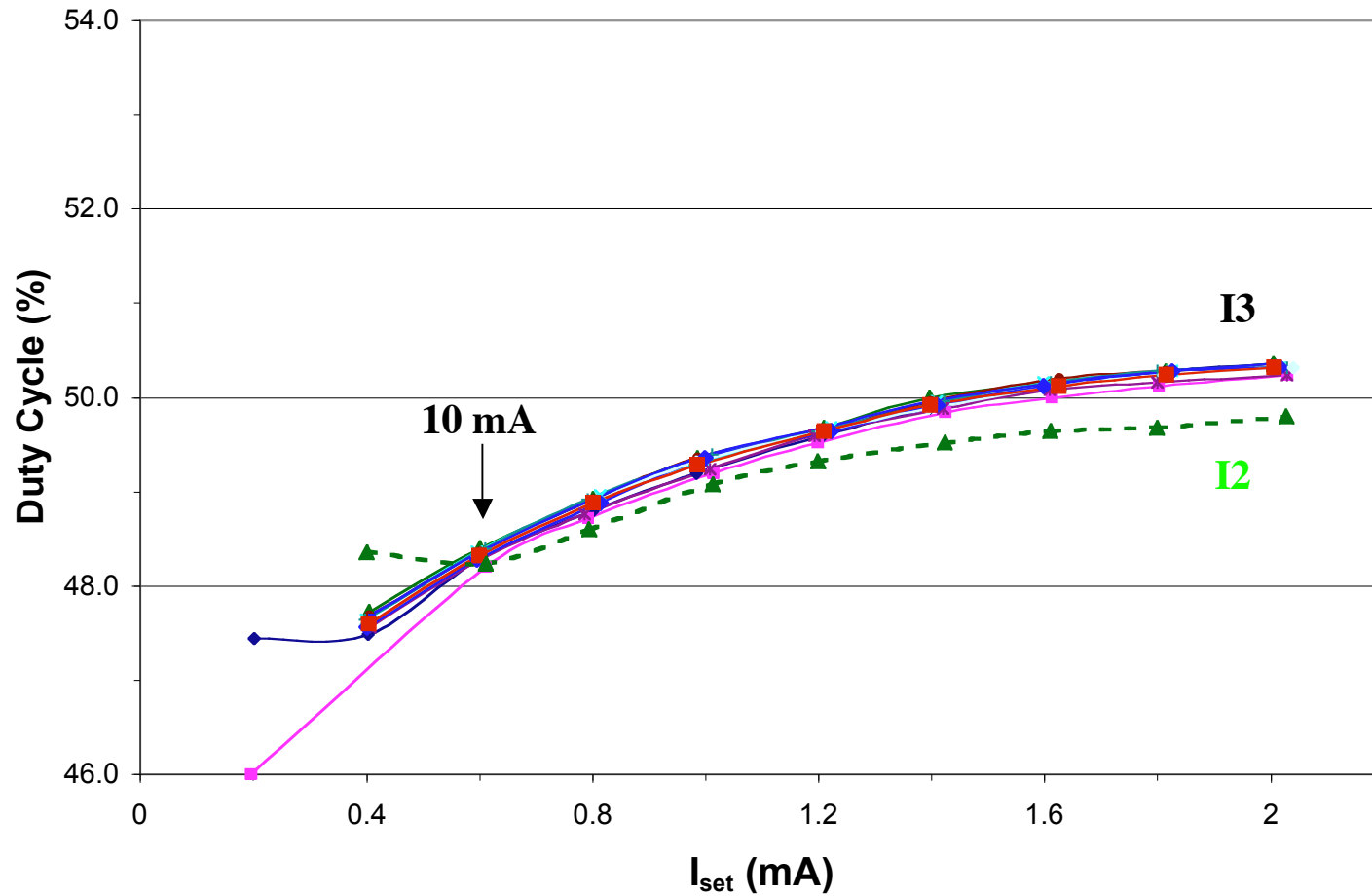
- VDC-I3 current consumption is consistent with expectation
- VDC-I3 consumes less current than VDC-I2

Rise/Fall Time vs I_{set}



- rise times somewhat above spec. (1 ns)
- fall times is better than VDC-I2

Clock Duty Cycle vs I_{set}

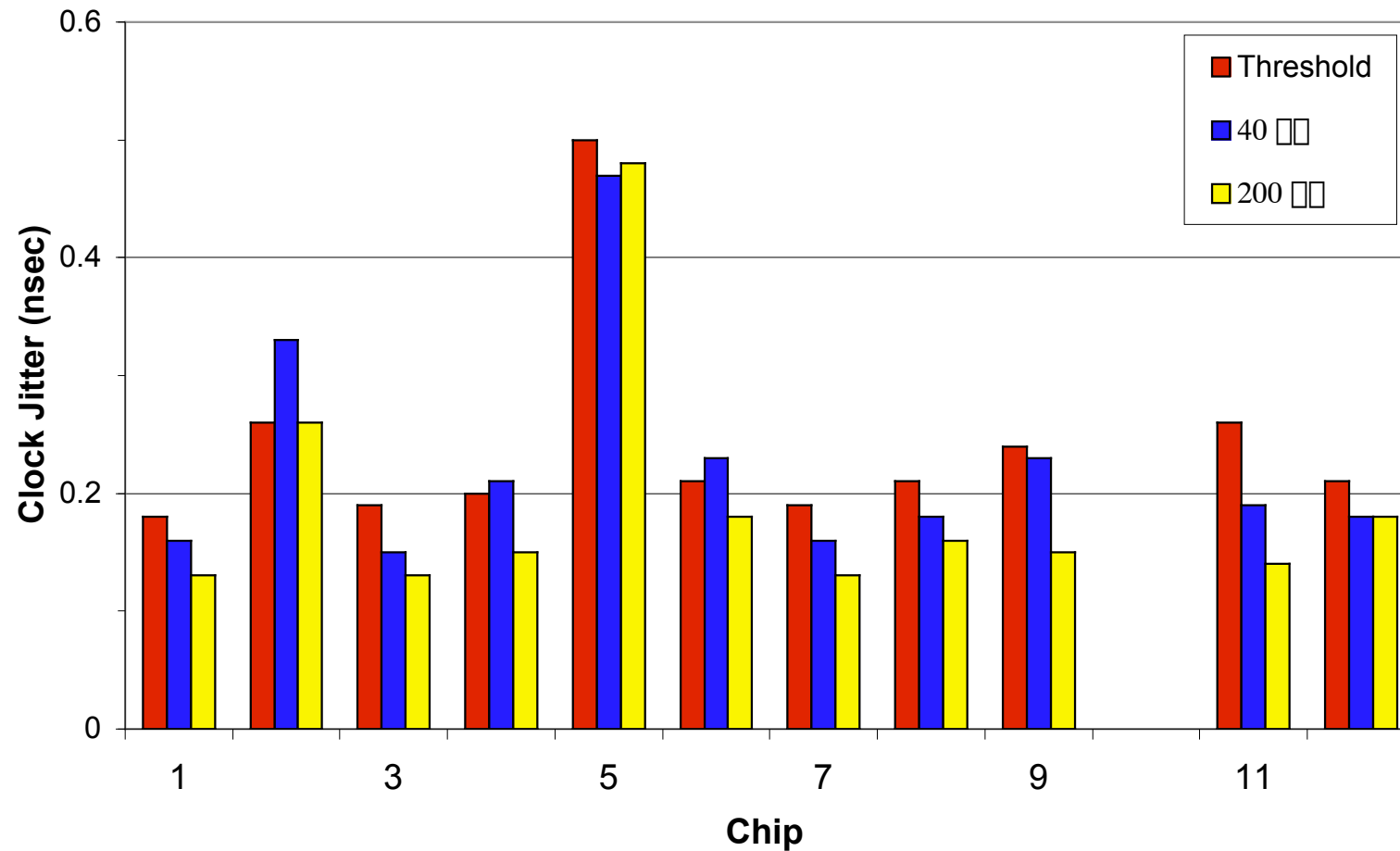


● clock duty cycle closer to 50% than VDC-I2

DORIC-I3

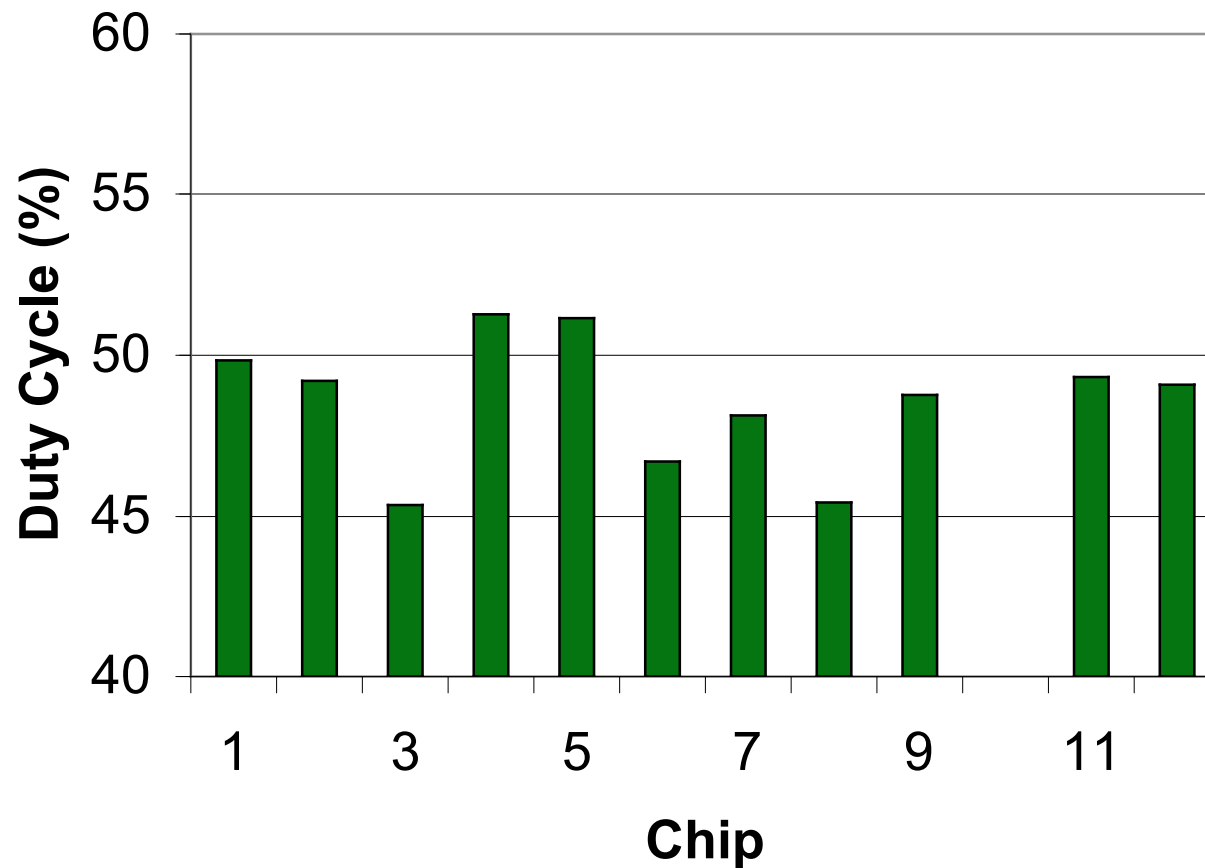
- first implementation of single-ended pre-amp
 - ☞ PIN bias voltage (up to 10 V) moved off die
- PIN current threshold for no bit errors are low:
 - ◆ 10-29 μ A for 7 links on opto-board with SCT opto-packs
 - ◆ 16-17 μ A for 4 links on opto-board with PIN array opto-packs
 - ◆ no need to bond the dummy channel in pre-amp for noise cancellation
 - ★ confirmed with HSPICE simulations

Jitter of Recovered Clock in DORIC-I3



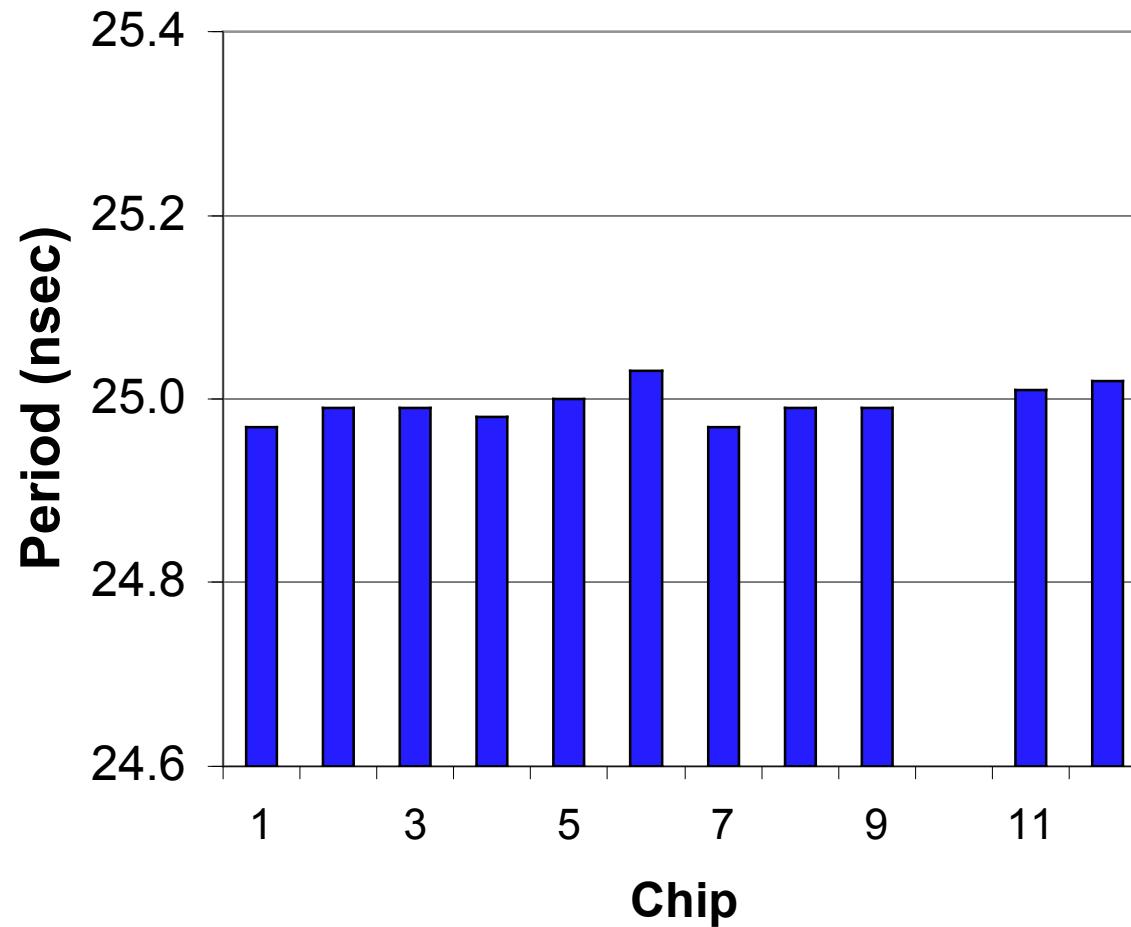
- clock jitter is typically ~ 150 ps
- clock jitter decreases with higher PIN current

Duty Cycle of Recovered Clock in DORIC-I3



● duty cycle is close to 50%

Period of Recovered Clock in DORIC-I3

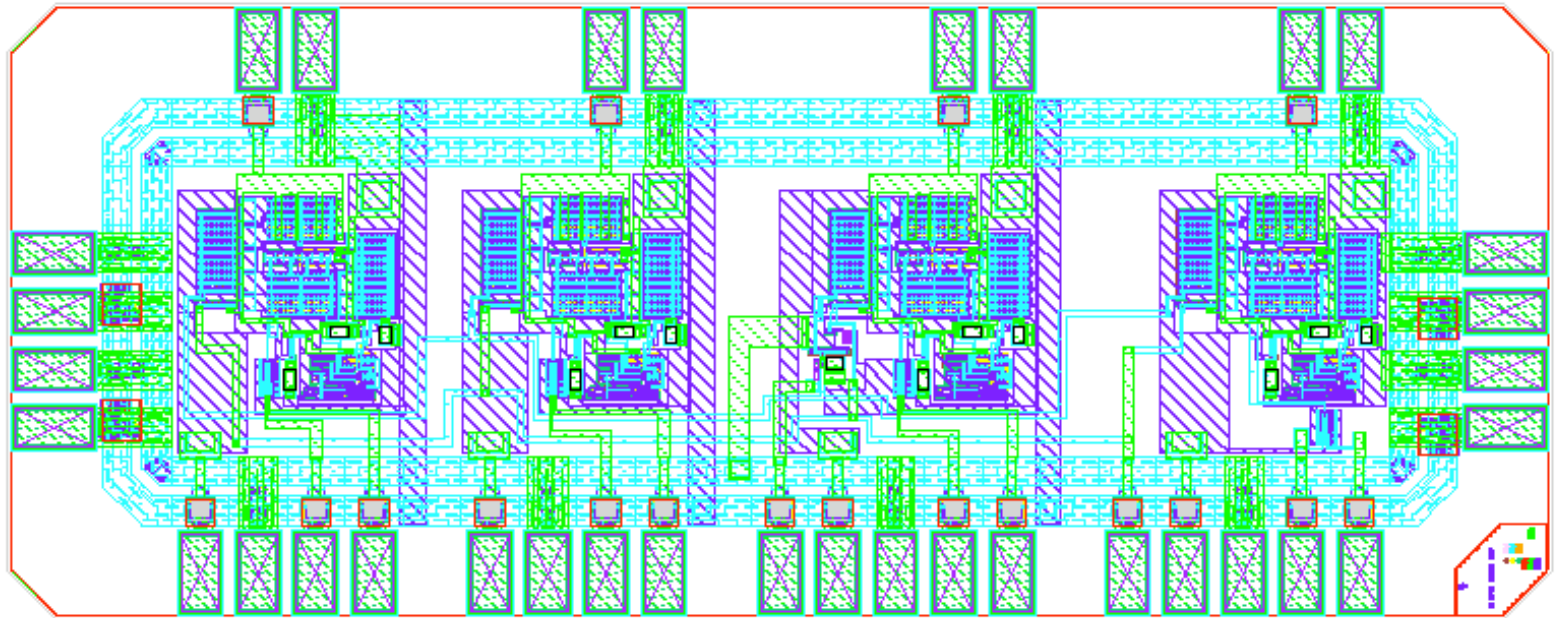


● clock period is very close to 25 ns

Status of VDC-I4

- first implementation for use with common cathode VCSEL array
- implemented all improvements presented at February Pixel Week
 - ◆ oversight in implementing faster rise/fall time
 - ☞ maximum bright current is 18 mA instead of 22 mA
 - ☞ to be fixed in next submission with larger transistors
- submitted both single and four channels as MPW run in April
 - ◆ VDC/DORIC-I2: no increase in PIN current threshold for no bit errors when all four VDC channels are running
- expect dice delivery near end of June

Four-Channel VDC-I4

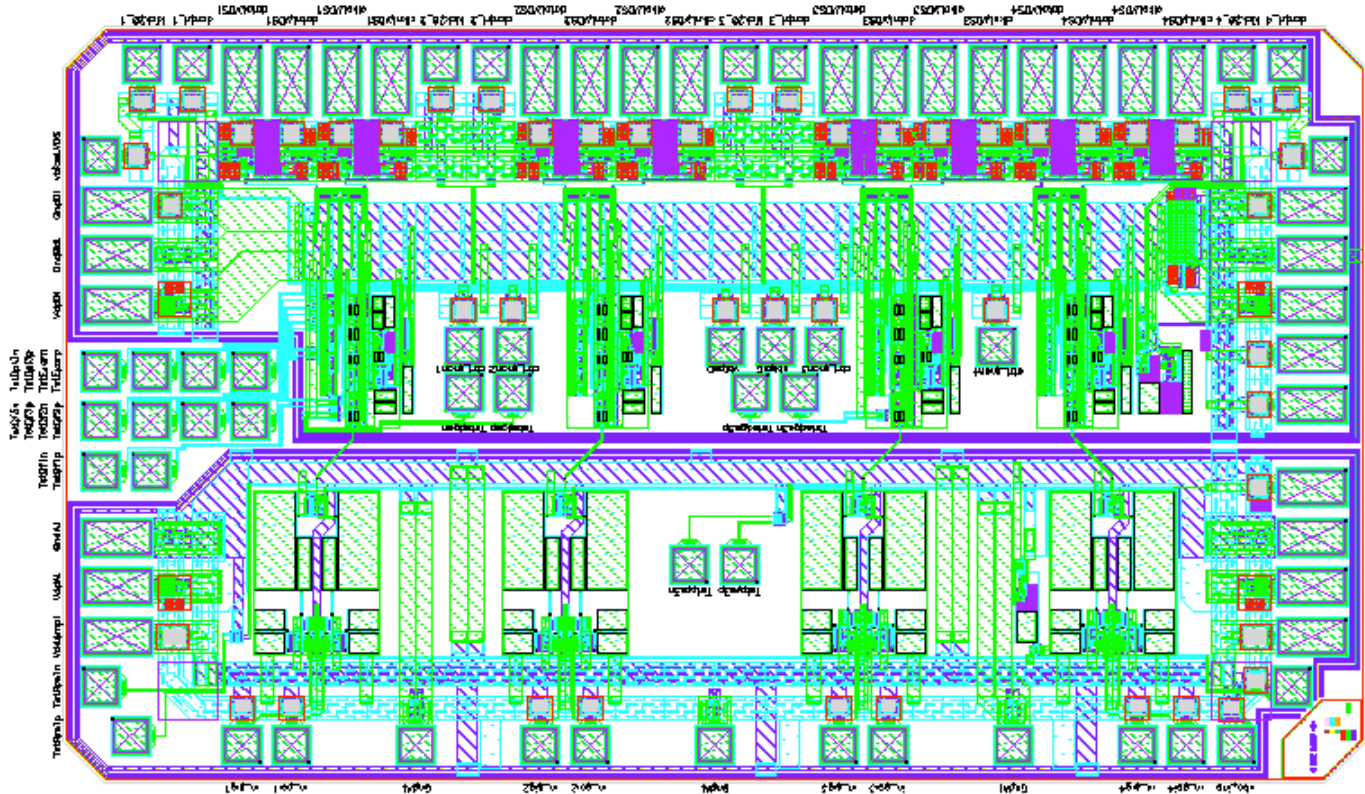


- each channel individually powered

Status of DORIC-I4

- first implementation for use with common anode PIN array
- implemented the large number of improvements presented at February Pixel Week
- first implementation of four-channel DORIC
- submitted both single and four channels as MPW run in April
- expect dice delivery near end of June

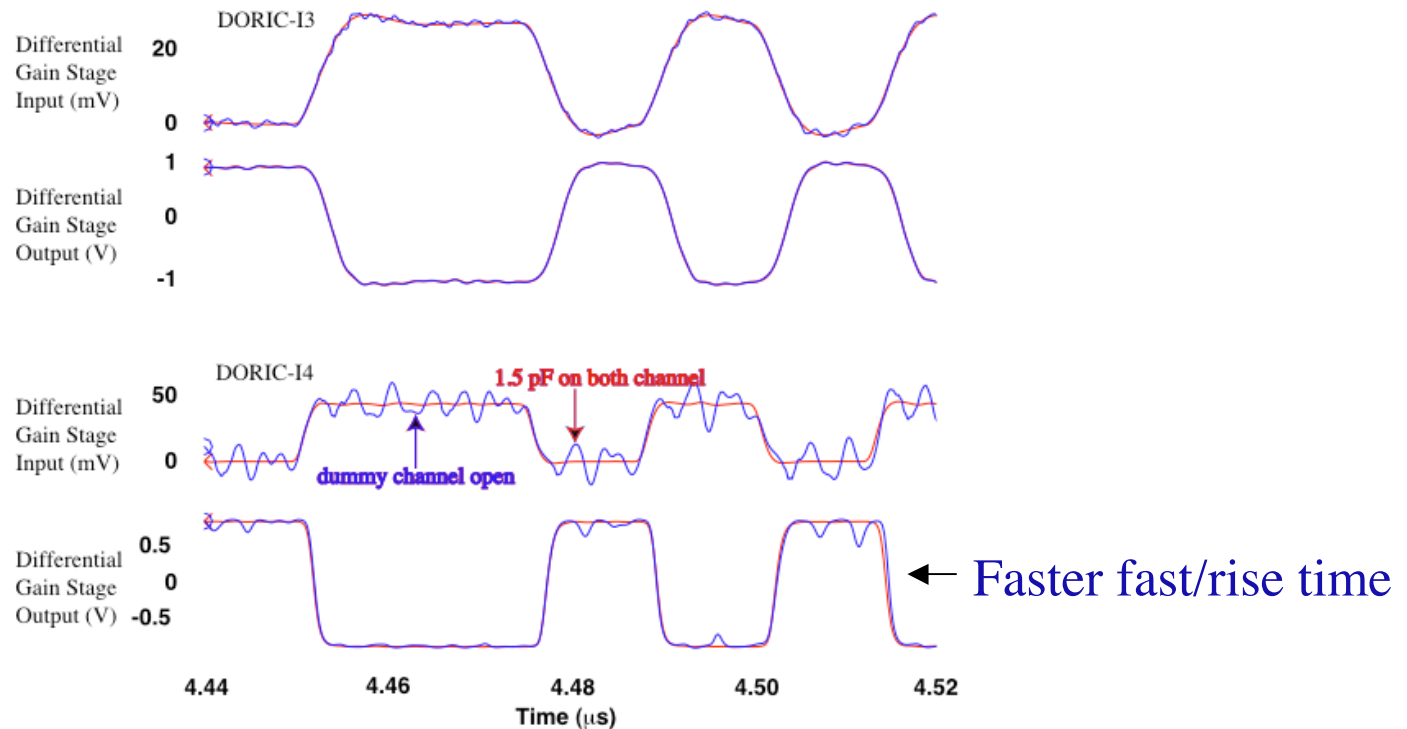
Four-Channel DORIC-I4



- all channels powered from single power supply
 - ◆ implement separate power for each channel in next submission?
- one channel contains spy circuits for probing

Open Dummy Channel in DORIC-I4?

- DORIC-I1/I2: differential pre-amp
- DORIC-I3/I4: single-ended pre-amp
 - 👉 add dummy channel before differential gain stage for noise cancellation



- DORIC-I3: dummy channel is open
 - 👉 no difference in PIN current threshold for no bit errors
- DORIC-I4: may need to bond to dummy trace to pick up stray capacitance

Summary

- AC and DC currents produce similar VCSEL annealing
- performance of VDC/DORIC-I3 is satisfactory
 - ◆ principle of single-ended pre-amp demonstrated
- VDC-I4 for common-cathode VCSEL array designed/submitted
- DORIC-I4 for common-anode PIN array designed/submitted