New Results on Opto-Electronics

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Outline

- Results on DORIC-I4
- Result on VCSEL Annealing
- Test with PP0 cable
- Light Budget
- Status of VDC/DORIC-I5
- Summary

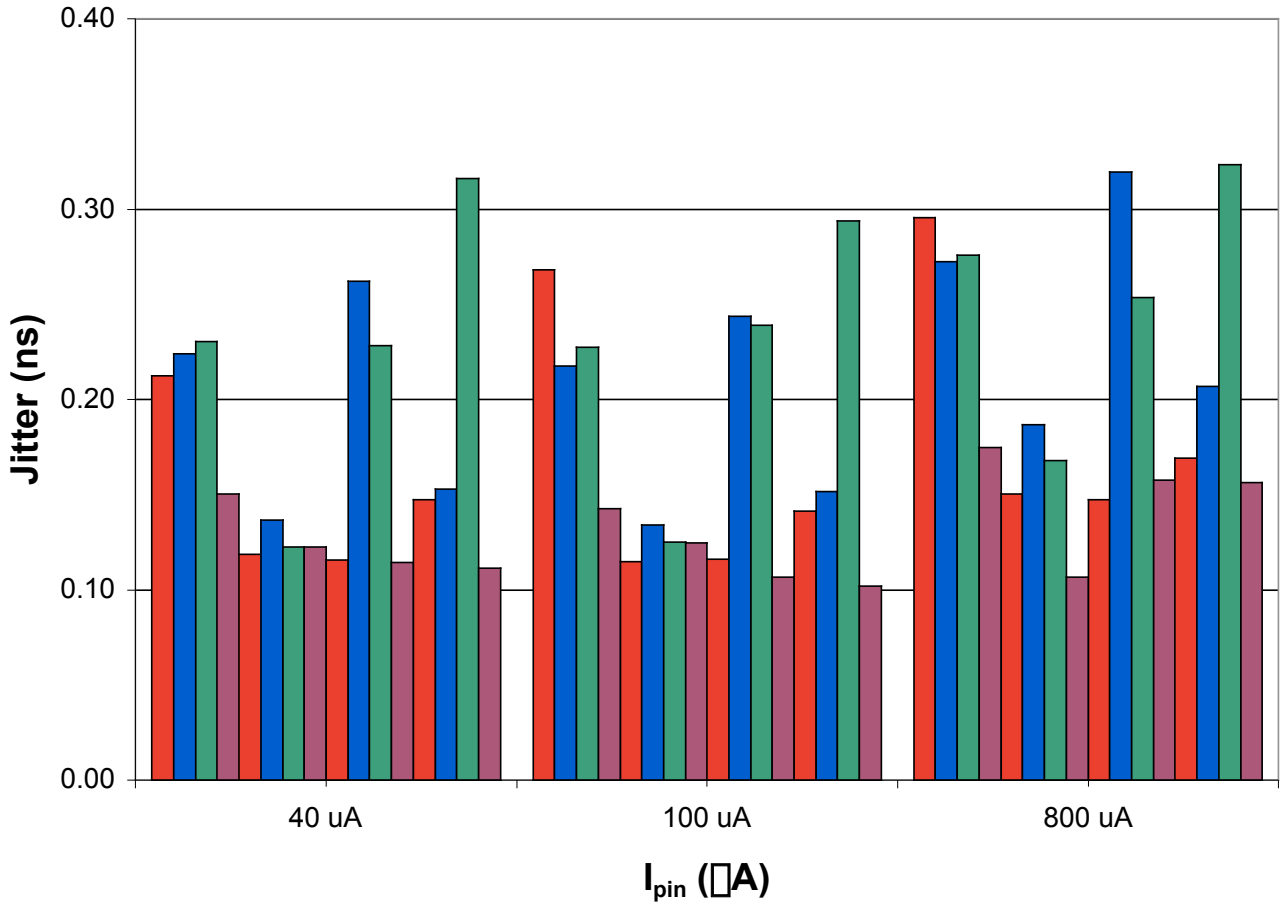
Opto-electronics Team

- The Ohio State University:
  - Kregg Arms, K.K. Gan, Mark Johnson, Harris Kagan, Richard Kass, Chuck Rush, Rouben Ter-Antonian, Michael Zoeller
- Siegen University:
  - Alex Ciliox, Martin Holder, Michal Ziolkowski

Results on DORIC-I4

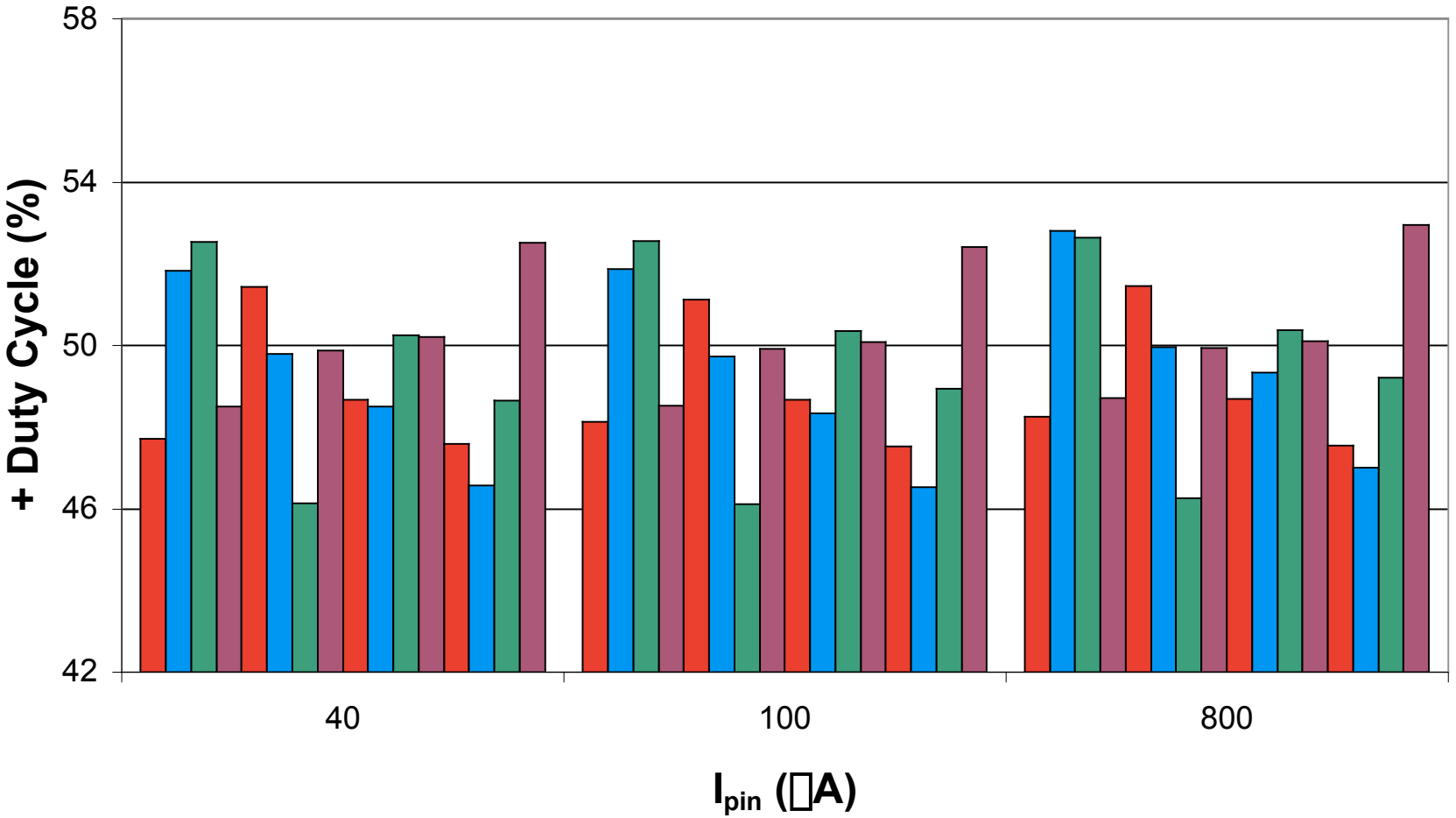
- measured 16 channels (4 chips):
  - current consumption
  - PIN current threshold
  - data and clock LVDS levels
  - data and clock rise/fall time
  - clock jitter/duty cycle vs PIN currents
  - delay between clock and data
  - ⇨ all characteristics are similar and within specs

Jitter of Recovered Clock in DORIC-I4



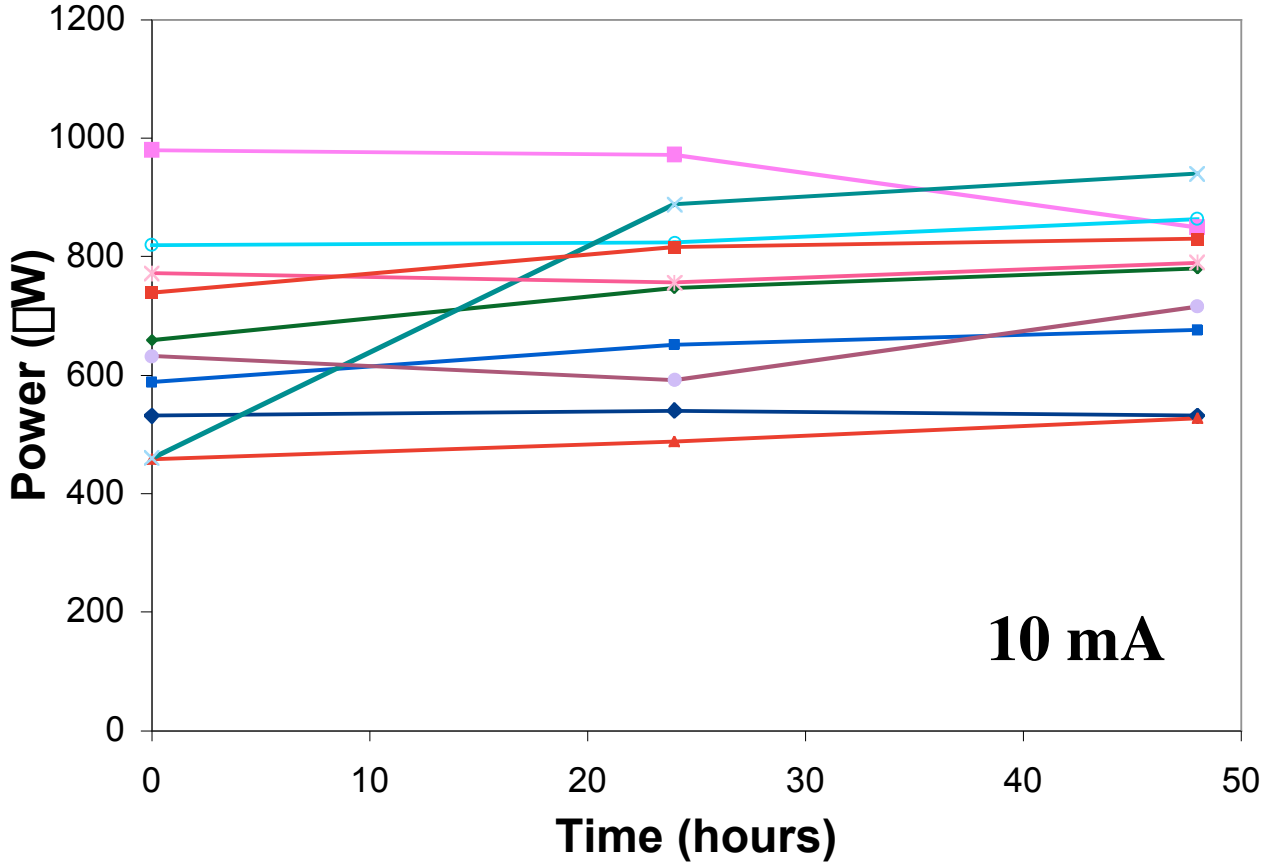
- jitter is small

Duty Cycle of Recovered Clock in DORIC-I4



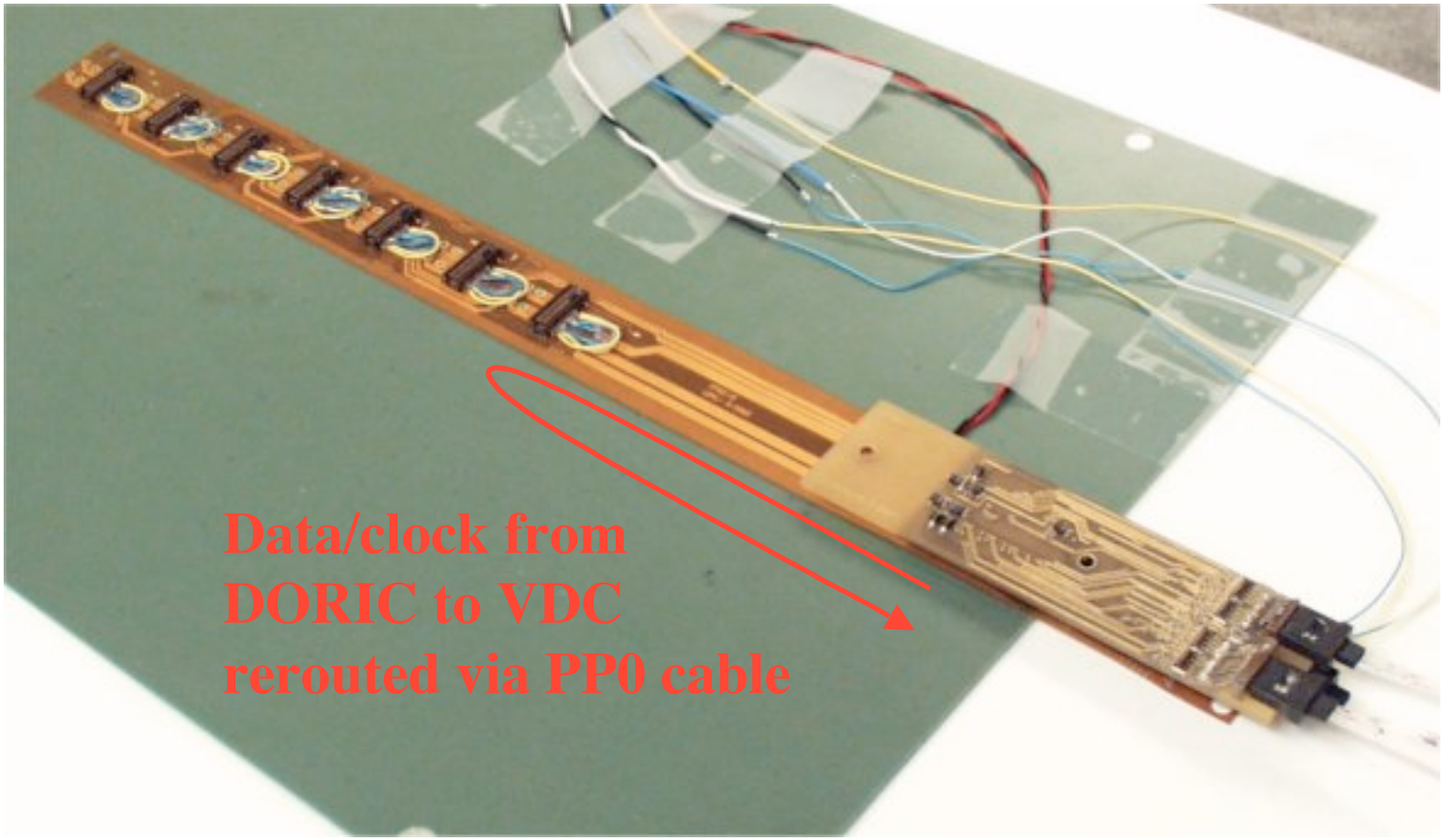
- duty cycle is within spec

Optical Power of Irradiated Opto-boards after Annealing

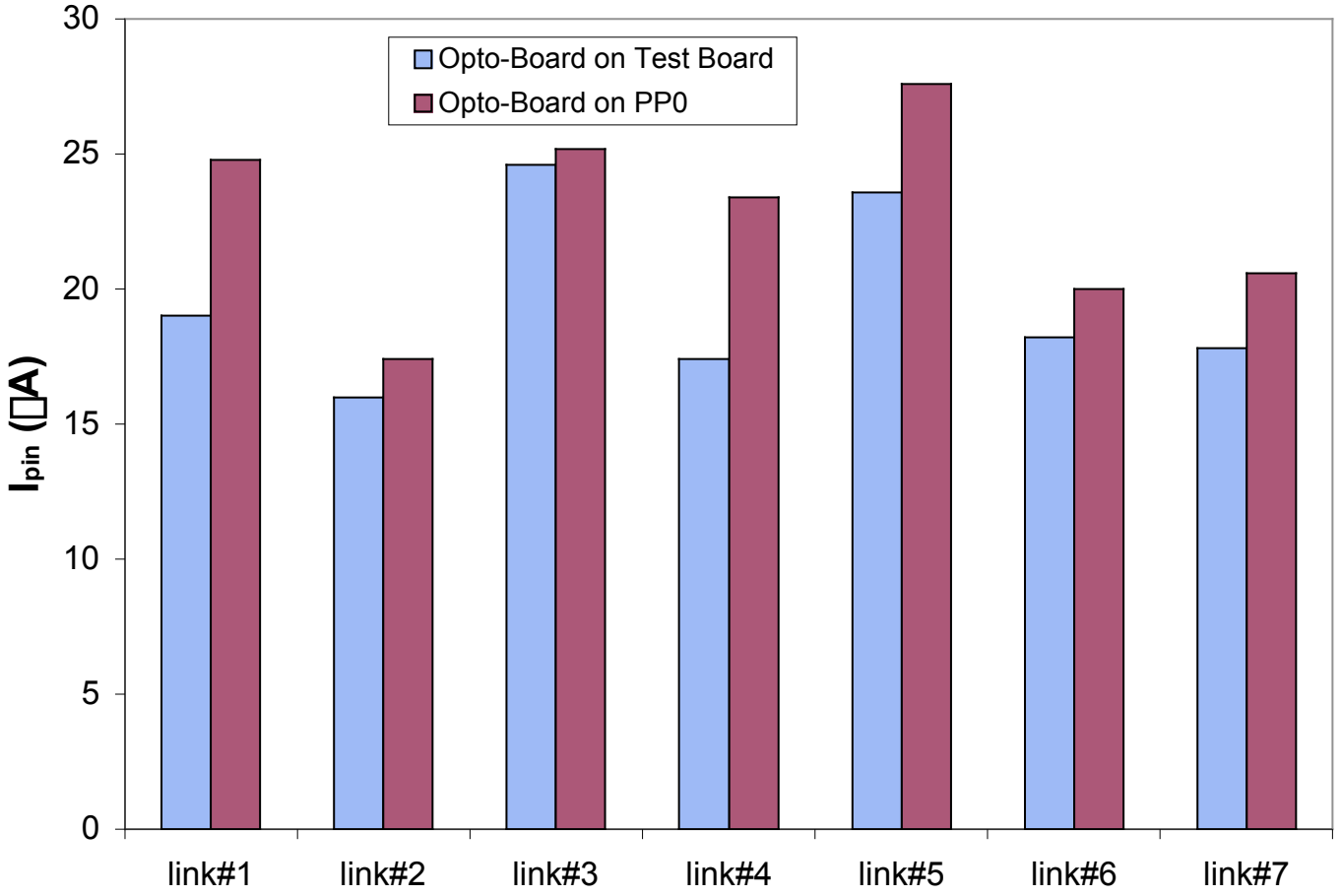


- all links have good optical power before annealing
- ⇨ only one link shows improvement after annealing
- limited annealing program in Aug ’02 irradiation is reasonable

PP0 Cable with Opto-Board

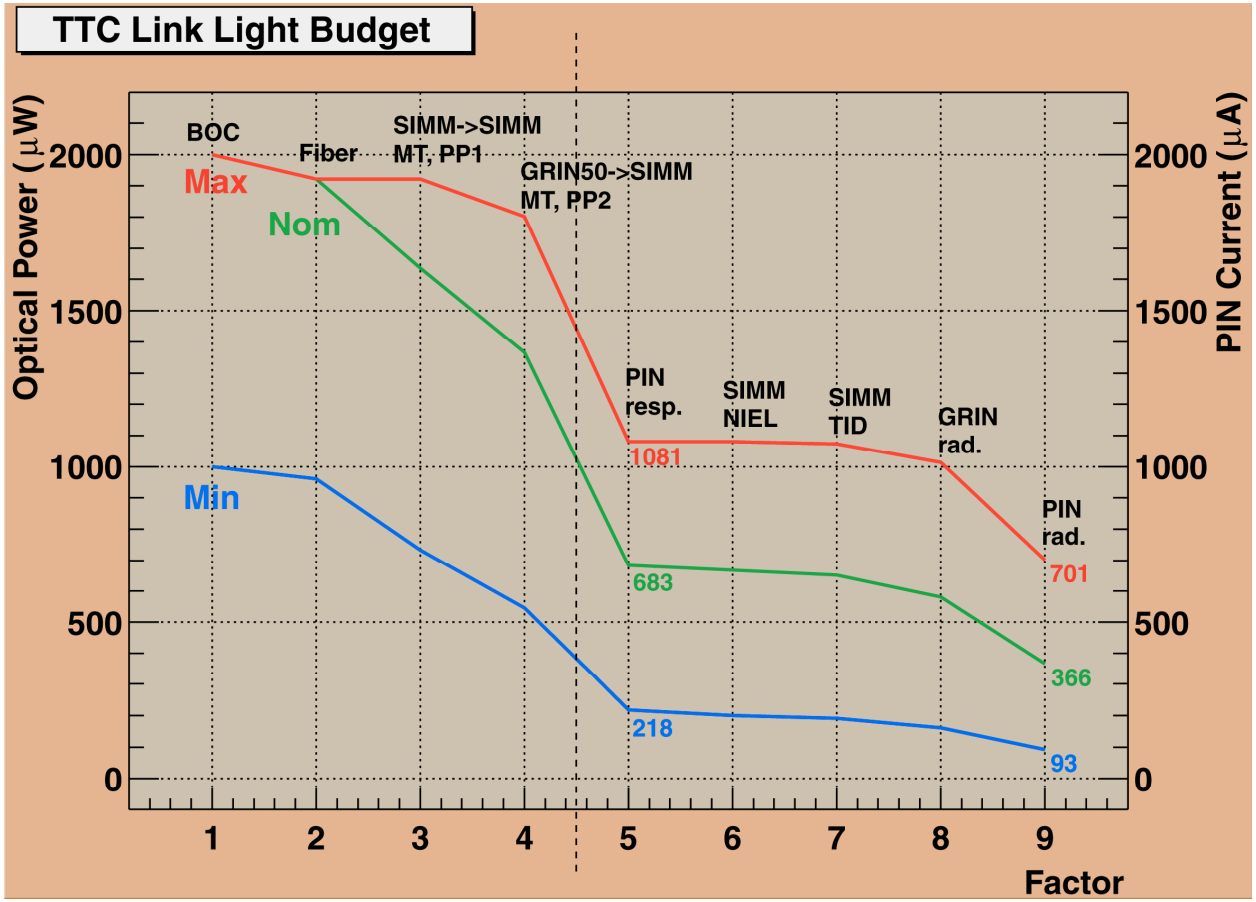


Pin Current Thresholds with PP0 Cable



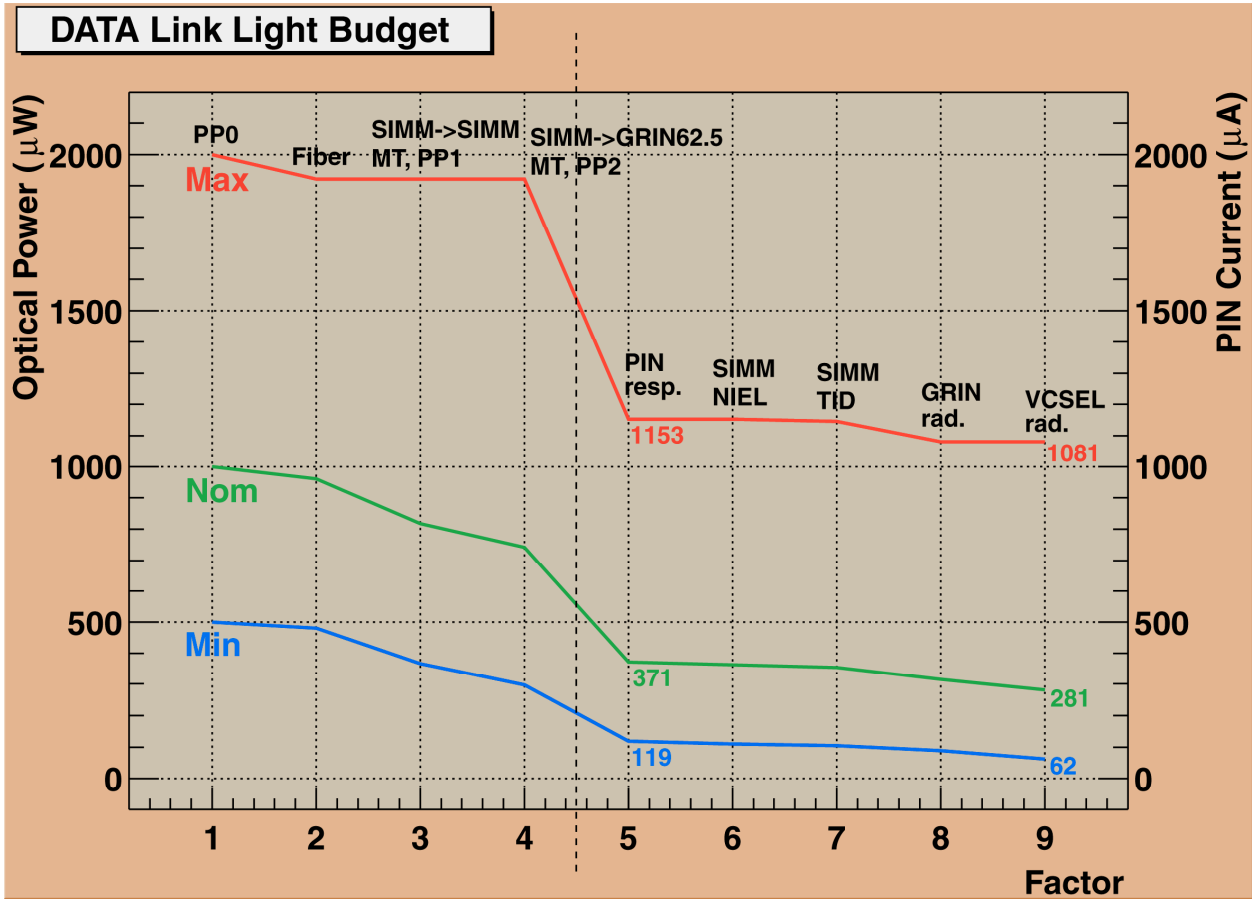
- PIN current thresholds measured with other links running at 40 □A
- small increase in thresholds?

TTC Link Light Budget



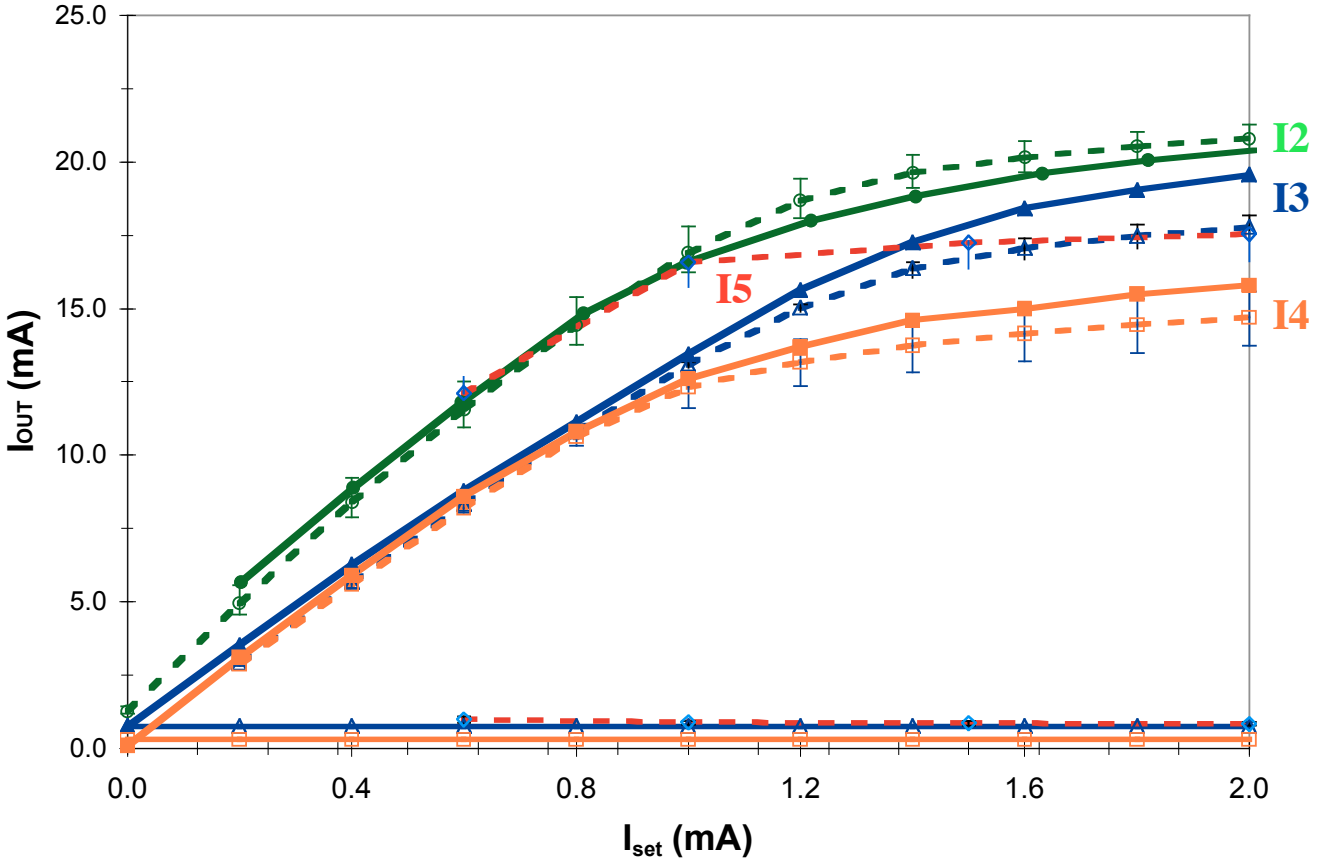
- PIN current at opto-board after radiation: 93-701 □A

Data Link Light Budget



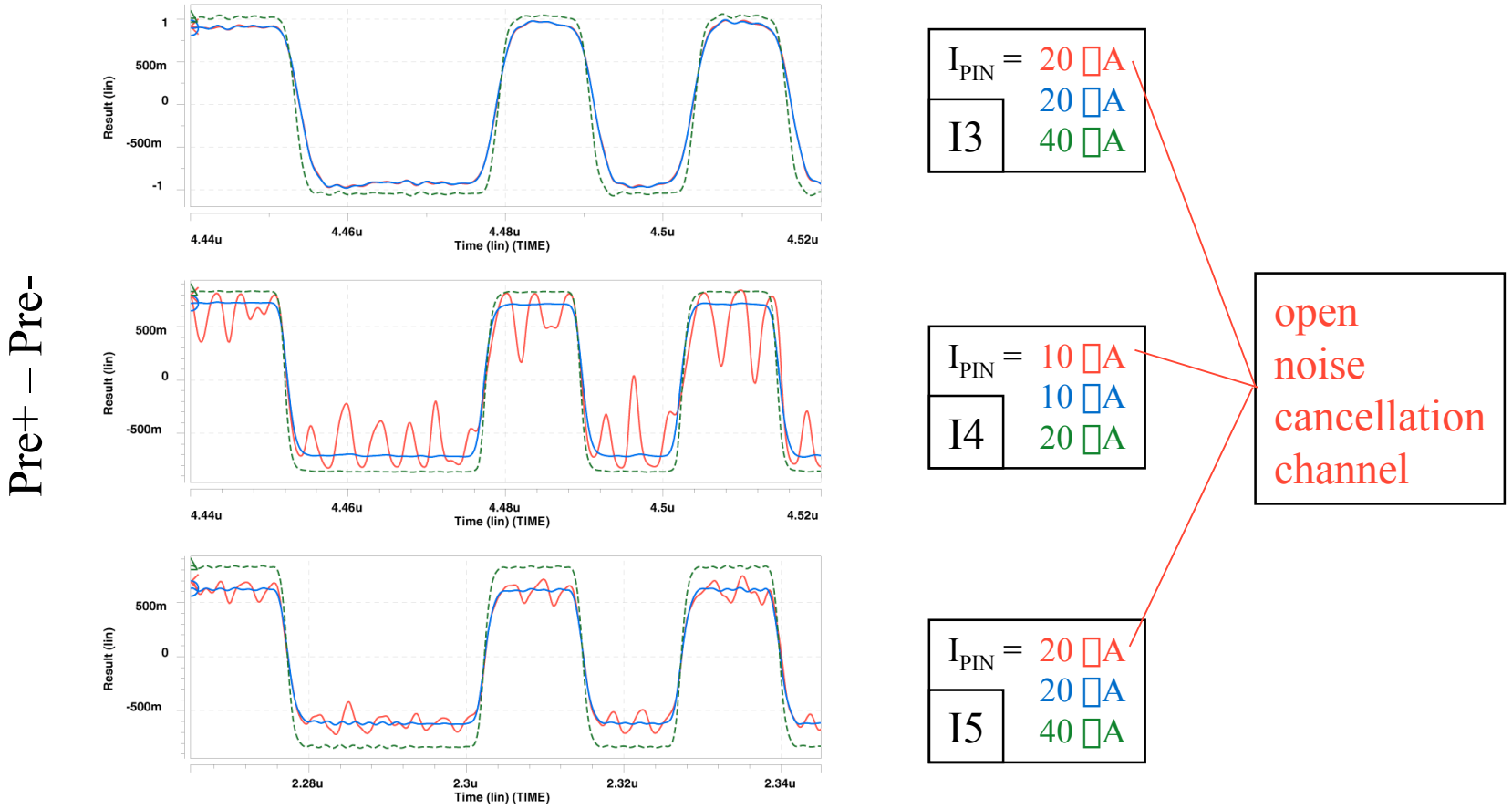
- PIN current at BOC after radiation: 62-1081 □A

VDC-I5: VCSEL Drive Currents vs I_{set}



- VDC-I5 is predicted to produce more currents
- turning over at high I_{set} is due to 10 Ω in series used in measurement
- VDC-I5 has maximum current of 22 mA without 10 Ω

Matching of Input Strays in DORIC-I3/I4/I5



- DORIC-I5 should be less sensitive to matching of stray capacitance than DORIC-I4

Status of VDC/DORIC-I5

- implemented all improvements presented at October Pixel week
  - simulations from layout with extracted stray capacitances predict proper working chips at all three corner transistor parameters except DORIC clock duty cycle :
    - spec: (50 ± 4)%
    - DORIC-I5: 54.8% at -3 transistor parameters
- submitted last week as 3-metal MPW run
- expected chip delivery in late February or early March
- participate in 5-metal engineering run with MCC in late February or early March

Summary

- irradiated VCSELs have good optical power
- small increase in PIN current thresholds for no bit errors with PP0 cable?
- large margin of light in opto-link
- VDC/DORIC-I5 submitted for MPW run