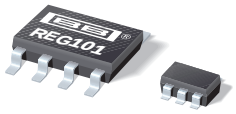


SBVS026C – JULY 2001

DMOS
100mA Low-Dropout Regulator

FEATURES

- **NEW DMOS TOPOLOGY:**
  Ultra Low Dropout Voltage:
  60mV typ at 100mA
  Output capacitor NOT required for stability
- **FAST TRANSIENT RESPONSE**
- **VERY LOW NOISE: 23μVrms**
- **HIGH ACCURACY: ±1.5% max**
- **HIGH EFFICIENCY:**
  I_{GND} = 500μA at I_{OUT} = 100mA
  Not Enabled: I_{GND} = 10nA
- **2.5V, 2.8V, 2.85V, 3.0V, 3.3V, 5.0V, AND ADJUSTABLE OUTPUT VERSIONS**
- **OTHER OUTPUT VOLTAGES AVAILABLE UPON REQUEST**
- **FOLDBACK CURRENT LIMIT**
- **THERMAL PROTECTION**
- **SMALL SURFACE-MOUNT PACKAGES:**
  SOT23-5 and SO-8

APPLICATIONS

- **PORTABLE COMMUNICATION DEVICES**
- **BATTERY-POWERED EQUIPMENT**
- **PERSONAL DIGITAL ASSISTANTS**
- **MODEMS**
- **BAR-CODE SCANNERS**
- **BACKUP POWER SUPPLIES**

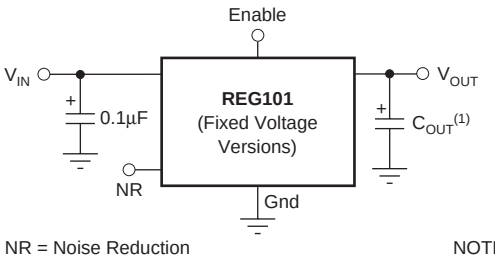
DESCRIPTION

The REG101 is a family of low-noise, low-dropout linear regulators with low ground pin current. Its new DMOS topology provides significant improvement over previous designs, including low dropout voltage (only 60mV typ at full load), and better transient performance. In addition, no output capacitor is required for stability, unlike conventional low-dropout regulators that are difficult to compensate and require expensive low ESR capacitors greater than 1μF.

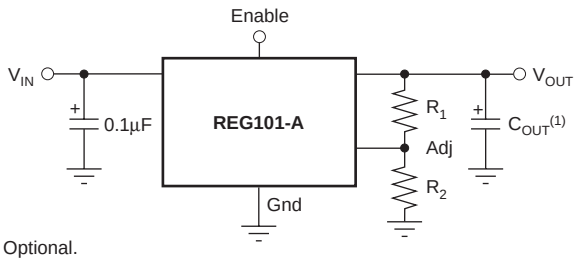
Typical ground pin current is only 500μA (at I_{OUT} = 100mA) and drops to 10nA when not in enabled mode. Unlike regulators with PNP pass devices, quiescent current remains relatively constant over load variation and under dropout conditions.

The REG101 has very low output noise (typically 23μVrms for V_{OUT} = 3.3V with C_{NR} = 0.01μF), making it ideal for use in portable communications equipment. Accuracy is maintained over temperature, line, and load variations. Key parameters are tested over the specified temperature range (–40°C to +85°C).

The REG101 is well protected—internal circuitry provides a current limit that protects the load from damage. Thermal protection circuitry keeps the chip from being damaged by excessive temperature. The REG101 is available in the SOT23-5 and the SO-8 packages.



NR = Noise Reduction



NOTE: (1) Optional.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Input Voltage, V_{IN}	–0.3V to 12V
Enable Input	–0.3V to V_{IN}
Output Short-Circuit Duration	Indefinite
Operating Temperature Range (T_J)	–55°C to +125°C
Storage Temperature Range (T_A)	–65°C to +150°C
Lead Temperature (soldering, 3s, SOT23-5, and SO-8)	+240°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	PACKAGE MARKING	ORDERING NUMBER[1]	TRANSPORT MEDIA
5V Output					
REG101NA-5	SOT23-5	331	R01B	REG101NA-5/250	Tape and Reel
"	"	"	"	REG101NA-5/3K	Tape and Reel
REG101UA-5	SO-8	182	REG101U50	REG101UA-5	Rails
"	"	"	"	REG101UA-5/2K5	Tape and Reel
3.3V Output					
REG101NA-3.3	SOT23-5	331	R01C	REG101NA-3.3/250	Tape and Reel
"	"	"	"	REG101NA-3.3/3K	Tape and Reel
REG101UA-3.3	SO-8	182	REG101U33	REG101UA-3.3	Rails
"	"	"	"	REG101UA-3.3/2K5	Tape and Reel
3V Output					
REG101NA-3	SOT23-5	331	R01D	REG101NA-3/250	Tape and Reel
"	"	"	"	REG101NA-3/3K	Tape and Reel
REG101UA-3	SO-8	182	REG101U30	REG101UA-3	Rails
"	"	"	"	REG101UA-3/2K5	Tape and Reel
2.85V Output					
REG101NA-2.85	SOT23-5	331	R01N	REG101NA-2.85/250	Tape and Reel
"	"	"	"	REG101NA-2.85/3K	Tape and Reel
REG101UA-2.85	SO-8	182	REG101285	REG101UA-2.85	Rails
"	"	"	"	REG101UA-2.85/2K5	Tape and Reel
2.8V Output					
REG101NA-2.8	SOT23-5	331	R01E	REG101NA-2.8/250	Tape and Reel
"	"	"	"	REG101NA-2.8/3K	Tape and Reel
REG101UA-2.8	SO-8	182	REG101U28	REG101UA-2.8	Rails
"	"	"	"	REG101UA-2.8/2K5	Tape and Reel
2.5V Output					
REG101NA-2.5	SOT23-5	331	R01G	REG101NA-2.5/250	Tape and Reel
"	"	"	"	REG101NA-2.5/3K	Tape and Reel
REG101UA-2.5	SO-8	182	REG101U25	REG101UA-2.5	Rails
"	"	"	"	REG101UA-2.5/2K5	Tape and Reel
Adjustable Output					
REG101NA-A	SOT23-5	331	R01A	REG101NA-A/250	Tape and Reel
"	"	"	"	REG101NA-A/3K	Tape and Reel
REG101UA-A	SO-8	182	REG101UA	REG101UA-A	Rails
"	"	"	"	REG101UA-A/2K5	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "REG101UA-5/2K5" will get a single 2500-piece Tape and Reel.

Many custom output voltage versions, from 2.5V to 5.1V in 50mV increments, are available upon request. Minimum order quantities apply. Contact factory for details.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_J = –40°C to +85°C.**

At T_J = +25°C, V_{IN} = V_{OUT} + 1V (V_{OUT} = 2.5V for REG101-A), V_{ENABLE} = 1.8V, I_{OUT} = 2mA, C_{NR} = 0.01µF, and C_{OUT} = 0.1µF[1], unless otherwise noted.

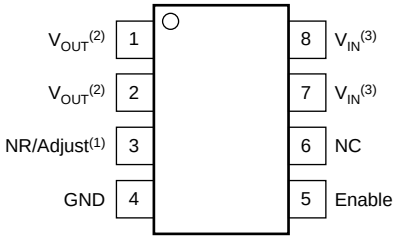
PARAMETER		CONDITION	REG101NA REG101UA MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE						
Output Voltage	V_{OUT}					
REG101-2.5				2.5		V
REG101-2.8				2.8		V
REG101-2.85				2.85		V
REG101-3.0				3.0		V
REG101-3.3				3.3		V
REG101-5				5		V
REG101-A			2.5		5.5	V
Reference Voltage	V_{REF}			1.267		V
Adjust Pin Current	I_{ADJ}			0.2	1	µA
Accuracy				±0.5	±1.5	%
Over Temperature					**±2.2**	%
vs Temperature	**dV_{OUT}/dT**			**50**		ppm/°C
Includes Line and Load		I_{OUT} = 2mA to 100mA, V_{IN} = (V_{OUT} + 0.4V) to 10V		±0.8	±2.0	%
Over Temperature		**V_{IN} = (V_{OUT} + 0.6V) to 10V**			**±2.7**	**%**
DC DROPOUT VOLTAGE[2]	V_{DROP}	I_{OUT} = 2mA		4	10	mV
For all models		I_{OUT} = 100mA		60	100	mV
Over Temperature		**I_{OUT} = 100mA**			**130**	mV
VOLTAGE NOISE	V_n	f = 10Hz to 100kHz				
Without C_{NR}		C_{NR} = 0, C_{OUT} = 0		23µVrms/V • V_{OUT}		µVrms
With C_{NR} (all fixed voltage models)		C_{NR} = 0.01µF, C_{OUT} = 10µF		7µVrms/V • V_{OUT}		µVrms
OUTPUT CURRENT						
Current Limit[3]	I_{CL}		130	170	220	mA
Over Temperature			**110**		**240**	mA
Short-Circuit Current	I_{SC}			60		mA
RIPPLE REJECTION						
f = 120Hz		I_{OUT} = 100mA		65		dB
ENABLE CONTROL						
V_{ENABLE} High (output enabled)	V_{ENABLE}		1.8		V_{IN}	V
V_{ENABLE} Low (output disabled)			–0.2		0.5	V
I_{ENABLE} High (output enabled)	I_{ENABLE}	V_{ENABLE} = 1.8V to V_{IN}, V_{IN} = 1.8V to 6.5[4]		1	100	nA
I_{ENABLE} Low (output disabled)		V_{ENABLE} = 0V to 0.5V		2	100	nA
Output Disable Time		C_{OUT} = 1.0µF, R_{LOAD} = 33Ω		200		µs
Output Enable Time		C_{OUT} = 1.0µF, R_{LOAD} = 33Ω		1.5		ms
THERMAL SHUTDOWN						
Junction Temperature						
Shutdown				160		°C
Reset from Shutdown				140		°C
GROUND PIN CURRENT						
Ground Pin Current	I_{GND}	I_{OUT} = 2mA		400	500	µA
		I_{OUT} = 100mA		500	650	µA
Enable Pin Low		$V_{ENABLE} \leq$ 0.5V		0.01	0.2	µA
INPUT VOLTAGE	V_{IN}					
Operating Input Voltage Range[5]			1.8		10	V
Specified Input Voltage Range		V_{IN} > 1.8V	V_{OUT} + 0.4		10	V
Over Temperature		**V_{IN} > 1.8V**	**V_{OUT} + 0.6**		**10**	V
TEMPERATURE RANGE						
Specified Range	T_J		–40		+85	°C
Operating Range	T_J		–55		+125	°C
Storage Range	T_A		–65		+150	°C
Thermal Resistance						
SOT23-5 Surface Mount	θ_{JA}	Junction-to-Ambient		200		°C/W
SO-8 Surface Mount	θ_{JA}	Junction-to-Ambient		150		°C/W

NOTES: (1) The REG101 does not require a minimum output capacitor for stability. However, transient response can be improved with proper capacitor selection. (2) Dropout voltage is defined as the input voltage minus the output voltage that produces a 2% change in the output voltage from the value at V_{IN} = V_{OUT} + 1V at fixed load. (3) Current limit is the output current that produces a 10% change in output voltage from V_{IN} = V_{OUT} + 1V and I_{OUT} = 2mA. (4) For V_{ENABLE} > 6.5V, see typical characteristic "I_{ENABLE} vs V_{ENABLE}". (5) The REG101 no longer regulates when V_{IN} < V_{OUT} + $V_{DROP\ (MAX)}$. In drop-out, the impedance from V_{IN} to V_{OUT} is typically less than 1Ω at T_J = +25°C.

PIN CONFIGURATIONS

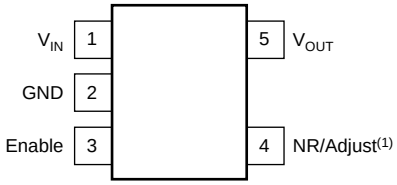
Top View

SO-8



(U Package)

SOT23-5



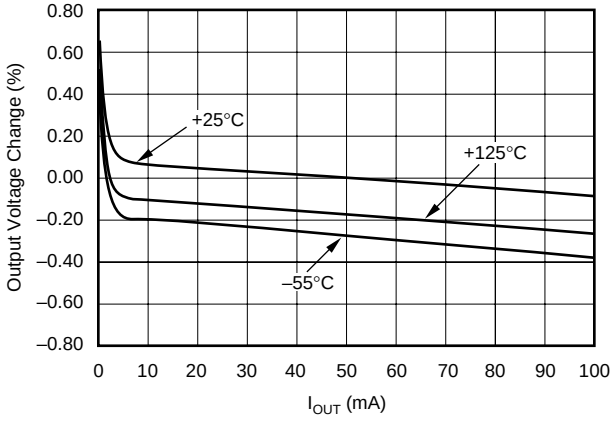
(N Package)

NOTE: (1) For REG101A-A: voltage setting resistor pin. All other models: noise reduction capacitor pin.
(2) Both pin 1 and pin 2 must be connected.
(3) Both pin 7 and pin 8 must be connected.

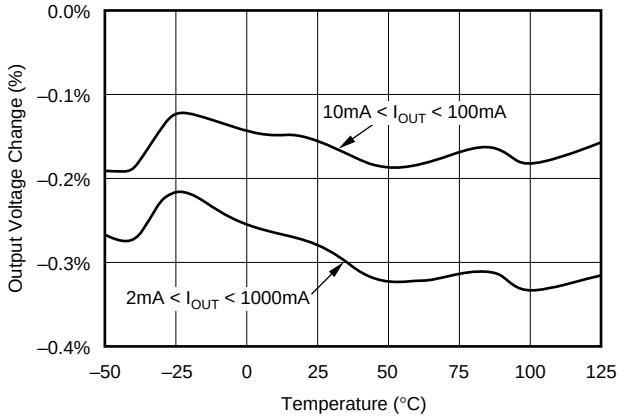
TYPICAL CHARACTERISTICS

For all models, at T_J = +25°C and V_{ENABLE} = 1.8V, unless otherwise noted.

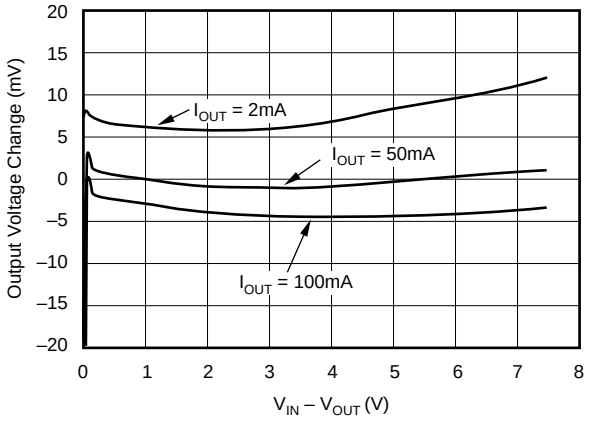
OUTPUT VOLTAGE CHANGE vs I_{OUT}
(V_{IN} = V_{OUT} + 1V, Output Voltage % Change
Refered to I_{OUT} = 50mA at +25°C)



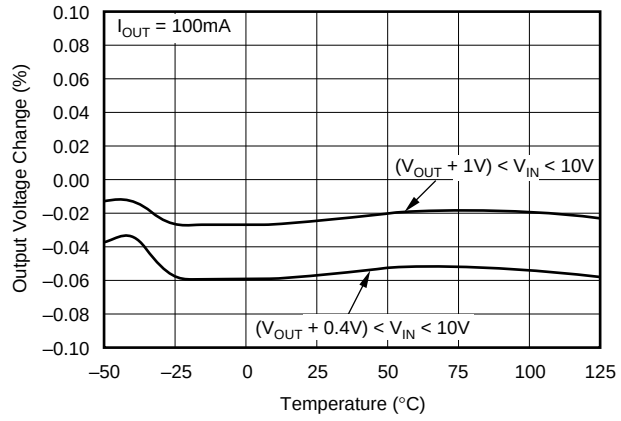
LOAD REGULATION vs TEMPERATURE
(V_{IN} = V_{OUT} + 1V)



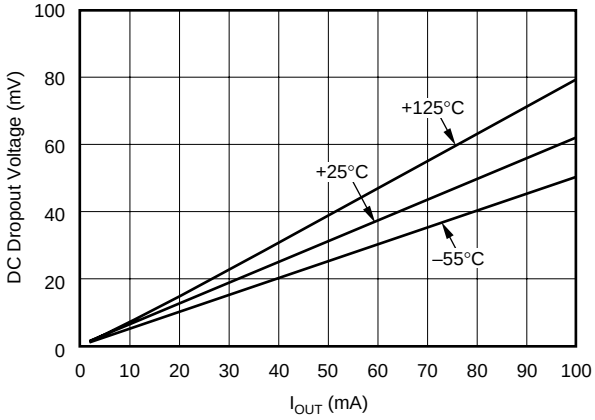
LINE REGULATION
(Referred to V_{IN} = V_{OUT} + 1V at I_{OUT} = 50mA)



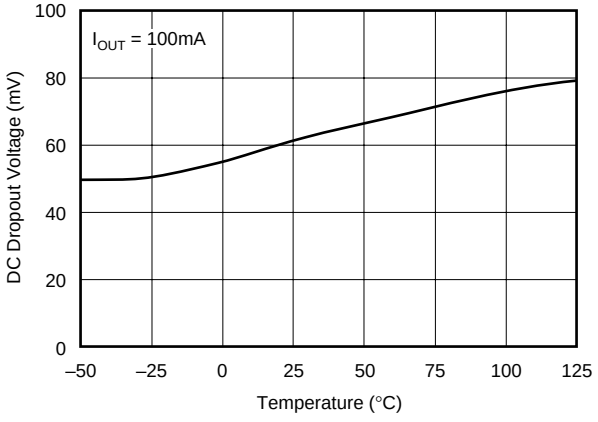
LINE REGULATION vs TEMPERATURE



DC DROPOUT VOLTAGE vs I_{OUT}



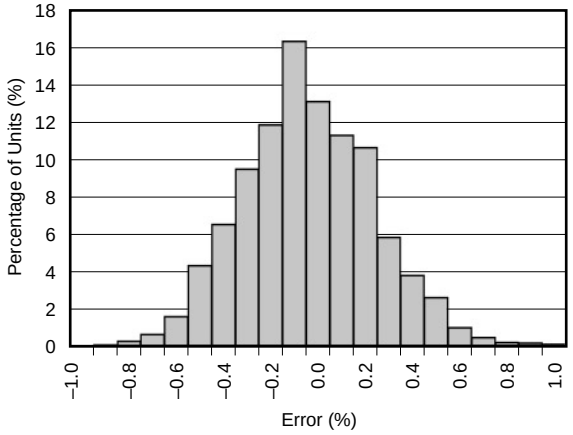
DC DROPOUT VOLTAGE vs TEMPERATURE



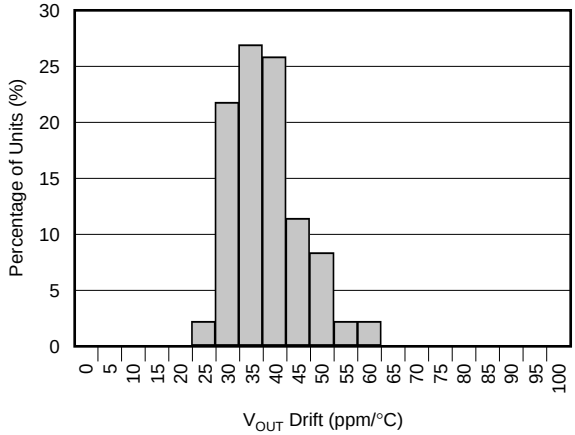
TYPICAL CHARACTERISTICS (Cont.)

For all models, at T_J = +25°C and V_{ENABLE} = 1.8V, unless otherwise noted.

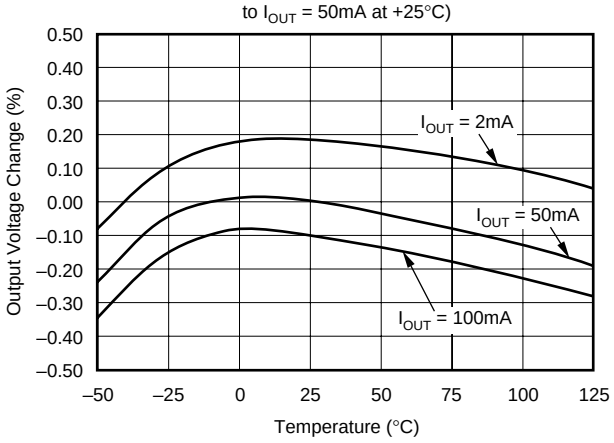
OUTPUT VOLTAGE ACCURACY HISTOGRAM



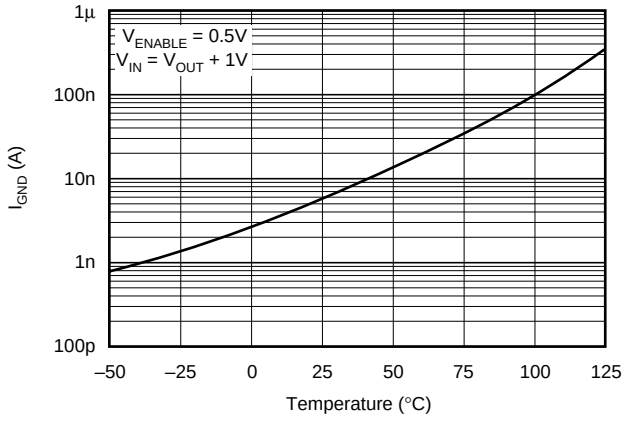
OUTPUT VOLTAGE DRIFT HISTOGRAM



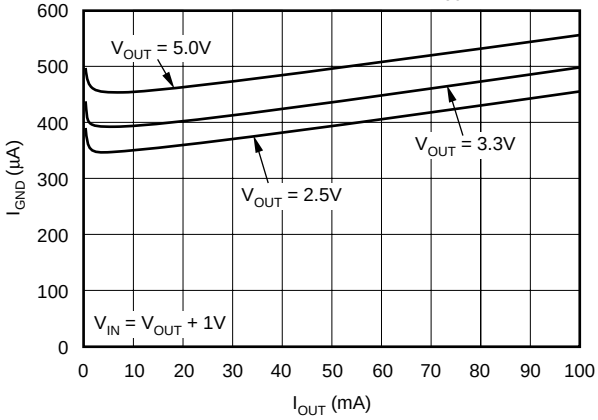
OUTPUT VOLTAGE vs TEMPERATURE
(Output Voltage % Change Referred to I_{OUT} = 50mA at +25°C)



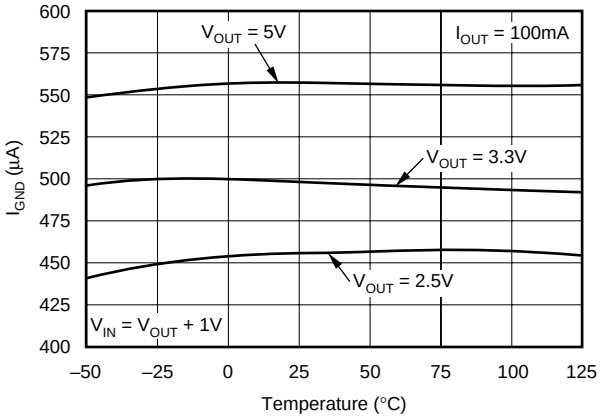
GROUND PIN CURRENT, NOT ENABLED vs TEMPERATURE



GROUND PIN CURRENT vs I_{OUT}



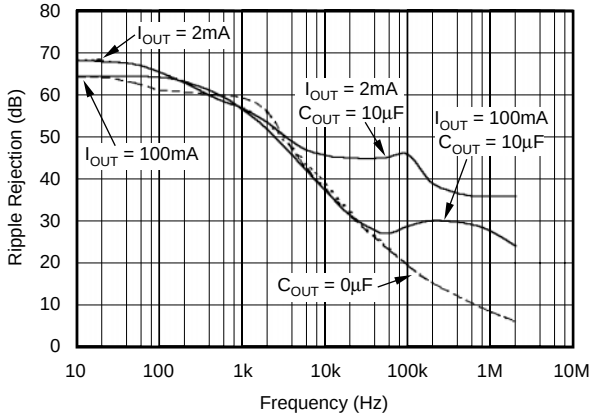
GROUND PIN CURRENT vs TEMPERATURE



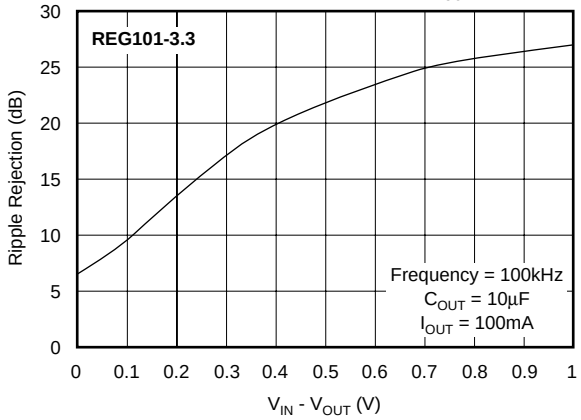
TTYPICAL CHARACTERISTICS (Cont.)

For all models, at T_J = +25°C and V_{ENABLE} = 1.8V, unless otherwise noted.

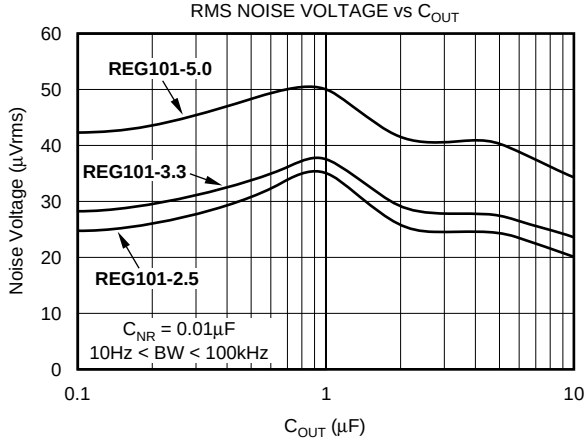
RIPPLE REJECTION vs FREQUENCY



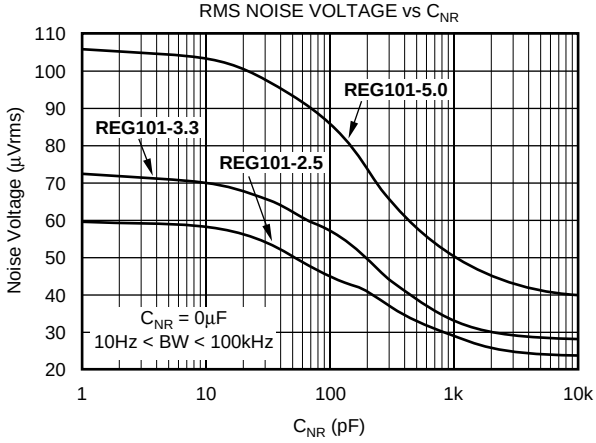
RIPPLE REJECTION vs (V_{IN} – V_{OUT})



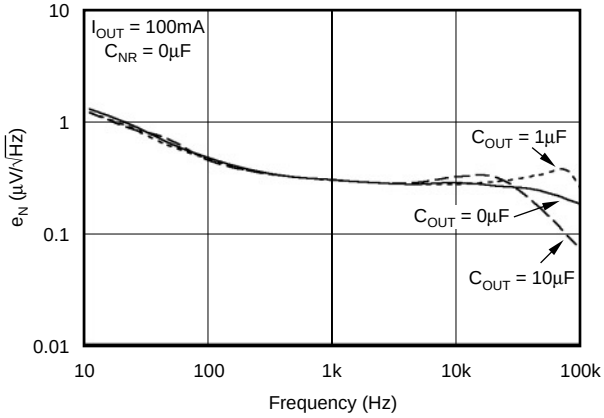
RMS NOISE VOLTAGE vs C_{OUT}



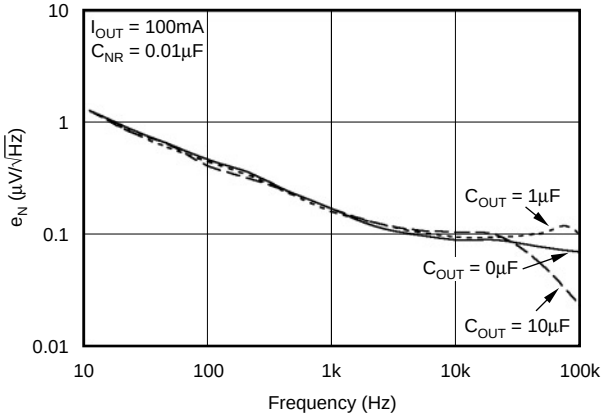
RMS NOISE VOLTAGE vs C_{NR}



NOISE SPECTRAL DENSITY



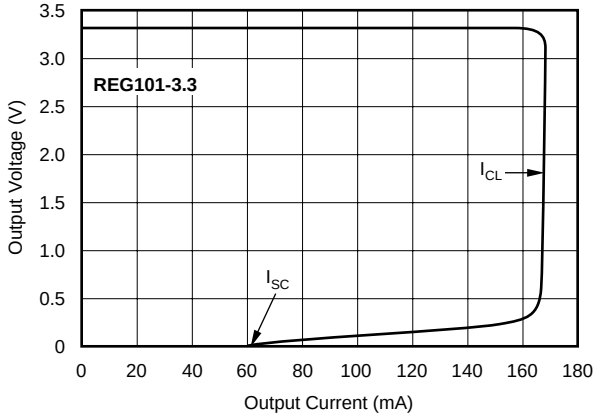
NOISE SPECTRAL DENSITY



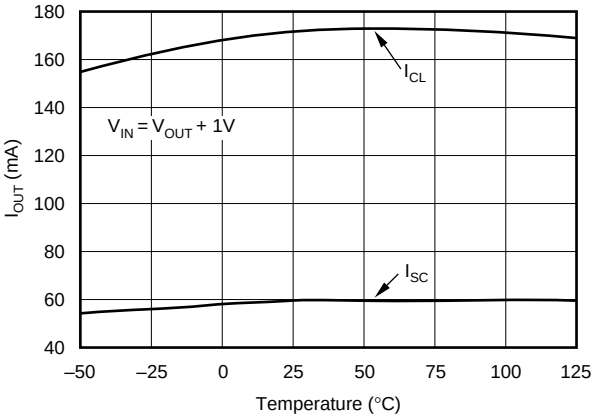
TYPICAL CHARACTERISTICS (Cont.)

For all models, at T_J = +25°C and V_{ENABLE} = 1.8V, unless otherwise noted.

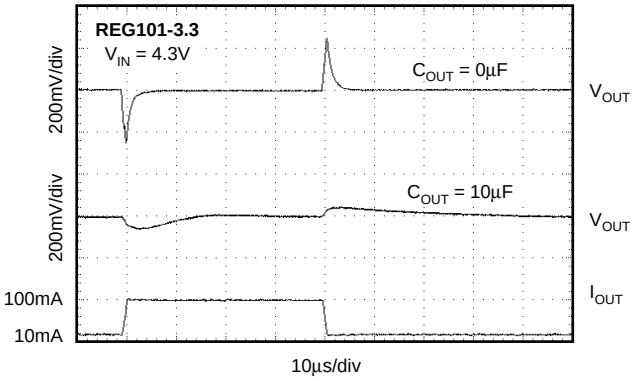
FOLDBACK CURRENT LIMIT



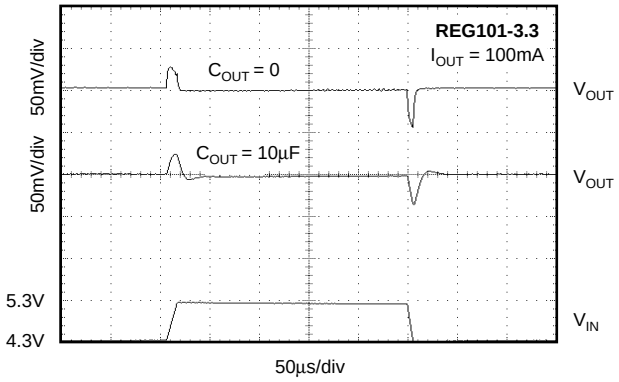
CURRENT LIMIT vs TEMPERATURE



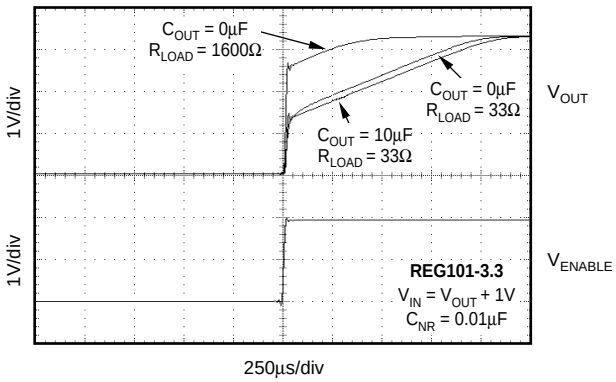
LOAD TRANSIENT RESPONSE



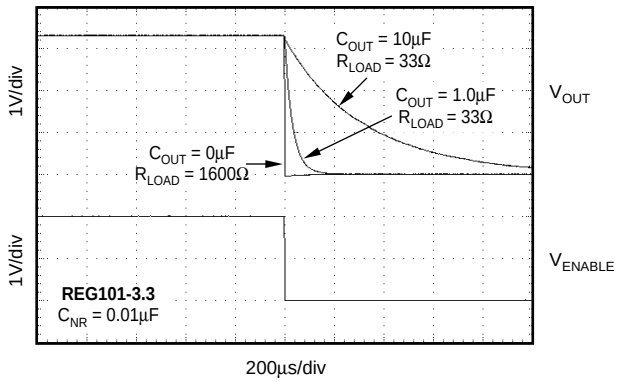
LINE TRANSIENT RESPONSE



TURN-ON



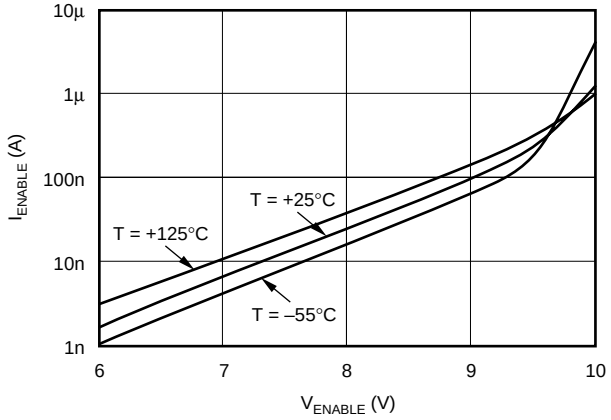
TURN-OFF



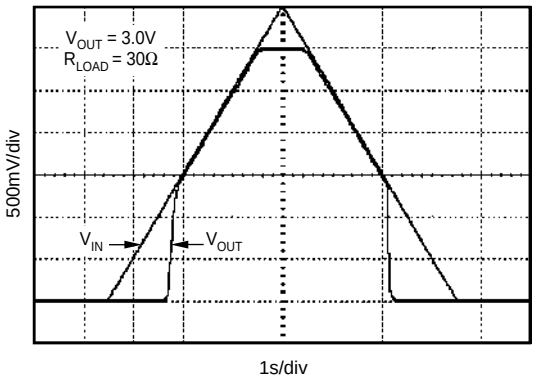
TYPICAL CHARACTERISTICS (Cont.)

For all models, at T_J = +25°C and V_{ENABLE} = 1.8V, unless otherwise noted.

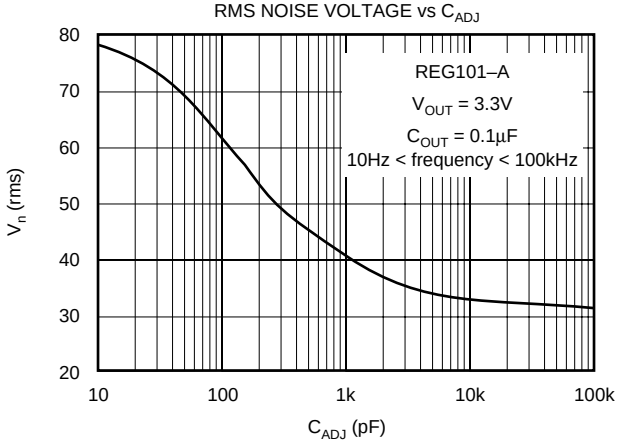
I_{ENABLE} vs V_{ENABLE}



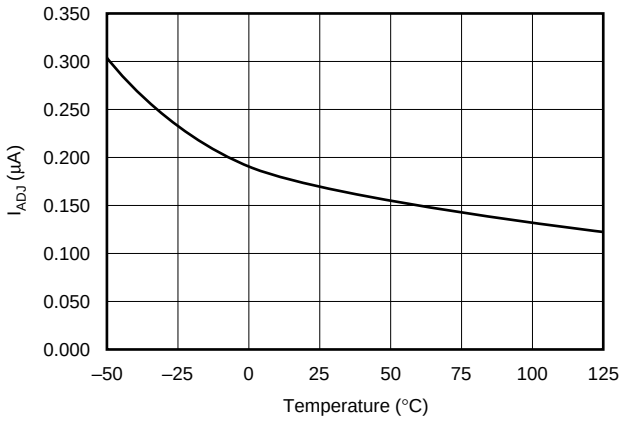
POWER UP/POWER DOWN



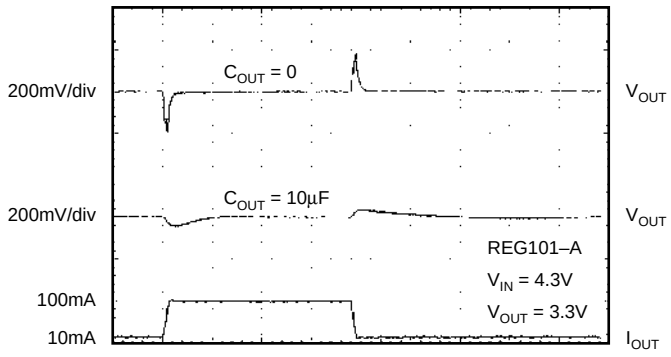
RMS NOISE VOLTAGE vs C_{ADJ}



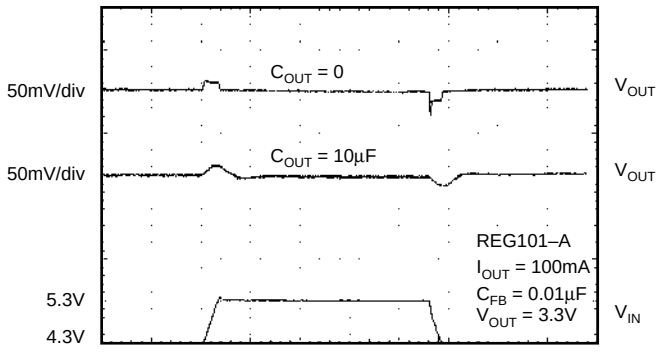
ADJUST PIN CURRENT vs TEMPERATURE



LOAD TRANSIENT-ADJUSTABLE VERSION



LINE TRANSIENT-ADJUSTABLE VERSION



BASIC OPERATION

The REG101 series of LDO (Low Drop-Out) linear regulators offers a wide selection of fixed output voltage versions and an adjustable output version. The REG101 belongs to a family of new generation LDO regulators that utilize a DMOS pass transistor to achieve ultra-low dropout performance and freedom from output capacitor constraints. Ground pin current remains under 650µA over all line, load, and temperature conditions. All versions have thermal and overcurrent protection, including foldback current limit.

The REG101 does not require an output capacitor for regulator stability and is stable over most output currents and with almost any value and type of output capacitor up to 10µF or more. For applications where the regulator output current drops below several milliamps, stability can be enhanced by: adding a 1kΩ to 2kΩ load resistor; using capacitance values less than 10µF; or keeping the effective series resistance greater than 0.05Ω including the capacitor's ESR and parasitic resistance in printed circuit board traces, solder joints, and sockets.

Although an input capacitor is not required, it is good analog design practice to connect a 0.1µF low ESR capacitor across the input supply voltage. This is recommended to improve ripple rejection by reducing input voltage ripple.

Figure 1 shows the basic circuit connections for the fixed voltage models. Figure 2 gives the connections for the adjustable output version (REG101A) and example resistor values for some commonly used output voltages. Values for other voltages can be calculated from the equation shown in Figure 2.

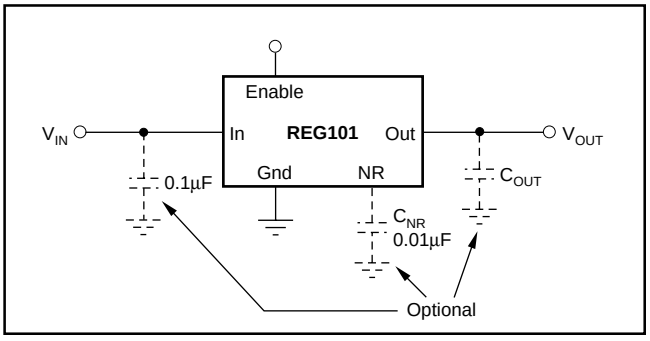


FIGURE 1. Fixed Voltage Nominal Circuit for REG101.

INTERNAL CURRENT LIMIT

The REG101 internal current limit has a typical value of 170mA. A foldback feature limits the short-circuit current to a typical short-circuit value of 60mA. This helps to protect the regulator from damage under all load conditions. A characteristic of V_{OUT} versus I_{OUT} is given in Figure 3 and in the Typical Characteristics section.

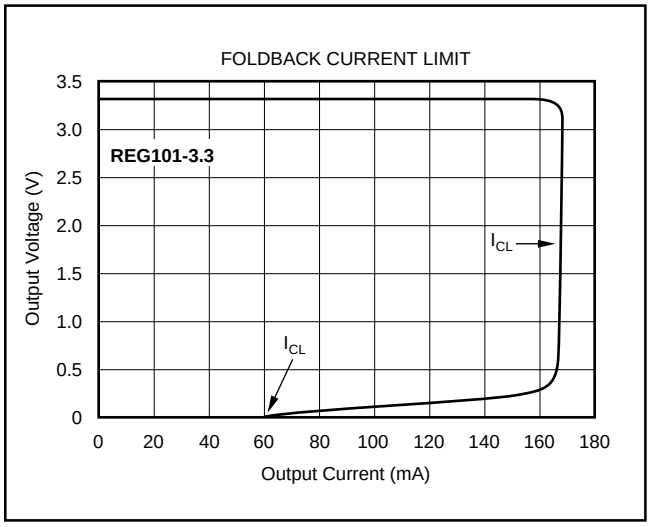
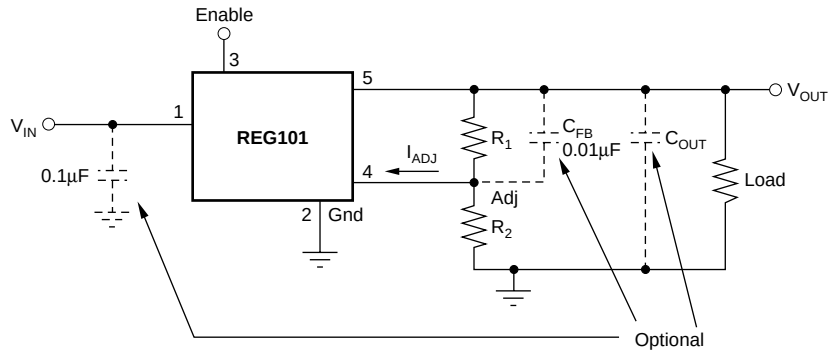


FIGURE 3. Foldback Current Limit of the REG101-3.3 at 25°C.



Pin numbers for SOT23 package.

$$V_{OUT} = (1 + R_1/R_2) \cdot 1.267V$$

To reduce current through divider, increase resistor values (see table at right).

As the impedance of the resistor divider increases, I_{ADJ} (~200nA) may introduce an error.

C_{FB} improves noise and transient response.

EXAMPLE RESISTOR VALUES

V_{OUT} (V)	R_1 (W)(1)	R_2 (Ω)(1)
2.5	11.3k 1.13k	11.5k 1.15k
3.0	15.8k 1.58k	11.5k 1.15k
3.3	18.7k 1.87k	11.5k 1.15k
5.0	34.0k 3.40k	11.5k 1.15k

NOTE: (1) Resistors are standard 1% values.

FIGURE 2. Adjustable Voltage Circuit for REG101A.

ENABLE

The Enable pin is active HIGH and compatible with standard TTL-CMOS levels. Inputs below 0.5V (max) turn the regulator off and all circuitry is disabled. Under this condition, ground pin current drops to approximately 10nA. When a pull-up resistor is used, and operation down to V_{IN} = 1.8V is required, use values < 50kΩ.

OUTPUT NOISE

A precision band-gap reference is used for the internal reference voltage, V_{REF}. This reference is the dominant noise source within the REG101 and it generates approximately 29μVrms in the 10Hz to 100kHz bandwidth at the reference output. The regulator control loop gains up the reference noise, so that the noise voltage of the regulator is approximately given by:

$$V_N = 29\mu Vrms \frac{R_1 + R_2}{R2} = 29\mu Vrms \bullet \frac{V_{OUT}}{V_{REF}}$$

Since the value of V_{REF} is 1.267V, this relationship reduces to:

$$V_N = 23 \frac{\mu Vrms}{V} \bullet V_{OUT}$$

Connecting a capacitor, C_{NR}, from the Noise Reduction (NR) pin to ground, as shown in Figure 4, forms a low-pass filter for the voltage reference. For C_{NR} = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by approximately a factor of 2.8 for V_O = 3.3V. This noise reduction effect is shown in Figure 5 and as "RMS Noise Voltage vs CNR" in the Typical Characteristics section.

Noise can be further reduced by carefully choosing an output capacitor, C_{OUT}. Best overall noise performance is achieved with very low (< 0.22μF) or very high (> 2.2μF) values of C_{OUT}. See "RMS Noise Voltage vs C_{OUT}" in the Typical Characteristics section.

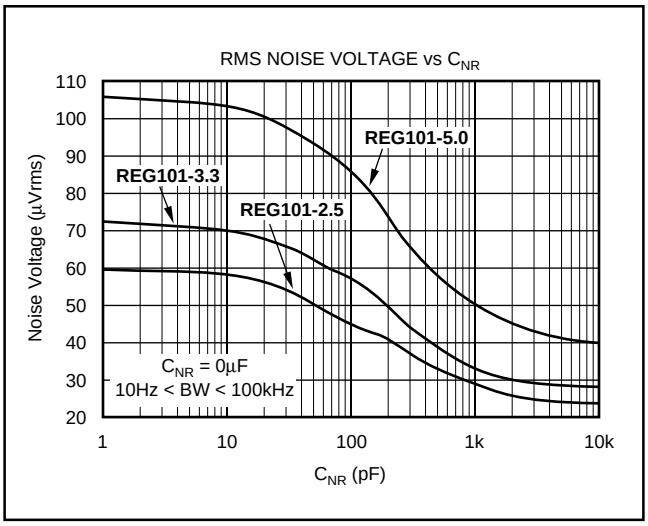


FIGURE 5. Output Noise versus Noise Reduction Capacitor.

The REG101 utilizes an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the DMOS pass element above V_{IN}. The charge-pump switching noise (nominal switching frequency = 2MHz) is not measurable at the output of the regulator over most values of C_{OUT} and I_{OUT}.

The REG101 adjustable version does not have the noise-reduction pin available, however, the adjust pin is the summing junction of the error amplifier. A capacitor, C_{FB}, connected from the output to the adjust pin will reduce both the output noise and the peak error from a load transient. See the typical characteristics for output noise performance.

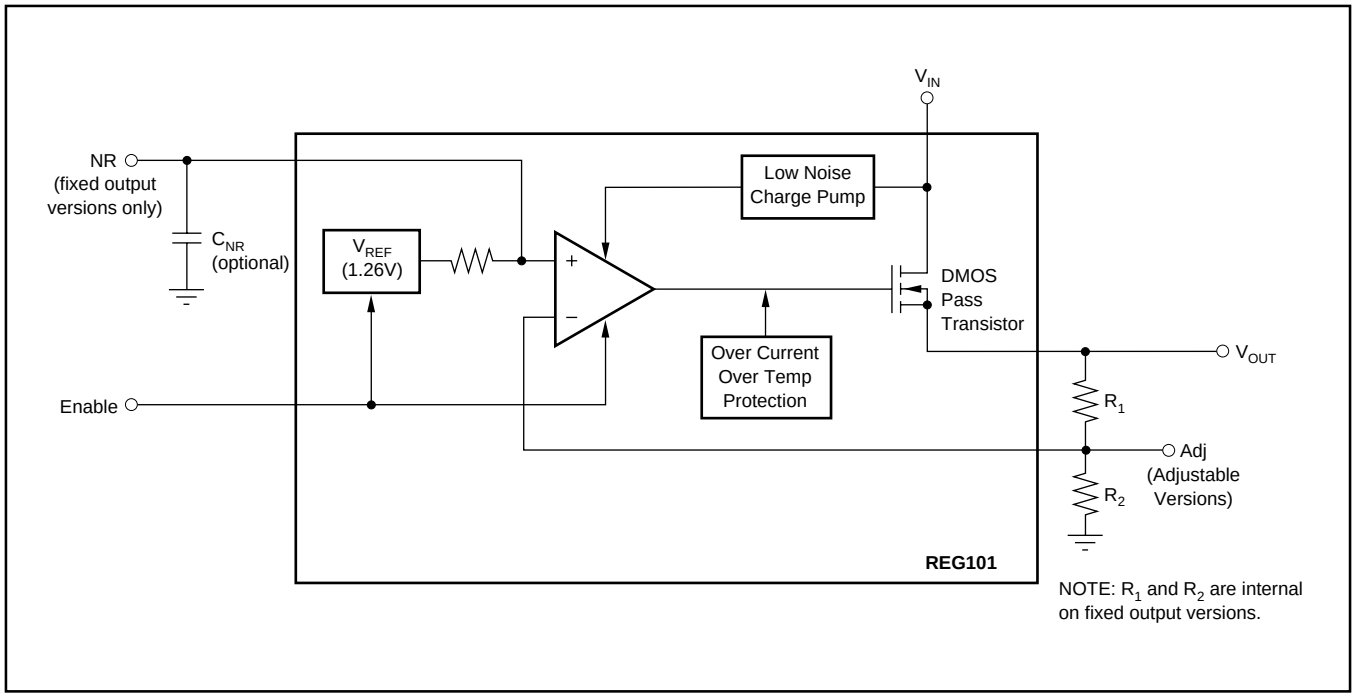


FIGURE 4. Block Diagram.

DROP-OUT VOLTAGE

The REG101 uses an N-channel DMOS as the "pass" element. When the input voltage is within a few tens of millivolts of the output voltage, the DMOS device behaves like a resistor. Therefore, for low values of V_{IN} to V_{OUT}, the regulator's input-to-output resistance is the Rds_{ON} of the DMOS pass element (typically 600mΩ). For static (DC) loads, the REG101 will typically maintain regulation down to V_{IN} to V_{OUT} voltage drop of 60mV at full rated output current. In Figure 6, the bottom line (DC dropout) shows the minimum V_{IN} to V_{OUT} voltage drop required to prevent drop-out under DC load conditions.

For large step changes in load current, the REG101 requires a larger voltage drop across it to avoid degraded transient response. The boundary of this "transient drop-out" region is shown as the top line in Figure 6. Values of V_{IN} to V_{OUT} voltage drop above this line insure normal transient response.

In the transient dropout region between "DC" and "Transient", transient response recovery time increases. The time required to recover from a load transient is a function of both the magnitude and rate of the step change in load current and the available "headroom" V_{IN} to V_{OUT} voltage drop. Under worst-case conditions (full-scale load change with V_{IN} to V_{OUT} voltage drop close to DC dropout levels), the REG101 can take several hundred microseconds to re-enter the specified window of regulation.

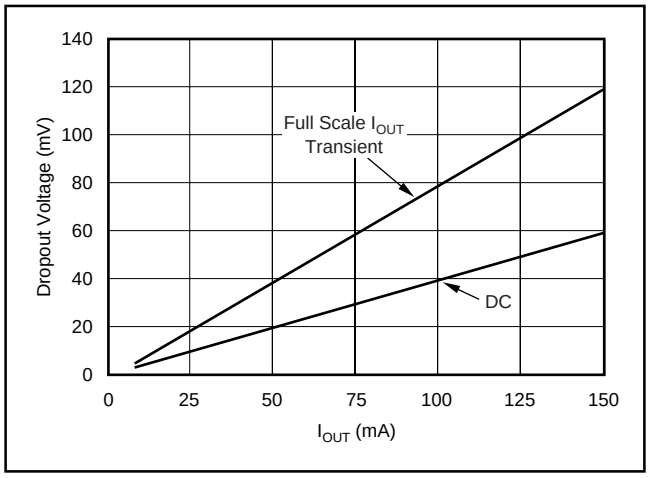


FIGURE 6. Transient and DC Dropout.

TRANSIENT RESPONSE

The REG101 response to transient line and load conditions improves at lower output voltages. The addition of a capacitor (nominal value 0.47µF) from the output pin to ground may improve the transient response. In the adjustable version, the addition of a capacitor, C_{FB} (nominal value 10nF), from the output to the adjust pin will also improve the transient response.

THERMAL PROTECTION

The REG101 has thermal shutdown circuitry that protects the regulator from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on various conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, but may have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loads and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the REG101 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the REG101 into thermal shutdown will degrade reliability.

POWER DISSIPATION

The REG101 is available in two different package configurations. The ability to remove heat from the die is different for each package type and, therefore, presents different considerations in the printed circuit-board layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. While it is difficult-to-impossible to quantify all of the variables in a thermal design of this type, performance data for several configurations are shown in Figure 7.

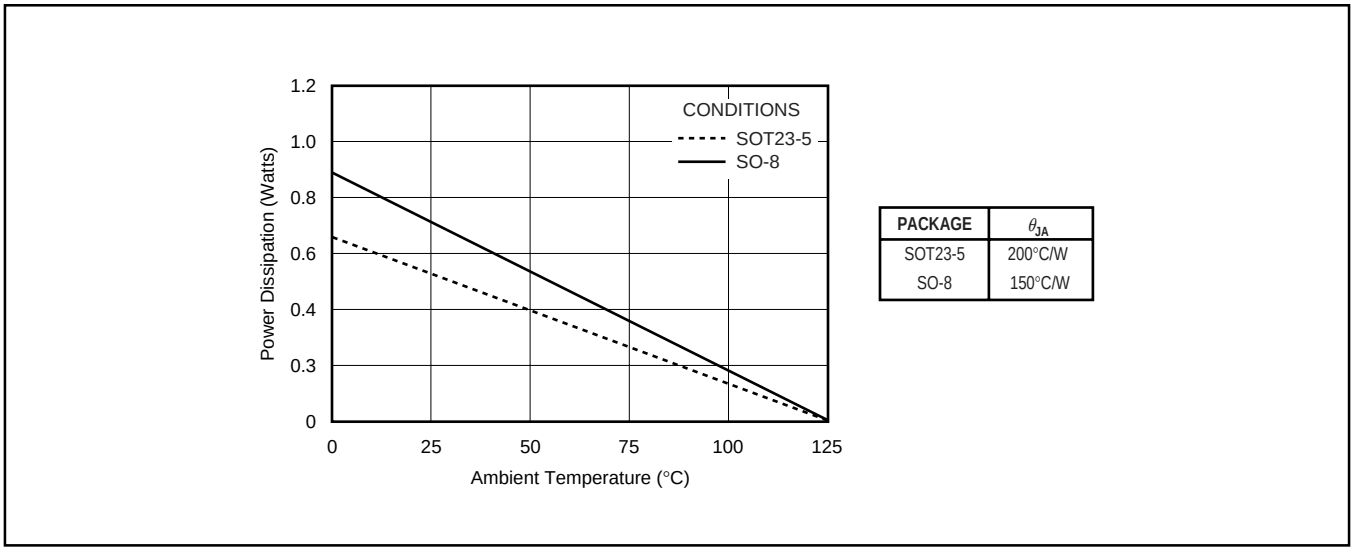
Power dissipation depends on input voltage, load condition, and duty cycle. Power dissipation is equal to the product of the average output current times the voltage across the output element, V_{IN} to V_{OUT} voltage drop.

$$P_D = (V_{IN} - V_{OUT}) \bullet I_{OUT(AVG)}$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

REGULATOR MOUNTING

Solder pad footprint recommendations for the various REG101 devices are presented in the Application Bulletin AB-132, "Solder Pad Recommendations for Surface-Mount Devices" (SBFA015), available from the Texas Instruments web site (www.ti.com).



PACKAGE	θ_{JA}
SOT23-5	200°C/W
SO-8	150°C/W

FIGURE 7. Maximum Power Dissipation versus Ambient Temperature for the Various Packages.

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