Configuration EPROMs

for FLEX Devices

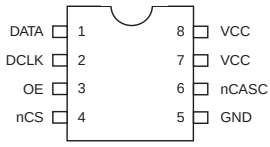
January 1998, ver. 8 Data Sheet

Features

- Serial EPROM family for configuring FLEX® devices
- Simple, easy-to-use 4-pin interface to FLEX devices
- Low current during configuration and near-zero standby current
- 5.0-V and 3.3-V operation
- Software design support with the Altera® MAX+PLUS II development system for 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Programming support with Altera's Master Programming Unit (MPU) and programming hardware from Data I/O, BP Microsystems, and other manufacturers
- Available in compact, one-time-programmable (OTP) plastic packages (see Figure 1)
  - 8-pin plastic dual in-line package (PDIP)
  - 20-pin plastic J-lead chip carrier (PLCC) package
  - 32-pin plastic thin quad flat pack (TQFP)

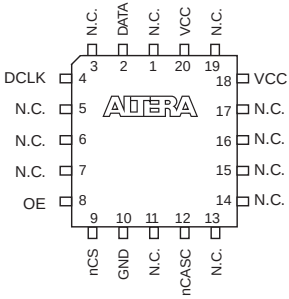
Figure 1. Configuration EPROM Package Pin-Out Diagrams

Package outlines not drawn to scale.



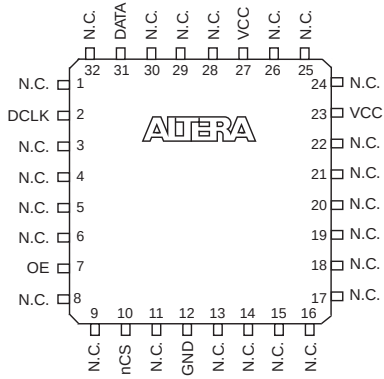
8-Pin PDIP

EPC1
EPC1441
EPC1213
EPC1064
EPC1064V



20-Pin PLCC

EPC1
EPC1441
EPC1213
EPC1064
EPC1064V



32-Pin TQFP

EPC1441
EPC1064
EPC1064V

Functional Description

With SRAM-based devices, configuration data must be reloaded each time the system initializes, or whenever new configuration data is needed. The Altera Configuration EPROMs store configuration data for SRAM-based FLEX devices. Table 1 lists the Configuration EPROMs provided by Altera.

Table 1. Configuration EPROMs

Device	Description
EPC1	1,046,496 × 1 bit device with 5.0-V or 3.3-V operation
EPC1441	440,800 × 1 bit device with 5.0-V or 3.3-V operation
EPC1213	212,942 × 1 bit device with 5.0-V operation
EPC1064	65,536 × 1 bit device with 5.0-V operation
EPC1064V	65,536 × 1 bit device with 3.3-V operation

Table 2 lists appropriate Configuration EPROMs for FLEX devices.

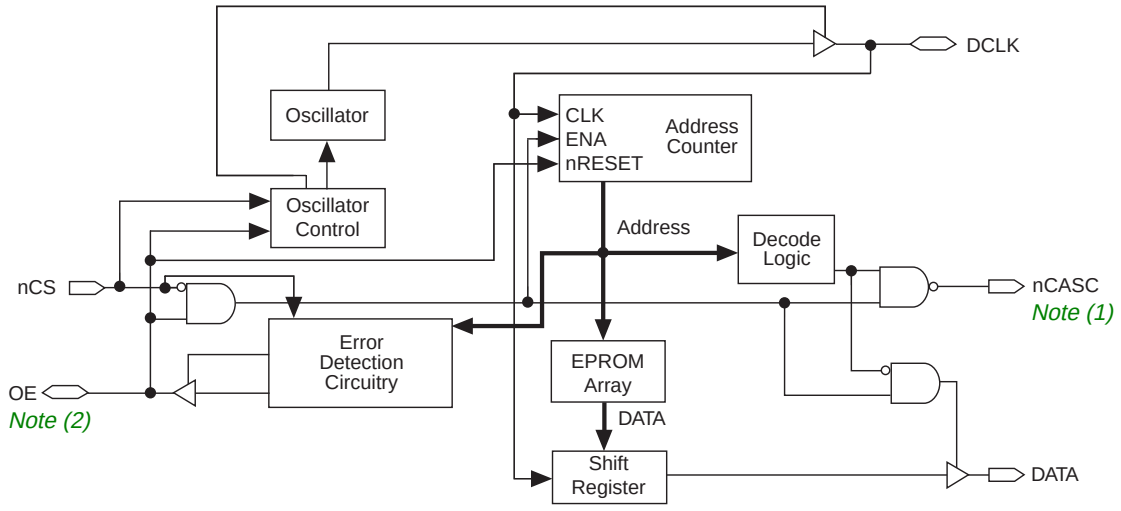
Table 2. Appropriate Configuration EPROM for FLEX Devices

FLEX Device	Configuration EPROM
EPF10K10, EPF10K10A	EPC1 or EPC1441
EPF10K20	EPC1 or EPC1441
EPF10K30, EPF10K30A, EPC10K30B	EPC1 or EPC1441
EPF10K40	EPC1
EPF10K50, EPF10K50V, EPF10K50B	EPC1
EPF10K70	EPC1
EPF10K100, EPF10K100A, EPF10K100B	Two EPC1 devices
EPF10K130V, EPF10K130B	Two EPC1 devices
EPF10K180B	Three EPC1 devices
EPF10K250A, EPF10K250B	Four EPC1 devices
EPF8282A	EPC1, EPC1441, EPC1213, or EPC1064
EPF8282AV	EPC1, EPC1441, or EPC1064V
EPF8452A	EPC1, EPC1441, EPC1213, or EPC1064
EPF8636A	EPC1, EPC1441, or EPC1213
EPF8820A	EPC1, EPC1441, or EPC1213
EPF81188A	EPC1, EPC1441, or EPC1213
EPF81500A	EPC1, EPC1441, or two EPC1213 devices
EPF6016, EPF6016A	EPC1 or EPC1441
EPF6024A	EPC1 or EPC1441

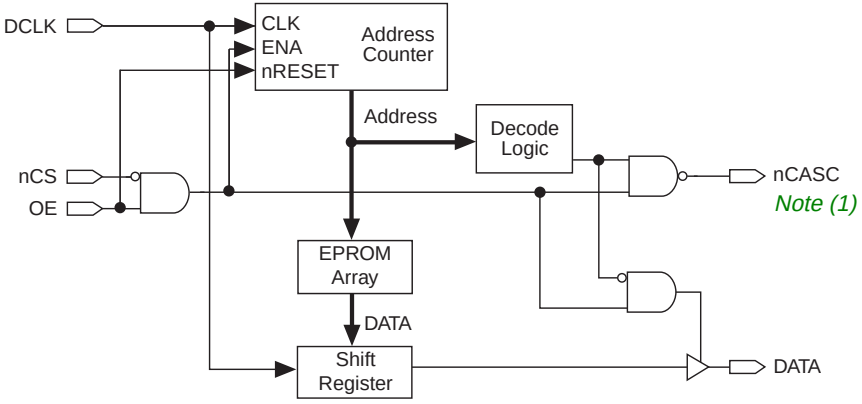
Figure 2 shows the Configuration EPROM block diagram.

Figure 2. Configuration EPROM Block Diagram

FLEX 10K & FLEX 6000 Device Configuration Using an EPC1 or EPC1441



FLEX 8000 Device Configuration Using an EPC1, EPC1441, EPC1213, EPC1064, or EPC1064V



Notes:

(1) The EPC1441, EPC1064, and EPC1064V devices do not support data cascading. The EPC1 and EPC1213 devices do support data cascading.

(2) The OE pin is a bidirectional open-drain pin.

Device Configuration

The control signals for Configuration EPROMs—nCS, OE, and DCLK—interface directly with FLEX device control signals. All FLEX devices can control the entire configuration process and retrieve data from the Configuration EPROM without requiring an external intelligent controller.

The Configuration EPROM OE and nCS pins control the tri-state buffer on the DATA output pin and enable the address counter (and the oscillator in the EPC1 and EPC1441 devices). When OE is driven low, the Configuration EPROM resets the address counter and tri-states its DATA pin. The nCS pin controls the output of the Configuration EPROMs. If nCS is held high after the OE reset pulse, the counter is disabled and the DATA output pin is tri-stated. When nCS is driven low, the counter and the DATA output pin are enabled. When OE is driven low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of nCS.

The EPC1 and EPC1441 devices determine the operation mode and whether FLEX 10K, FLEX 8000, or FLEX 6000 protocols should be used when OE is driven high.

When the Configuration EPROM has driven out all of its data and drives nCASC low, the device tri-states the DATA pin to avoid contention with other Configuration EPROMs. Upon power-up, the address counter is automatically reset.

FLEX 10K & FLEX 6000 Device Configuration

FLEX 10K and FLEX 6000 devices can be configured with EPC1 or EPC1441 Configuration EPROMs. The EPC1 or EPC1441 device stores configuration data in its EPROM array and serially clocks the data out with an internal oscillator. The OE, nCS, and DCLK pins supply the control signals for the address counter and the output tri-state buffer. The EPC1 or EPC1441 device sends a serial bitstream of configuration data to its DATA pin, which is routed to the DATA0 or DATA input pin on the FLEX 10K or FLEX 6000 device. One EPC1441 device can configure the EPF10K10, EPF10K20, or EPF10K30 device. Figure 3 shows a FLEX 10K device configured with a single EPC1 or EPC1441 Configuration EPROM.

Figure 3. FLEX 10K Device Configured with an EPC1 or EPC1441

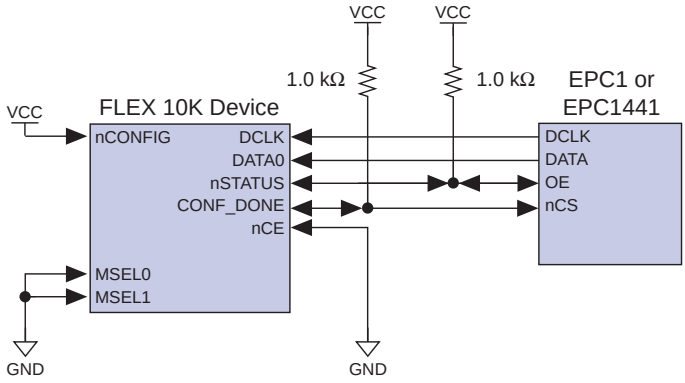
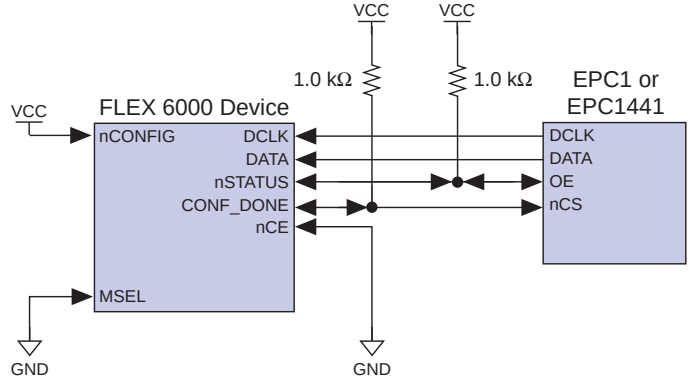


Figure 4 shows a FLEX 6000 device configured with a single EPC1 or EPC1441 Configuration EPROM.

Figure 4. FLEX 6000 Device Configured with an EPC1 or EPC1441



When configuration data for a FLEX 10K device exceeds the capacity of a single EPC1 device, multiple EPC1 devices can be cascaded together. (The EPC1441 does not support data cascading.) If multiple EPC1 devices are required, the nCASC and nCS pins provide handshaking between the EPC1 devices.

When configuring FLEX devices with cascaded EPC1 devices, the position of an EPC1 device in the chain determines its operation. When the first EPC1 device in a Configuration EPROM chain is powered up or reset and the nCS pin is driven low, the EPC1 will control FLEX 10K configuration. This EPC1 device supplies all clock pulses to one or more FLEX 10K devices and to any "downstream" EPC1 devices during configuration. The first EPC1 device also provides the first stream of data to the FLEX 10K devices during multi-device configuration. Once the first EPC1 device finishes sending configuration data, it drives its nCASC pin low, which drives the nCS pin of the second EPC1 device low. This activates the second EPC1 device to send configuration data.

The first EPC1 device clocks all subsequent EPC1 devices until configuration is complete. Once all configuration data is transferred and the nCS pin on the first EPC1 device is driven high via the FLEX 10K device's CONF_DONE pin, the first EPC1 device clocks 16 additional cycles to initialize the FLEX 10K device. The first EPC1 device then goes into zero-power (idle) state. If nCS on the first EPC1 device is driven high before all configuration data is transferred—or if the nCS is not driven high after all configuration data is transferred—the FLEX 10K nSTATUS pin is driven low by the first EPC1 device, indicating a configuration error.

Configuration automatically restarts if the *Auto-Restart Configuration on Frame Error* option is turned on before project compilation in the MAX+PLUS II software **Global Project Device Options** dialog box (Assign menu). Figure 5 shows a FLEX 10K device configured with two EPC1 devices. More EPC1 devices can be added by connecting nCASC to nCS of the subsequent EPC1 device in the chain and connecting DCLK, DATA, and OE in parallel.

When configuring FLEX 10KB devices with an EPC1 device, a 3.3-V power supply is used and the FLEX 10KB VCCIO and pull-up resistors are tied to 3.3-V.

An EPC1 device will emulate an EPC1441 when programmed with a Programmer Object File (**.pof**) generated for an EPC1441 device.

Figure 5. FLEX 10K Device Configured with Two EPC1 Devices

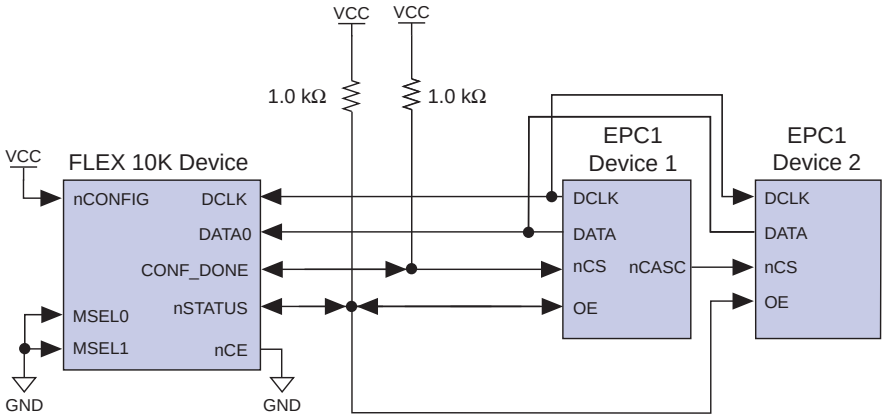


Figure 6 shows two FLEX 10K devices configured with two EPC1 devices.

Figure 6. Two FLEX 10K Devices Configured with Two EPC1 Devices

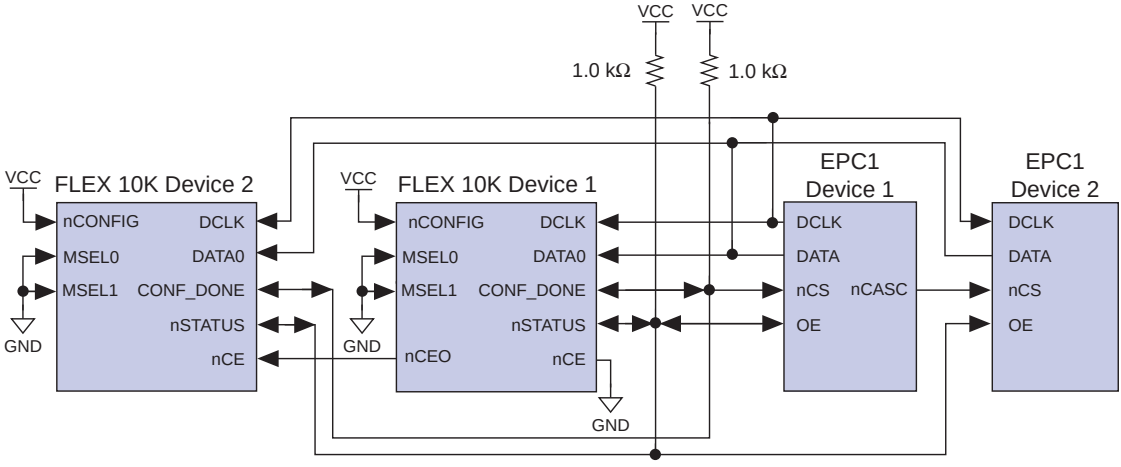


Table 3 describes EPC1 and EPC1441 pin functions during FLEX 10K and FLEX 6000 device configuration.

Table 3. EPC1 & EPC1441 Pin Functions during FLEX 10K & FLEX 6000 Device Configuration

Pin Name	Pin Number			Pin Type	Description
	8-Pin PDIP	20-Pin PLCC	32-Pin TQFP		
	EPC1 & EPC1441		EPC1441		
DATA	1	2	31	Output	Serial data output.
DCLK	2	4	2	I/O	Clock output or clock input. Rising edges on DCLK increment the internal address counter and present the next bit of data to the DATA pin. The counter is incremented only if the OE input is held high, the nCS input is held low, and all configuration data has not been transferred to the target device. On the first EPC1 device in a FLEX 10K or FLEX 6000 configuration cycle, the DCLK pin drives low after configuration is complete or whenever OE is low.
OE	3	8	7	I/O Open-drain	Output enable (active high) and reset (active low). A low logic level resets the address counter. A high logic level enables DATA and permits the address counter to count. In a FLEX 10K or FLEX 6000 configuration cycle, if this pin is low (reset), the internal oscillator becomes inactive and DCLK drives low. See "Error Detection Circuitry" on page 475.
nCS	4	9	10	Input	Chip select input (active low). A low input allows DCLK to increment the address counter and enables DATA to drive out. If the EPC1 is reset with nCS low, the device initializes as the first device in a configuration chain. If the EPC1 is reset with nCS high, the device initializes as the subsequent EPC1 device in the chain.
nCASC	6 *Note (1)*	12 *Note (1)*	– *Note (1)*	Output	Cascade select output (active low). This output goes low when the address counter has reached its maximum value. In a configuration chain of EPC1 devices, the nCASC pin of one device is connected to the nCS input pin of the next device in the chain, which permits DCLK to clock data from the next EPC1 device in the chain.
GND	5	10	12	Ground	A 0.2-µF decoupling capacitor must be placed between the VCC and GND pins.
VCC	7, 8	18, 20	23, 27	Power	Power pin.

Note:

(1) The EPC1441 does not support data cascading. The EPC1 Configuration EPROM supports data cascading.

For more information on FLEX 10K or FLEX 6000 device configuration, go to the following documents:

- *Application Note 59 (Configuring FLEX 10K Devices)*
- *Application Note 87 (Configuring FLEX 6000 Devices)*

FLEX 8000 Device Configuration

FLEX 8000 devices have internal oscillators that can provide a DCLK signal to the Configuration EPROM. The Configuration EPROM sends configuration data out as a serial bitstream on the DATA output pin. This data is routed into the FLEX 8000 device via the DATA0 input pin. The nCASC and nCS pins provide handshaking between multiple Configuration EPROMs, allowing several cascaded EPC1 or EPC1213 devices to serially configure multiple FLEX 8000 devices. The EPC1441, EPC1064 and EPC1064V do not support data cascading.

The EPC1 and EPC1441 can replace the EPC1213, EPC1064, and EPC1064V Configuration EPROMs, which are also used to configure FLEX 8000 devices. The EPC1 or EPC1441 device automatically emulates the EPC1213, EPC1064, or EPC1064V when it is programmed with the appropriate POF. When the EPC1 or EPC1441 device is programmed with a EPC1213, EPC1064, or EPC1064V POF, the FLEX 8000 device drives the EPC1 or EPC1441 device's OE pin high and clocks the EPC1 or EPC1441 device. One EPC1 device can store more configuration data than the EPC1064, EPC1064V, EPC1213, or EPC1441 device. Therefore, designers can use one type of Configuration EPROM, the EPC1, for all FLEX devices. Also, a single EPC1 or EPC1441 device can configure any FLEX 8000 device.

Table 4 describes the pin functions of the EPC1, EPC1441, EPC1213, EPC1064, and EPC1064V devices during FLEX 8000 device configuration.

Table 4. Configuration EPROM Pin Functions during FLEX 8000 Device Configuration

Pin Name	Pin Number			Pin Type	Description
	8-Pin PDIP	20-Pin PLCC	32-Pin TQFP *Note (1)*		
DATA	1	2	31	Output	Serial data output.
DCLK	2	4	2	Input	Clock input. Rising edges on DCLK increment the internal address counter and cause the next bit of data to be presented on DATA. The counter is incremented only if the OE input is held high and the nCS input is held low.
OE	3	8	7	Input	Output enable (active high) and reset (active low). A low logic level resets the address counter. A high logic level enables DATA and permits the address counter to count.
nCS	4	9	10	Input	Chip-select input (active low). A low input allows DCLK to increment the address counter and enables DATA.
nCASC	6 *Note (2)*	12 *Note (2)*	– *Note (2)*	Output	Cascade-select output (active low). This output goes low when the address counter has reached its maximum value. The nCASC output is usually connected to the nCS input of the next Configuration EPROM in a configuration chain, so the next DCLK clocks data out of the next Configuration EPROM.
GND	5	10	12	Ground	A 0.2-µF decoupling capacitor must be placed between the VCC and GND pins.
VCC	7, 8	18, 20	23, 27	Power	Power pin.

Notes:

(1) EPC1441, EPC1064, and EPC1064V devices only.

(2) The EPC1441, EPC1064, and EPC1064V devices do not support data cascading. The EPC1 and EPC1213 devices support data cascading for FLEX 8000 devices.

Active serial (AS) and multi-device sequential active serial (MD-SAS) configuration schemes can also use EPC1 or EPC1441 Configuration EPROM devices as a data source for FLEX 8000 devices.

For more information on FLEX 8000 device configuration, go to the following documents:

- *Application Note 33 (Configuring FLEX 8000 Devices)*
- *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*

Power & Operation

The following section describes Power on Reset (POR) delay, error detection, and 3.3-V and 5.0-V operation of Altera Configuration EPROMs.

Power on Reset

During initial power-up, a Power on Reset (POR) delay occurs to permit voltage levels to stabilize. When configuring a FLEX 10K or FLEX 6000 device with an EPC1 or EPC1441 device, the POR delay occurs inside the EPROM. However, when configuring a FLEX 8000 device with the EPC1213, EPC1064, or EPC1064V device, the POR delay occurs inside the FLEX 8000 device. In either case, the POR delay is a maximum of 100 ms.

Error Detection Circuitry

The EPC1 and EPC1441 Configuration EPROMs have built-in error detection circuitry. The nCS pin of the Configuration EPROM monitors the CONF_DONE pin on the FLEX 10K or FLEX 6000 device. An error condition occurs if the CONF_DONE pin does not go high after all the configuration data has been sent, or if the CONF_DONE pin goes high before the Configuration EPROM has completed sending configuration data. Upon an error condition, the Configuration EPROM will drive its OE pin low, which drives the FLEX 10K or FLEX 6000 device's nSTATUS pin low indicating an error. After an error, configuration will automatically restart if the *Auto-Restart Configuration on Frame Error* option is turned on in the MAX+PLUS II software, before project compilation, in the **Global Project Device Options** dialog box (Assign menu).

In addition, if the FLEX 10K or FLEX 6000 device detects a cyclic redundancy code (CRC) error in the data that it receives, the FLEX 10K or FLEX 6000 device may also flag the error by driving nSTATUS low. This low signal on nSTATUS will reset the Configuration EPROM, allowing reconfiguration.

3.3-V or 5.0-V Operation

EPC1 and EPC1441 devices are capable of configuring FLEX devices with an I/O supply voltage of either 3.3 V or 5.0 V. The 3.3-V or 5.0-V operation is controlled by a programming bit in the POF generated by the MAX+PLUS II software. The programming bit value is determined by the core supply voltage of the targeted device during compilation in the MAX+PLUS II software. For example, EPC1 devices are programmed to operate in 3.3-V mode when configuring FLEX 10KA and FLEX 6000A devices, which have an I/O supply voltage of 3.3 V. The EPC1 VCC pin is then connected to a 3.3-V power supply.

Designers may choose to set the Configuration EPROM for low voltage when using the MultiVolt™ feature. The MultiVolt feature allows a FLEX device to bridge between systems operating with different voltages. To set the Configuration EPROM for low voltage operation, turn on *Low-Voltage I/O* under *Device Options* in the **Global Project Device Options** dialog box (Assign menu).

For more information on FLEX 10K, FLEX 8000, and FLEX 6000 devices, go to the following documents in this data book:

- *FLEX 10K Embedded Programmable Logic Family Data Sheet*
- *FLEX 8000 Programmable Logic Device Family Data Sheet*
- *FLEX 6000 Programmable Logic Device Family Data Sheet*

MAX+PLUS II Support

The MAX+PLUS II development system provides programming support for Altera Configuration EPROMs. The MAX+PLUS II software automatically generates a POF for each Configuration EPROM in a project. In a multi-device project, the MAX+PLUS II software can combine the programming files for multiple FLEX devices into one or more Configuration EPROMs. The MAX+PLUS II software allows you to select the appropriate Configuration EPROM to most efficiently store the data for each FLEX device. Moreover, when compiling for 3.3-V devices, e.g., FLEX 10KA or FLEX 6000A devices, the MAX+PLUS II software will automatically generate the EPC1 POF with the programming bit set for 3.3-V operation.

The POF includes a preamble, cyclic redundancy code (CRC), and synchronization data that allow the POF to be used in a serial bitstream. The POF is programmed into the Configuration EPROM with the MAX+PLUS II software and a Configuration EPROM programming adapter. Many programming hardware manufacturers support programming of Configuration EPROMs.

For more information on programming hardware, see the *Altera Programming Hardware Data Sheet* and *Programming Hardware Manufacturers* in this data book.

Operating Conditions

The following tables provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for Configuration EPROM devices.

Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground, *Note (2)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or ground current			50	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			250	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage for 5.0-V operation	*Notes (3), (4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for 3.3-V operation	*Notes (3), (4)*	3.0 (3.0)	3.6 (3.6)	V
V_I	Input voltage	With respect to ground, *Note (2)*	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
t_R	Input rise time			20	ns
t_F	Input fall time			20	ns

DC Operating Conditions *Note (5), (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	5.0-V mode high-level TTL output voltage	I_{OH} = –4 mA DC, *Note (7)*	2.4		V
	3.3-V mode high-level CMOS output voltage	I_{OH} = –0.1 mA DC, *Note (7)*	V_{CC} – 0.2		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (7)*		0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or ground	–10	10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or ground	–10	10	µA

EPC1213, EPC1064 & EPC1064V Device I_{CC} Supply Current Values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			100	200	µA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 6 MHz		10	50	mA

EPC1 Device I_{CC} Supply Current Values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			50	100	µA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 10 MHz, *Note (8)* V_{CC} = 5.0 V		30	50	mA
I_{CC2}	V_{CC} supply current (during configuration)	DCLK = 5 MHz, *Note (8)* V_{CC} = 3.3 V		10	16.5	mA

EPC1441 Device I_{CC} Supply Current Values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			30	60	µA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 10 MHz, *Note (8)*		15	30	mA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 5 MHz, *Note (8)* V_{CC} = 3.3 V		5	10	mA

Capacitance *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

FLEX 10K & FLEX 6000 Device Configuration Parameters Using EPC1 & EPC1441

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CE}	OE high to first clock delay				200	ns
t_{OEZX}	OE high to data output enabled				160	ns
t_{CO}	DCLK to data out delay				30	ns
t_{MCH}	DCLK high time for the first device in the configuration chain		30	50	150	ns
t_{MCL}	DCLK low time for the first device in the configuration chain		30	50	150	ns
t_{SCH}	DCLK high time for subsequent devices		30			ns
t_{SCL}	DCLK low time for subsequent devices		30			ns
t_{CASC}	CLK rising edge to nCASC				20	ns
t_{CCA}	nCS to nCASC cascade delay				10	ns
f_{CDOE}	CLK to data enable/disable				30	ns
t_{OEC}	OE low to CLK disable delay				45	ns
t_{NRCAS}	OE low (reset) to nCASC delay				25	ns
t_{NRR}	OE low time (reset) minimum		100			ns

FLEX 8000 Device Configuration Parameters Using EPC1, EPC1441, EPC1213, EPC1064 & EPC1064V

			EPC1064V		EPC1064 EPC1213		EPC1 EPC1441		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{OEZX}	OE high to DATA output enabled			75		50		50	ns
t_{CSZX}	nCS low to DATA output enabled			75		50		50	ns
t_{CSXZ}	nCS high to DATA output disabled			75		50		50	ns
t_{CSS}	nCS low setup time to first DCLK rising edge		150		100		50		ns
t_{CSH}	nCS low hold time after DCLK rising edge		0		0		0		ns
t_{DSU}	Data setup time before rising edge on DCLK		75		50		50		ns
t_{DH}	Data hold time after rising edge on DCLK		0		0		0		ns
t_{CO}	DCLK to DATA out delay			100		75		75	ns
t_{CK}	Clock period		240		160		100		ns
f_{CK}	Clock frequency			4		6		10	MHz
t_{CL}	DCLK low time		120		80		50		ns
t_{CH}	DCLK high time		120		80		50		ns
t_{XZ}	OE low or nCS high to DATA output disabled			75		50		50	ns
t_{OEW}	OE pulse width to guarantee counter reset		150		100		100		ns
t_{CASC}	Last DCLK + 1 to nCASC low delay			90		60		50	ns
t_{CKXZ}	Last DCLK + 1 to DATA tri-state delay			75		50		50	ns
t_{CEOUT}	nCS high to nCASC high delay			150		100		100	ns

Notes to tables:

(1) See *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) These values are specified under the "Recommended Operating Conditions" on page 477.
(7) The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to low-level TTL output current.
(8) Maximum DCLK for EPC1 and EPC1441 devices is 10 MHz when V_{CC} is 5.0 V and 5 MHz when V_{CC} is 3.3 V.
(9) Capacitance is sample-tested only.