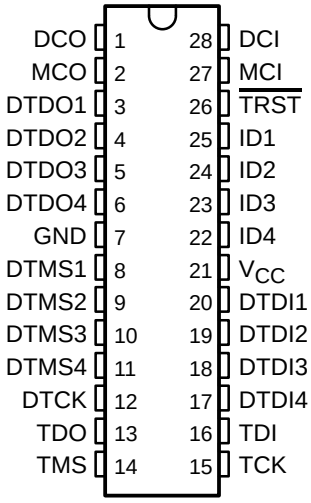
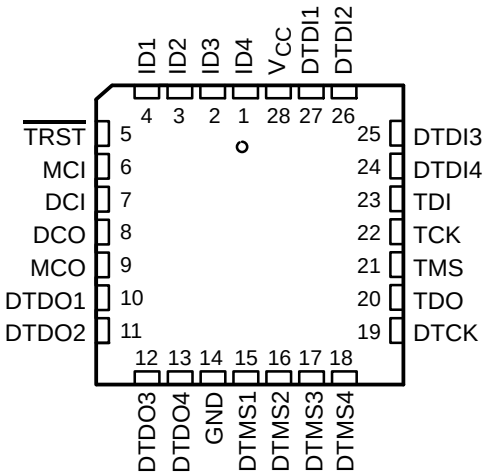
- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Serial Test Bus**
- **Allow Partitioning of System Scan Paths**
- **Can Be Cascaded Horizontally or Vertically**
- **Select Up to Four Secondary Scan Paths to Be Included in a Primary Scan Path**
- **Include 8-Bit Programmable Binary Counter to Count or Initiate Interrupt Signals**
- **Include 4-Bit Identification Bus for Scan-Path Identification**
- **Inputs Are TTL Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

SN54ACT8997 . . . JT PACKAGE
SN74ACT8997 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ACT8997 . . . FK PACKAGE
(TOP VIEW)



description

The ’ACT8997 are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of components facilitates testing of complex circuit-board assemblies.

The ’ACT8997 enhance the scan capability of TI’s SCOPE™ family by allowing augmentation of a system’s primary scan path with secondary scan paths (SSPs), which can be individually selected by the ’ACT8997 for inclusion in the primary scan path. These devices also provide buffering of test signals to reduce the need for external logic.

By loading the proper values into the instruction register and data registers, the user can select up to four SSPs to be included in a primary scan path. Any combination of the SSPs can be selected at a time. Any of the device’s six data registers or the instruction register can be placed in the device’s scan path, i.e., placed between test data input (TDI) and test data output (TDO) for subsequent shift and scan operations.

All operations of the device except counting are synchronous to the test clock pin (TCK). The 8-bit programmable up/down counter can be used to count transitions on the device condition input (DCI) pin and output interrupt signals via the device condition output (DCO) pin. The device can be configured to count on either the rising or falling edge of DCI.

The test access port (TAP) controller is a finite-state machine compatible with IEEE Standard 1149.1.

The SN54ACT8997 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ACT8997 is characterized for operation from 0°C to 70°C.

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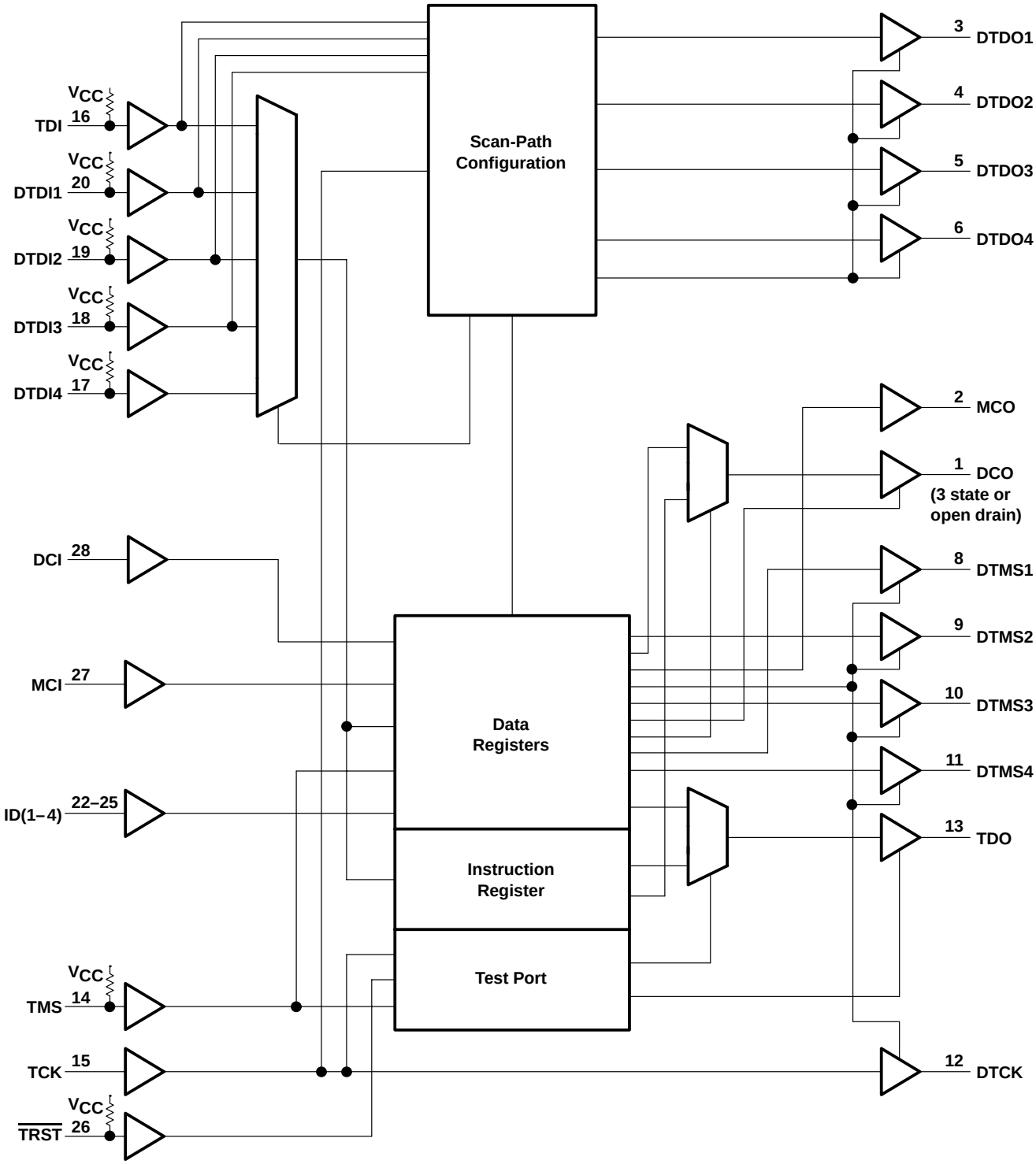
functional block diagram



Pin numbers shown are for the DW, JT, and NT packages.

functional block description

The ’ACT8997 is intended to link secondary scan paths for inclusion in a primary scan path. Any combination of the four secondary scan paths can be linked, or the device can be bypassed entirely.

The least-significant bit (LSB) of any value scanned into any register of the device is the first bit shifted in (nearest to TDO). The most-significant bit (MSB) is the last bit shifted in (nearest to TDI).

The ’ACT8997 is divided into functional blocks as detailed below.

test port

The test port decodes the signals on TCK, TMS, and $\overline{\text{TRST}}$ to control the operation of the circuit. The test port includes a TAP controller that issues the proper control instructions to the data registers according to the IEEE Standard 1149.1 protocol. The TAP controller state diagram is shown in Figure 1.

instruction register

The instruction register (IR) is an 8-bit-wide serial-shift register that issues commands to the device. Data is input to the instruction register via TDI (or one of the DTDI pins) and shifted out via TDO. All device operations are initiated by loading the proper instruction or sequence of instructions into the IR.

data registers

Six parallel data registers are included in the ’ACT8997: bypass, control, counter, boundary-scan, ID-bus, and select. The ID bus register is a part of the boundary-scan register. Each data register is serially loaded via TDI or DTDI and outputs data via TDO. Table 1 summarizes the registers in the ’ACT8997.

scan-path-configuration circuit

This circuit decodes bits in the select and control registers to determine which, if any, of the secondary scan paths are to be included in the primary scan path.

Table 1. Register Summary

REGISTER NAME	LENGTH (BITS)	FUNCTION
Instruction	8	Issue command information to the device
Control	10	Configuration and enable control
Counter	8	Count events on DCI, output interrupts via DCO
Select	8	Select one or more secondary scan paths
Boundary Scan	10	Capture and force test data at device periphery
ID Bus	4	Provide subsystem identification code
Bypass	1	Remove the ’ACT8997 from the scan path

Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
DCI	I	Device condition input. DCI receives interrupt and protocol signals from the secondary scan path(s). When the counter register is instructed to count up or down, DCI is configured as the counter clock.
DCO	O	Device condition output. DCO is configured by the control register to output protocol and interrupt signals and can be configured by the control register to output an error signal if the instruction register is loaded with an invalid value. DCO is further configured by the control register as: Active high or active low (reset condition = active low) Open drain or 3 state (reset condition = open drain)
DTCK	O	Device test clock. DTCK outputs the buffered test clock TCK to the secondary scan path(s).
DTDI1 DTDI2 DTDI3 DTDI4	I	Device test data input 1–4. DTDI1–DTDI4 receive the serial test data output(s) of the selected secondary scan path(s). An internal pullup forces DTDI1–DTDI4 to a high logic level if it is left unconnected.
DTDO1 DTDO2 DTDO3 DTDO4	O	Device test data output 1–4. These outputs send serial test data to the TDI input(s) of the secondary scan path(s).
DTMS1 DTMS2 DTMS3 DTMS4	O	Device test mode select 1–4. Any combination of these four outputs can be selected to follow TMS to direct the secondary scan path(s) through the TAP controller states in Figure 1. The unselected DTMS outputs can be set independently to a high or low logic level. The TMS circuit monitors input from the select register to determine the configuration of the DTMS outputs.
GND		Ground
IDI ID2 ID3 ID4	I	Identification 1–4. This 4-bit data bus can be hardwired to provide identification of the subsystem under test. The value present on the bus can be scanned out through the boundary scan or ID bus registers.
MCI	I	Master condition input. MCI receives interrupt and protocol signals from a primary bus controller (PBC). The level on MCI is buffered and output on MCO.
MCO	O	Master condition output. MCO transmits interrupt and protocol signals to the secondary scan path(s).
TCK	I	Test clock. One of four terminals required by IEEE Standard 1149.1. All operations of the ’ACT8997 except for the count function are synchronous to TCK. Data on the device inputs is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI	I	Test data input. One of four terminals required by IEEE Standard 1149.1. TDI is the serial input for shifting information into the instruction register or selected data register. TDI is typically driven by the TDO of the PBC. An internal pullup forces TDI to a high level if left unconnected.
TDO	O	Test data output. One of four terminals required by IEEE Standard 1149.1. TDO is the serial output for shifting information out of the instruction register or selected data register. TDO is typically connected to the TDI of the next scannable device in the primary scan path.
TMS	I	Test mode select. One of four terminals required by IEEE Standard 1149.1. The level of TMS at the rising edge of TCK directs the ’ACT8997 through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected.
$\overline{\text{TRST}}$	I	Test reset. This active-low input implements the optional reset terminal of IEEE Standard 1149.1. When asserted, $\overline{\text{TRST}}$ causes the ’ACT8997 to go to the Test-Logic-Reset state and configure the instruction register and data registers to their power-up values. An internal pullup forces $\overline{\text{TRST}}$ to a high level if left unconnected.
V_{CC}		Supply voltage

state diagram description

The TAP proceeds through the states in Figure 1 according to IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow) and ten unstable states in the diagram. A stable state is a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to manipulate a data register and one to manipulate the instruction register. No more than one register can be manipulated at a time.

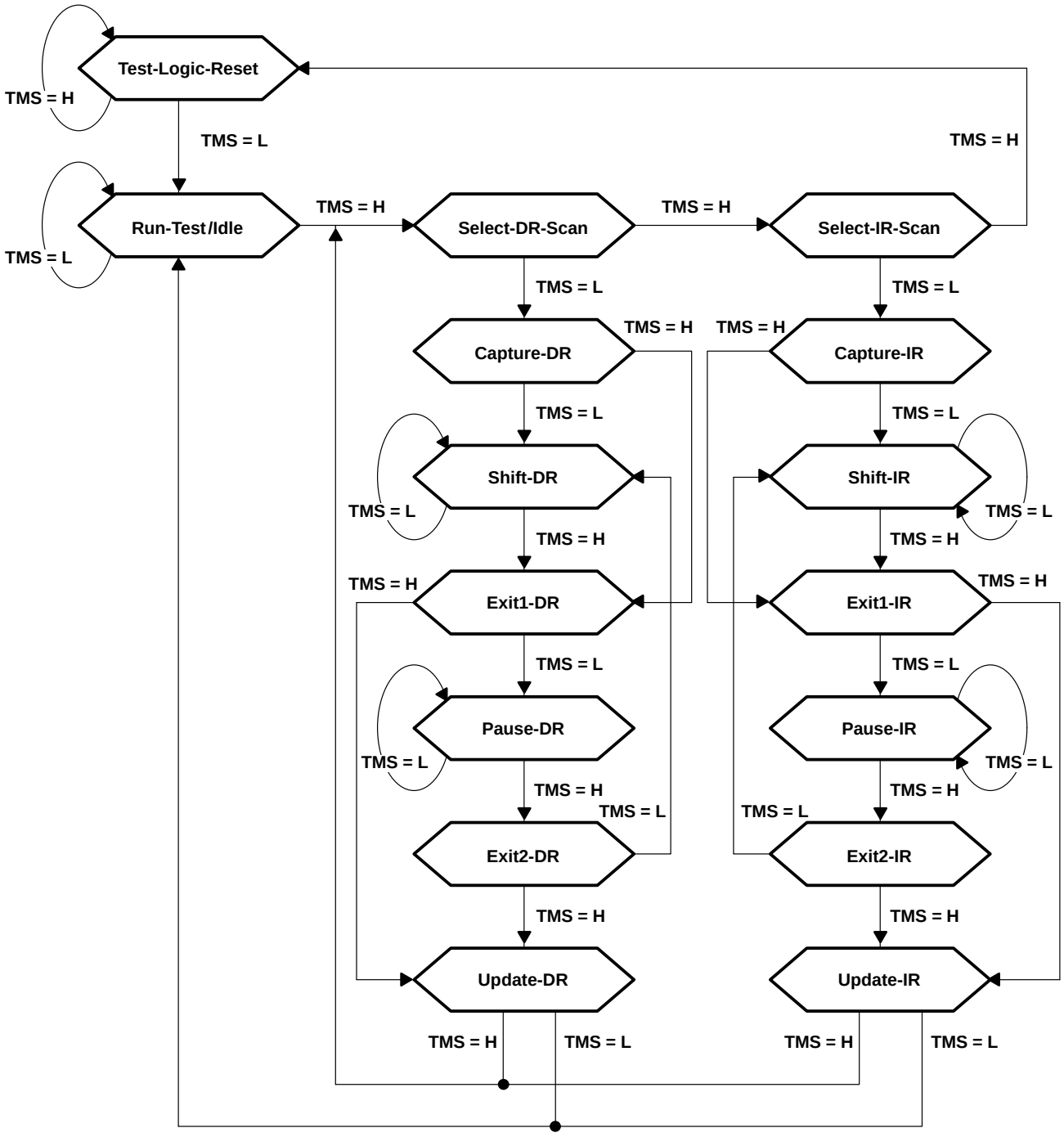


Figure 1. TAP-Controller State Diagram

Test-Logic-Reset

In this state, the test logic is inactive and an internal reset signal is applied to all registers in the device. During device operation, the TAP returns to this state in no more than five TCK cycles if the test mode select (TMS) input is high. The TMS pin has an internal pullup that forces it to a high level if it is left unconnected or if a board defect causes it to be open circuited. The device powers up in the Test-Logic-Reset state.

Run-Test/Idle

The TAP must pass through this state before executing any test operations. The TAP may retain this state indefinitely, and no registers are modified while in Run-Test/Idle. The 8-bit programmable up/down counter can be operated in this state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states; the TAP exits either of them on the next TCK cycle.

Capture-DR

The selected data register is placed in the scan path (i.e., between TDI and TDO). Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK, causing the TAP state to change.

Shift-DR

In this state, data is serially shifted through the selected data register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). On the falling edge of TCK in Shift-DR, TDO goes from the high-impedance state to the active state. TDO enables to the value present in the least-significant bit of the selected data register.

Exit1-DR, Exit2-DR

These are temporary states that end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-DR to Exit-DR. TDO changes from the active state to the high-impedance state on the falling edge of TCK in Exit1-DR.

Pause-DR

The TAP can remain in this state indefinitely. The Pause-DR state suspends and resumes shift operations without loss of data.

Update-DR

If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated only during this state.

Capture-IR

The instruction register is preloaded with the IR status word (see Table 4) and placed in the scan path.

Shift-IR

In this state, data is serially shifted through the instruction register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). On the falling edge of TCK in Shift-IR, TDO goes from the high-impedance state to the active state, and will enable to a high level.

Exit1-IR, Exit2-IR

These are temporary states that end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-IR to Exit1-IR. TDO changes from the active state to the high-impedance state on the falling edge of TCK in Exit1-IR.

Pause-IR

The TAP can remain in this state indefinitely. The Pause-IR state suspends and resumes shift operations without loss of data.

Update-IR

In this state, the latches shadowing the instruction register are updated with the new instruction.

instruction-register description

The instruction register (IR) is an 8-bit serial register that outputs control signals to the device. Table 2 lists the instructions implemented in the ’ACT8997 and the data register selected by each instruction. The MSB of the IR is an even-parity bit. If the value scanned into the IR during Shift-IR does not contain even parity, an error signal ($\overline{\text{IRERR}}$) is generated internally as shown in Table 3. The ’ACT8997 can be configured to output $\overline{\text{IRERR}}$ via DCO if the TAP enters the Pause-IR state.

During the Capture-IR state, the IR status word is loaded.The IR status word contains information about the most recently loaded value of the instruction register and the logic level present at the DCI input. The IR status word is encoded as shown in Table 4. Figure 2 shows the order of scan for the IR.

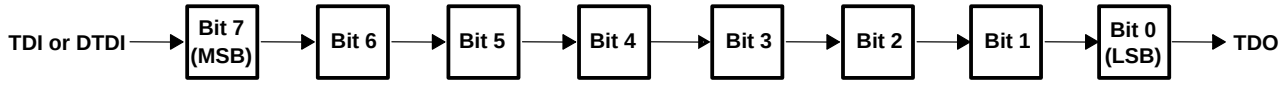


Figure 2. Instruction-Register Bits and Order of Scan

Table 2. Instruction-Register Opcodes

BINARY CODE BIT 7 → BIT 0 MSB → LSB	HEX VALUE	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
00000000	00	EXTEST	Boundary scan	Boundary scan	Test
10000001	81	BYPASS†	Bypass scan	Bypass	Normal
10000010	82	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
00000011	03	INTEST	Boundary scan	Boundary scan	Test
10000100	84	BYPASS†	Bypass scan	Bypass	Normal
00000101	05	BYPASS†	Bypass scan	Bypass	Normal
00000110	06	BYPASS†	Bypass scan	Bypass	Normal
10000111	87	BYPASS†	Bypass scan	Bypass	Normal
10001000	88	COUNT	Count	Bypass	Normal
00001001	09	COUNT	Count	Bypass	Normal
00001010	0A	BYPASS†	Bypass scan	Bypass	Normal
10001011	8B	BYPASS†	Bypass scan	Bypass	Normal
00001100	0C	BYPASS†	Bypass scan	Bypass	Normal
10001101	8D	BYPASS	Bypass scan	Bypass	Normal
10001110	8E	SCANCN	Control register scan	Control	Normal
00001111	0F	SCANCN	Control register scan	Control	Normal
11111010	FA	SCANCNT	Counter scan	Counter	Normal
01111011	7B	READCNT	Counter read	Counter	Normal
11111100	FC	SCANIDB	ID bus register scan	ID bus	Normal
01111101	7D	READIDB	ID bus register read	ID bus	Normal
01111110	7E	SCANSEL	Select register scan	Select	Normal
All others		BYPASS	Bypass scan	Bypass	Normal

† A SCOPE opcode exists but is not supported by the 'ACT8997.

Table 3. $\overline{\text{IRERR}}$ Function Table

NO. OF INSTRUCTION REGISTER BITS = 1	$\overline{\text{IRERR}}$
0, 2, 4, 6, 8	1
1, 3, 5, 7	0

Table 4. Instruction-Register Status Word

IR BIT	VALUE†
7	$\overline{\text{IRERR}}$ (see Table 3)
6	0
5	0
4	0
3	DCI (1 = active, 0 = inactive)
2	0
1	0
0	1

† This value is loaded in the instruction register during the Capture-IR TAP state.

instruction-register opcode description

The operation of the 'ACT8997 is dependent on the instruction loaded into the IR. Each instruction selects one of the data registers to be placed between TDI or DTDI and TDO during the Shift-DR TAP state. All the required instructions of IEEE Standard 1149.1 are implemented in the 'ACT8997.

boundary scan

This instruction implements the required EXTEST and optional INTEST operations of IEEE Standard 1149.1. The boundary-scan register (which includes the ID-bus register) is placed in the scan path. Data appearing at input pins included in the boundary-scan register is captured. Data previously loaded into the output pins included in the boundary-scan register is forced through the outputs.

bypass scan

This instruction implements the required BYPASS operation of IEEE Standard 1149.1. The bypass register is placed in the scan path and preloads with a logic 0 during Capture-DR.

sample boundary

This instruction implements the required SAMPLE/PRELOAD operation of IEEE Standard 1149.1. The boundary-scan register is placed in the scan path, and data appearing at the inputs and outputs included in the boundary-scan register is sampled on the rising edge of TCK in Capture-DR.

count

The counter register begins counting on each DCI transition. The count begins from the value present in the register before the count instruction was loaded. The counter can be configured by the control register to count up or down on either the low-to-high or high-to-low transition of DCI. Counting occurs only while in the Run-Test/Idle TAP state.

control-register scan

The control register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

counter-register scan

The counter register is placed in the scan path. During Capture-DR, the current value of the counter is loaded in the counter register. At Update-DR, the newly shifted value is preloaded to the counter.

counter-register read

The counter register is placed in the scan path. During Capture-DR, the prior preload value of the counter is loaded into the counter register. At Update-DR, the newly shifted value is preloaded to the counter.

ID-bus-register scan

The ID-bus register (a subset of the boundary-scan register) is placed in the scan path for a subsequent shift operation. The data appearing on the ID bus is loaded into the ID-bus register on the rising edge of TCK in Capture-DR.

ID-bus-register read

The ID-bus register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

select-register scan

The select register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

control register description

The control register (CTLR) is a 10-bit serial register that controls the enable and select functions of the ’ACT8997. A reset operation forces all bits to a low logic level. The contents of the CTLR are latched and decoded during the Update-DR TAP state. The specific function of each bit is listed in Table 5. The enable and select functions of the CTLR bits are mapped as follows:

Table 5. Control-Register Bit Mapping

BIT	VALUE	FUNCTION
9	0	Configure counter to count up
	1	Configure counter to count down
8	0	Do not stop counting when the count reaches 00000000
	1	Stop counting when the count reaches 00000000 (count down only)
7	0	Configure DCO as an active-low output
	1	Configure DCO as an active-high output
6, 5	00	DCO = Inactive (level depends on CTLR bit 7)
	01	DCO = $\overline{\text{IRERR}}$
	10	DCO = $\overline{\text{CE}}$, an internal logic 0 generated when the count is 00000000 (count down) or 11111111 (count up)
	11	DCO = DCI
4	0	Do not mask $\overline{\text{IRERR}}$ from DCO
	1	Mask $\overline{\text{IRERR}}$ from DCO
3	0	Configure DCO as an open-drain output
	1	Configure DCO as a 3-state output
2	0	Disable DCO
	1	Enable DCO
1	0	Configure DCI as an active-low input
	1	Configure DCI as an active-high input
0	0	Enable DTCK, DTDO(1–4), and DTMS(1–4) [outputs DTDO(1–4) depend on select register (see Table 7)]
	1	Disable DTCK, DTDO(1–4), and DTMS(1–4)

Bit 9 – $\overline{\text{Up}}$/Down

This bit sets the count mode of the counter register (reset condition = count up).

Bit 8 – Latch on Zero

The counter register can be configured to stop counting when its value is 00000000 and ignore subsequent transitions on the counter clock, DCI. The latch-on-zero option is valid only in the count-down mode (reset condition = do not latch on zero). The value of this bit has no effect on the operation of the counter if CTLR bit 9 = 0.

Bit 7 – DCO Polarity Select

DCO can be configured as an active-low or active-high output (reset condition = active low).

Bit 6/Bit 5 – DCO Source Select 1/DCO Source Select 0

DCO can be used to output the $\overline{\text{IRERR}}$ signal generated by the ’ACT8997 (see Table 3). Bits 6 and 5 can be set to output $\overline{\text{IRERR}}$ via DCO on the falling edge of TCK in the Pause-IR state. DCO can also be configured to become active when the value of the counter is 00000000, to follow DCI, or be set to a static high or low level (reset condition = static high level).

Bit 4 – Parity Mask

The signal $\overline{\text{IRERR}}$ can be masked from appearing on DCO even if bits 6 and 5 are set such that it is output in the Pause-IR state (reset condition = do not mask $\overline{\text{IRERR}}$).

Bit – DCO Drive Select

DCO can be configured as either an open-drain or 3-state output (reset condition = open drain). The open-drain configuration allows multiple DCO outputs to be used in a wired-OR or wired-AND application. The 3-state configuration allows the DCO output to be connected to a bus.

Bit 2 – DCO Enable

When configured as a 3-state output, DCO can be placed in the high-impedance state (reset condition = disabled). If configured as an open-drain output and disabled, DCO outputs a high level.

Bit 1 – DCI Polarity Select

DCI can be configured as an active-low or active-high input (reset condition = active low).

Bit 0 – Device Test Pins Output Enable (active low)

DTCK, DTDO1–4, and DTMS1–4 pins can be placed in the high-impedance state (disabled) with this bit (reset condition = not disabled). If DTDO1–4 pins are not disabled using this control bit, then their drive state is dependent on the value of the select register (see Table 7).

Several CTLR bits affect the functionality of the DCO output. The DCO function table is given in Table 6. Figure 3 illustrates the order of scan for the CTLR.

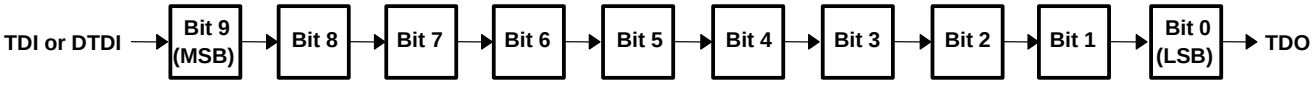


Figure 3. Control-Register Bits and Order of Scan

Table 6. DCO Function Table

DCI	INTERNAL SIGNALS†		CONTROL-REGISTER BITS‡							DCO
	$\overline{\text{IRERR}}$	$\overline{\text{CE}}$	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	
X	X	X	X	X	X	X	0	0	X	H
X	X	X	X	X	X	X	1	0	X	Z
X	X	X	0	0	0	X	X	1	X	H
X	X	X	1	0	0	X	X	1	X	L
X	X	X	0	0	1	1	X	1	X	H
X	X	X	1	0	1	1	X	1	X	L
X	0	X	0	0	1	0	X	1	X	L in Pause-IR§, H otherwise
X	1	X	0	0	1	0	X	1	X	H
X	0	X	1	0	1	0	X	1	X	H in Pause-IR§, L otherwise
X	1	X	1	0	1	0	X	1	X	L
X	X	0	0	1	0	X	X	1	X	L
X	X	0	1	1	0	X	X	1	X	H
X	X	1	0	1	0	X	X	1	X	H
X	X	1	1	1	0	X	X	1	X	L
L	X	X	1	1	1	X	X	1	0	H
L	X	X	1	1	1	X	X	1	1	L
L	X	X	0	1	1	X	X	1	0	L
L	X	X	0	1	1	X	X	1	1	H
H	X	X	1	1	1	X	X	1	0	L
H	X	X	1	1	1	X	X	1	1	H
H	X	X	0	1	1	X	X	1	0	H
H	X	X	0	1	1	X	X	1	1	L

† These signals are generated as described elsewhere in this data sheet.
‡ The control register must contain these values after the TAP has passed through its most recent Update-DR state.
§ DCO becomes active on the falling edge of TCK as the TAP enters the Pause-IR state and becomes inactive on the falling edge of TCK as the TAP enters Exit2-IR.

select register description

The select register (SR) is an 8-bit serial register that determines which, if any, of the secondary scan paths (SSPs) will be included in the primary scan path. A reset operation forces all bits to a logic 0. The register is divided into four 2-bit sections, each of which controls one SSP. Figure 4 shows the mapping of the bits to the SSPs and the order of scan. For each SSP, the higher-order bit is the MSB and the lower-order bit is the LSB (e.g., bit 3 is the MSB of SSP2 and bit 2 is the LSB of SSP2).

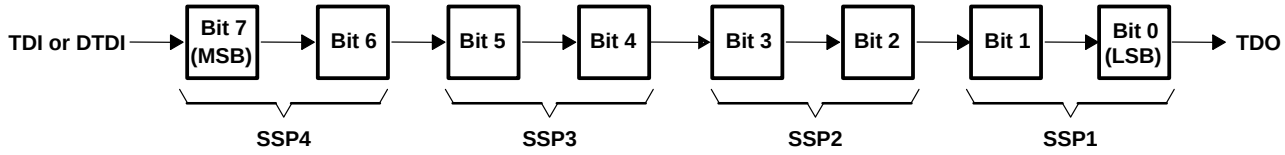


Figure 4. Select Register Bits and Order of Scan

When a new 8-bit value is loaded into the SR, the configuration of one or more DTMS pins may change. If the new value of the SR configures a DTMS pin to a static (high or low) level, it assumes that level on the falling edge of TCK in the Update-DR TAP state. This condition is independent of any previous SR configurations. If the new value of the SR forces a DTMS pin to follow TMS (i.e., select the secondary scan path) and one or more DTMS pins are currently in the TMS-follow mode, the transfer of DTMS lines occurs on the falling edge of TCK in the Update-DR TAP state. If, however, the new configuration forces a DTMS pin to follow TMS while no other DTMS pin is selected, the DTMS pin is forced low and does not begin following TMS until the falling edge of TCK in the Run-Test/Idle TAP state; therefore, when an SSP is initially selected, the TAP state should travel from Update-DR to Run-Test/Idle, not from Update-DR to Select-DR-Scan.

Although any combination of SSPs can be selected, the order of scan for each combination is fixed (see data flow description for details). The SR bit decoding is shown in Table 7.

Table 7. Select Register-Bit Decoding

MSB	LSB	DTMS SOURCE	DTDO STATUS
0	0	H	Z
0	1	L	Z
1	X	TMS	Active†

† The DTDO1–4 outputs are active only in the Shift-IR and Shift-DR TAP states.

boundary-scan register/ID-bus register description

The boundary-scan register (BSR) is a 10-bit serial register that can be used to capture data appearing at selected device inputs, force data through device outputs, and apply data to the device's internal logic. The BSR is made up of boundary-scan cells (BSCs). Table 8 lists the device signal for each of the 10 BSCs that comprise the BSR. A reset operation does not affect the contents of the BSR.

Table 8. Boundary-Scan Register Bit Mapping

BIT	TERMINAL NAME	SIGNAL DESCRIPTION
9	MCI	Master condition in
8	MCO	Master condition out
7	DCI	Device condition in
6	$\overline{\text{DCOTS}}$†	Enable control for DCO in 3-state configuration (active low)
5	$\overline{\text{DCOOD}}$†	Enable control for DCO in open-drain configuration (active low)
4	DCO	Device condition out
3	ID4	Identification bus bit 4
2	ID3	Identification bus bit 3
1	ID2	Identification bus bit 2
0	ID1	Identification bus bit 1

† This internal signal cannot be observed from the I/O terminals of the device.

The four BSCs connected to the ID(1–4) terminals form a subset of the BSR called the ID-bus register (IDBR). The IDBR can be scanned without accessing the remaining BSCs of the BSR. Figure 5 shows the order of scan for the BSR and IDBR.

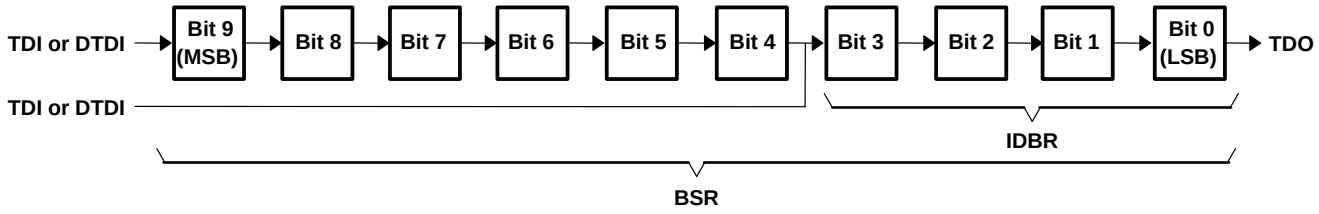


Figure 5. Boundary-Scan Register Bits and Order of Scan

bypass register description

The bypass register (BR) is a 1-bit serial register. The BR provides a means of effectively removing the 'ACT8997 from the primary scan path when it is not needed for the current test operation. Any selected secondary scan paths remain active in the primary scan path as described in the data flow description. At power up, the BR is placed in the scan path. During Capture-DR, the BR is preloaded with a low logic level. Figure 6 shows the order of scan for the bypass register.

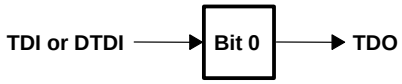


Figure 6. Bypass-Register Bit and Order of Scan

counter register description

The counter register (CNTR) is an 8-bit serial register and an associated 8-bit parallel-load up/down counter. A reset operation forces all bits of the shift register to a logic 0 but does not affect the counter. The counter can be preloaded with an initial value before counting begins, and the current value of the counter scanned out via the shift register. The CNTR can be used to count events occurring on the secondary scan path(s) using the DCI pin as a counter clock and can output interrupt signals via DCO when the count has reached its end value.

An internal signal, $\overline{CE}$, is generated as a logic 0 when the count reaches its end value (i.e., 00000000 for count down, 11111111 for count up). For any other count value, $\overline{CE}$ is a logic 1. Many of the features of the CNTR are configured by a bit in the CTLR including:

Count direction up or down (control register bit 9; reset condition = count up).

Stop counting upon counting down to 00000000 (control register bit 8; reset condition = do not latch on zero).

Output $\overline{CE}$ signals at DCO (control register bits 5 and 6; reset condition = do not output $\overline{CE}$ at DCO).

Edge of DCI on which to trigger (control register bit 1; reset condition = positive edge).

Figure 7 shows the order of scan for the CNTR.

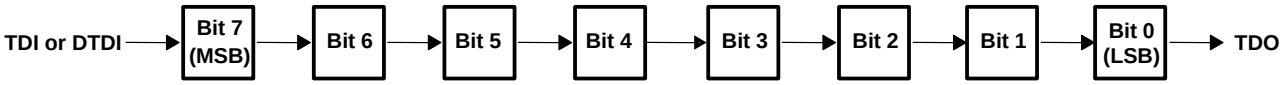


Figure 7. Counter-Register Bits and Order of Scan

data flow description

The direction of serial-data flow in the 'ACT8997 is dependent on the current instruction and value of the SR. Figure 8 shows the data flow when one or more SSPs have been selected. When more than one SSP has been selected, the order of scan is determined by which SSPs have been selected as shown in Table 9. The 'ACT8997 add one bit of delay from TDI or DTDI to DTDO.

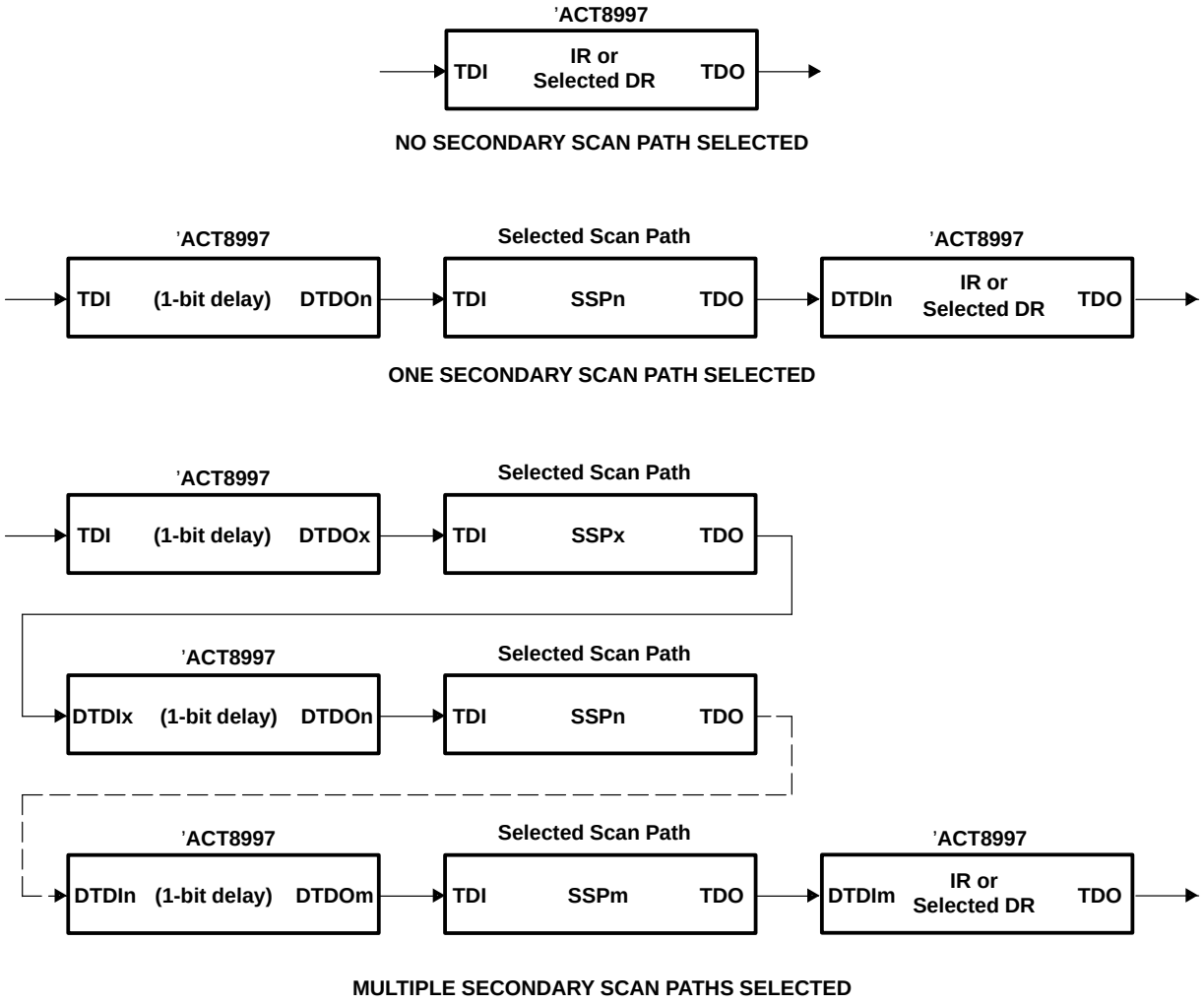


Figure 8. Data Flow in the 'ACT8997

Table 9. Scan-Path Configurations

SR BIT				SSP CONFIGURATION				SCAN-PATH CONFIGURATION†‡
7	5	3	1	SSP4	SSP3	SSP2	SSP1	
0	0	0	0	Inactive	Inactive	Inactive	Inactive	TDI–SPL–TDO
0	0	0	1	Inactive	Inactive	Inactive	Active	TDI–(1)–SSP1–SPL–TDO
0	0	1	0	Inactive	Inactive	Active	Inactive	TDI–(1)–SSP2–SPL–TDO
0	0	1	1	Inactive	Inactive	Active	Active	TDI–(1)–SSP1–(1)–SSP2–SPL–TDO
0	1	0	0	Inactive	Active	Inactive	Inactive	TDI–(1)–SSP3–SPL–TDO
0	1	0	1	Inactive	Active	Inactive	Active	TDI–(1)–SSP1–(1)–SSP3–SPL–TDO
0	1	1	0	Inactive	Active	Active	Inactive	TDI–(1)–SSP2–(1)–SSP3–SPL–TDO
0	1	1	1	Inactive	Active	Active	Active	TDI–(1)–SSP1–(1)–SSP2–(1)–SSP3–SPL–TDO
1	0	0	0	Active	Inactive	Inactive	Inactive	TDI–(1)–SSP4–SPL–TDO
1	0	0	1	Active	Inactive	Inactive	Active	TDI–(1)–SSP1–(1)–SSP4–SPL–TDO
1	0	1	0	Active	Inactive	Active	Inactive	TDI–(1)–SSP2–(1)–SSP4–SPL–TDO
1	0	1	1	Active	Inactive	Active	Active	TDI–(1)–SSP1–(1)–SSP2–(1)–SSP4–SPL–TDO
1	1	0	0	Active	Active	Inactive	Inactive	TDI–(1)–SSP3–(1)–SSP4–SPL–TDO
1	1	0	1	Active	Active	Inactive	Active	TDI–(1)–SSP1–(1)–SSP3–(1)–SSP4–SPL–TDO
1	1	1	0	Active	Active	Active	Inactive	TDI–(1)–SSP2–(1)–SSP3–(1)–SSP4–SPL–TDO
1	1	1	1	Active	Active	Active	Active	TDI–(1)–SSP1–(1)–SSP2–(1)–SSP3–(1)–SSP4–SPL–TDO

† The scan-path configuration is the order of scan, beginning with the TDI of the 'ACT8997 and ending with the TDO of the 'ACT8997.
‡ A (1) indicates one bit of delay through the 'ACT8997. SPL indicates the selected scan register within the 'ACT8997.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package . . . . . 1.7 W
NT package . . . . . 1.3 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions

			SN54ACT8997		SN74ACT8997		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	TDO, DTDO(1–4), MCO		–7		–10	mA
		DTMS(1–4), DCO (3 state), DTCK		–11		–16	
I_{OL}	Low-level output current	TDO, DTDO(1–4), MCO		7		10	mA
		DCO (open drain or 3 state)		11		16	
		DTMS(1–4)		16		24	
		DTCK		32		48	
T_A	Operating free-air temperature		–55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ACT8997		SN74ACT8997			UNIT
				MIN	MAX	MIN	TYP†	MAX	
V_{OH}	TDO, DTDO(1–4), MCO	V_{CC} = 4.5 V	I_{OH} = –7 mA	3.6					V
			I_{OH} = –10 mA			3.7			
	DTMS(1–4), DCO (3 state), DTCK	V_{CC} = 4.5 V	I_{OH} = –11 mA	3.6					
			I_{OH} = –16 mA			3.7			
V_{OL}	TDO, DTDO(1–4), MCO	V_{CC} = 4.5 V	I_{OL} = 7 mA		0.5				V
			I_{OL} = 10 mA					0.5	
	DCO (open drain or 3 state)	V_{CC} = 4.5 V	I_{OL} = 11 mA		0.5				
			I_{OL} = 16 mA					0.5	
	DTMS(1–4)	V_{CC} = 4.5 V	I_{OL} = 16 mA		0.5				
			I_{OL} = 24 mA					0.5	
	DTCK	V_{CC} = 4.5 V	I_{OL} = 32 mA		0.5				
			I_{OL} = 48 mA					0.5	
I_{OZ}‡	DTDO(1–4), DTMS(1–4), DCO, DTCK	V_{CC} = 5.5 V,	V_O = V_{CC} or GND		±10			±5	µA
I_{OH}	DCO (open drain)	V_{CC} = 5.5 V,	V_O = V_{CC}		20			10	µA
I_I	MCI, DCI, TCK, ID(1–4)	V_{CC} = 5.5 V,	V_I = V_{CC} or GND		±1			±1	µA
	TDI, DTDI(1–4), TMS, $\overline{TRST}$	V_{CC} = 5.5 V	V_I = V_{CC}		±1			±1	
			V_I = GND	–0.1	–20	–0.1		–20	
I_{CC}		V_{CC} = 5.5 V,	V_I = V_{CC} or GND, I_O = 0		100			100	µA
ΔI_{CC}§		V_{CC} = 5.5 V, One input at V_I = 3.4 V, Other inputs at V_{CC} or GND			1			1	mA
C_i		V_I = V_{CC} or GND					6		pF
C_o	DCO	V_O = V_{CC} or GND					15		pF
C_o	All other outputs	V_O = V_{CC} or GND					10		pF

† Typical values are at V_{CC} = 5 V.
‡ For I/O pins, the parameter I_{OZ} includes the input-leakage current. For the DCO pin, the parameter I_{OZ} includes the open-drain output-leakage current.
§ This is the increase in supply current for each input being driven at TTL levels rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

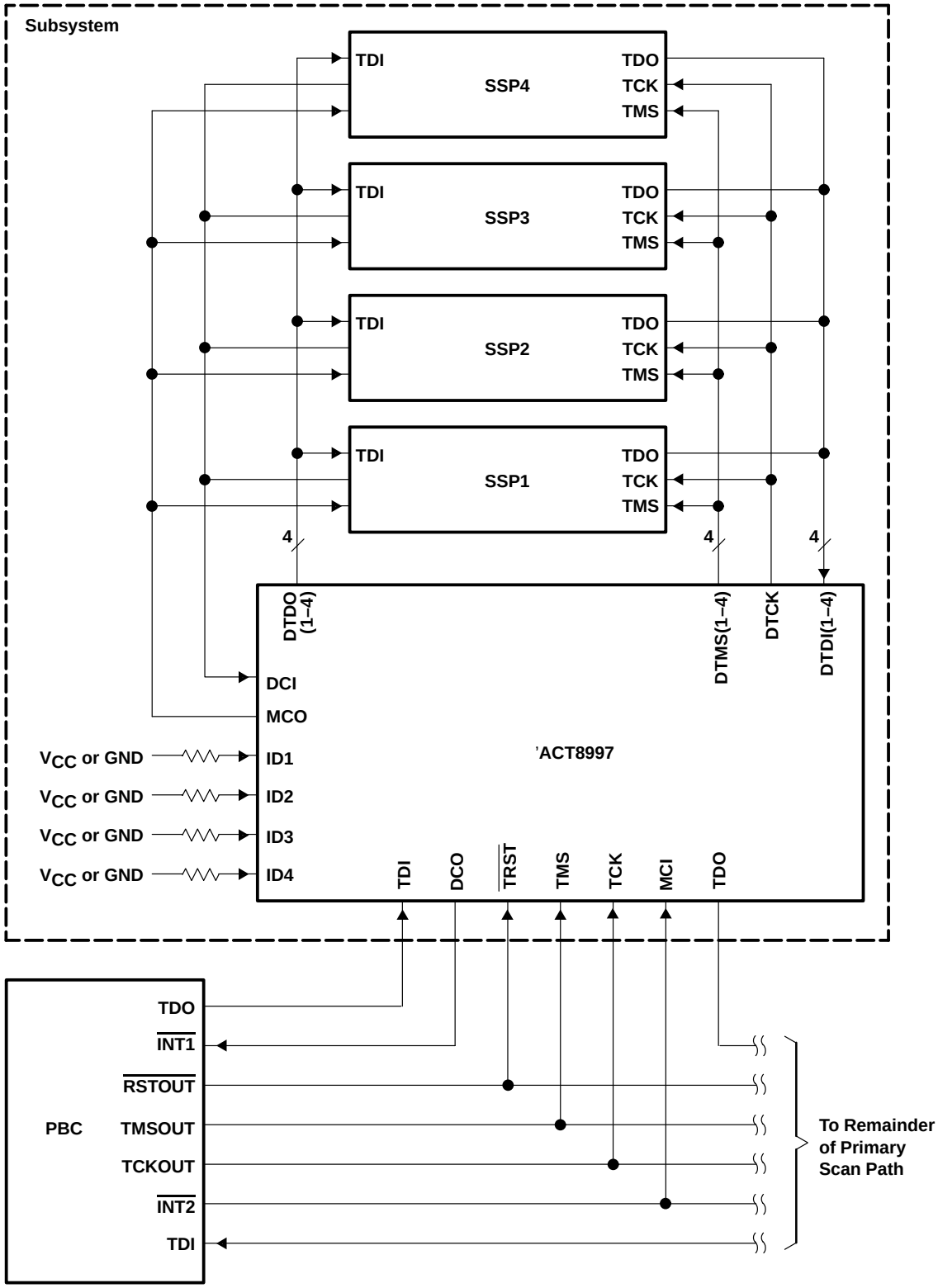
			SN54ACT8997		SN74ACT8997		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	20	0	20	MHz
		DCI (count mode)	0	20	0	20	
t_w	Pulse duration	TCK high or low	12		12		ns
		DCI high or low (count mode)	7		7		
		$\overline{\text{TRST}}$ low	7		7		
t_{su}	Setup time	TMS before TCK↑	8		8		ns
		TDI before TCK↑	9		9		
		Any DTDI before TCK↑	7		7		
		MCI before TCK↑	3		3		
		DCI before TCK↑	3		2		
		Any ID before TCK↑	2		2		
t_h	Hold time	TMS after TCK↑	2		2		ns
		TDI after TCK↑	2		2		
		Any DTDI after TCK↑	2		2		
		MCI after TCK↑	4		4		
		DCI after TCK↑	4		4		
		Any ID after TCK↑	4		4		
t_d	Delay time	Power up to TCK↑	100*		100		ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

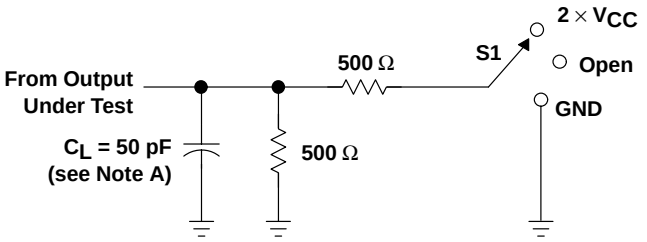
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 9)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT8997		SN74ACT8997		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	TCK		20		20		MHz
	DCI (count mode)		20		20		
t_{PLH}	TCK	DTCK	2	14	3	12	ns
t_{PHL}			2	16	3	14	
t_{PLH}	TCK↓	TDO	7	28	9	25	ns
t_{PHL}			7	26	9	24	
t_{PLH}	TCK↓	Any DTDO	7	27	9	25	ns
t_{PHL}			7	26	9	24	
t_{PLH}	TCK↓	Any DTMS	9	31	11	29	ns
t_{PHL}			9	31	12	29	
t_{PLH}	TCK↓	DCO (open drain)	9	33	12	31	ns
		DCO (3 state)	9	32	12	30	
t_{PHL}	TCK↓	DCO (open drain)	9	34	12	32	
		DCO (3 state)	9	31	12	29	
t_{PLH}	TMS	Any DTMS	4	21	6	19	ns
t_{PHL}			5	23	7	21	
t_{PLH}	MCI	MCO	5	23	7	20	ns
t_{PHL}			5	22	7	20	
t_{PLH}	DCI	DCO (open drain)	9	30	11	27	ns
		DCO (3 state)	6	29	10	26	
t_{PHL}	DCI	DCO (open drain)	7	29	10	25	
		DCO (3 state)	6	26	9	23	
t_{PHZ}	TCK↓	TDO	3	17	5	15	ns
t_{PLZ}			3	16	4	14	
t_{PHZ}	TCK↓	Any DTDO	5	19	5	17	ns
t_{PLZ}			5	20	7	18	
t_{PHZ}	TCK↓	Any DTMS	6	23	7	21	ns
t_{PLZ}			6	28	9	26	
t_{PHZ}	TCK↓	DCO	6	23	9	21	ns
t_{PLZ}			6	24	9	22	
t_{PZH}	TCK↓	TDO	8	30	10	27	ns
t_{PZL}			8	31	10	28	
t_{PZH}	TCK↓	Any DTDO	9	31	11	28	ns
t_{PZL}			9	33	11	30	
t_{PZH}	TCK↓	Any DTMS	8	31	11	29	ns
t_{PZL}			10	35	13	33	
t_{PZH}	TCK↓	DCO	9	37	14	35	ns
t_{PZL}			8	35	13	32	

APPLICATION INFORMATION

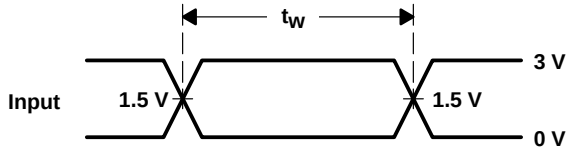


PARAMETER MEASUREMENT INFORMATION

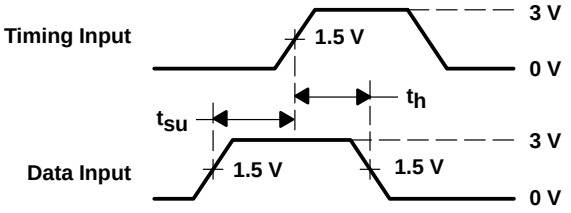


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

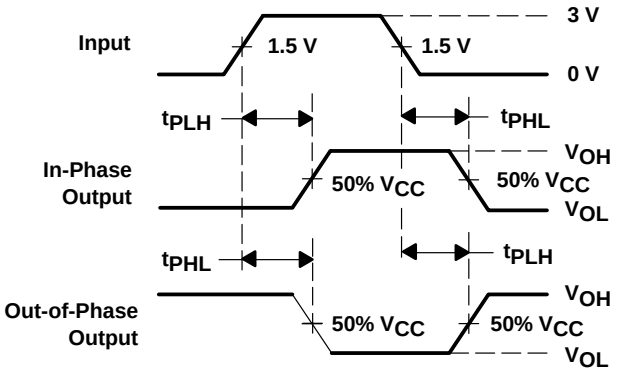
LOAD CIRCUIT



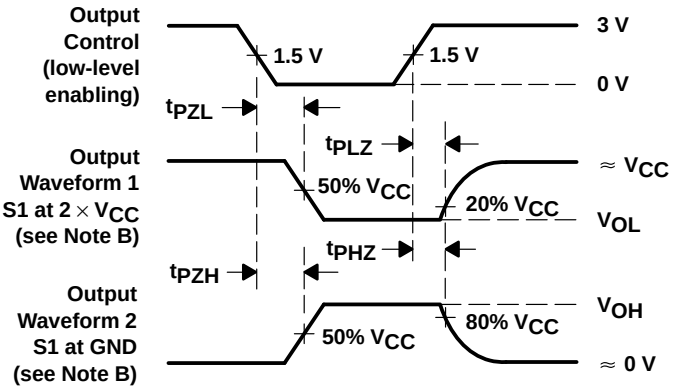
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns. Pulse polarity may be either high-to-low-to-high or a low-to-high-to-low.
D. The outputs are measured one at a time with one transition per measurement.

Figure 9. Load Circuit and Voltage Waveforms

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