B. Winer
Collaboration Meeting
July 24-25th, 1997

# XFTII Status

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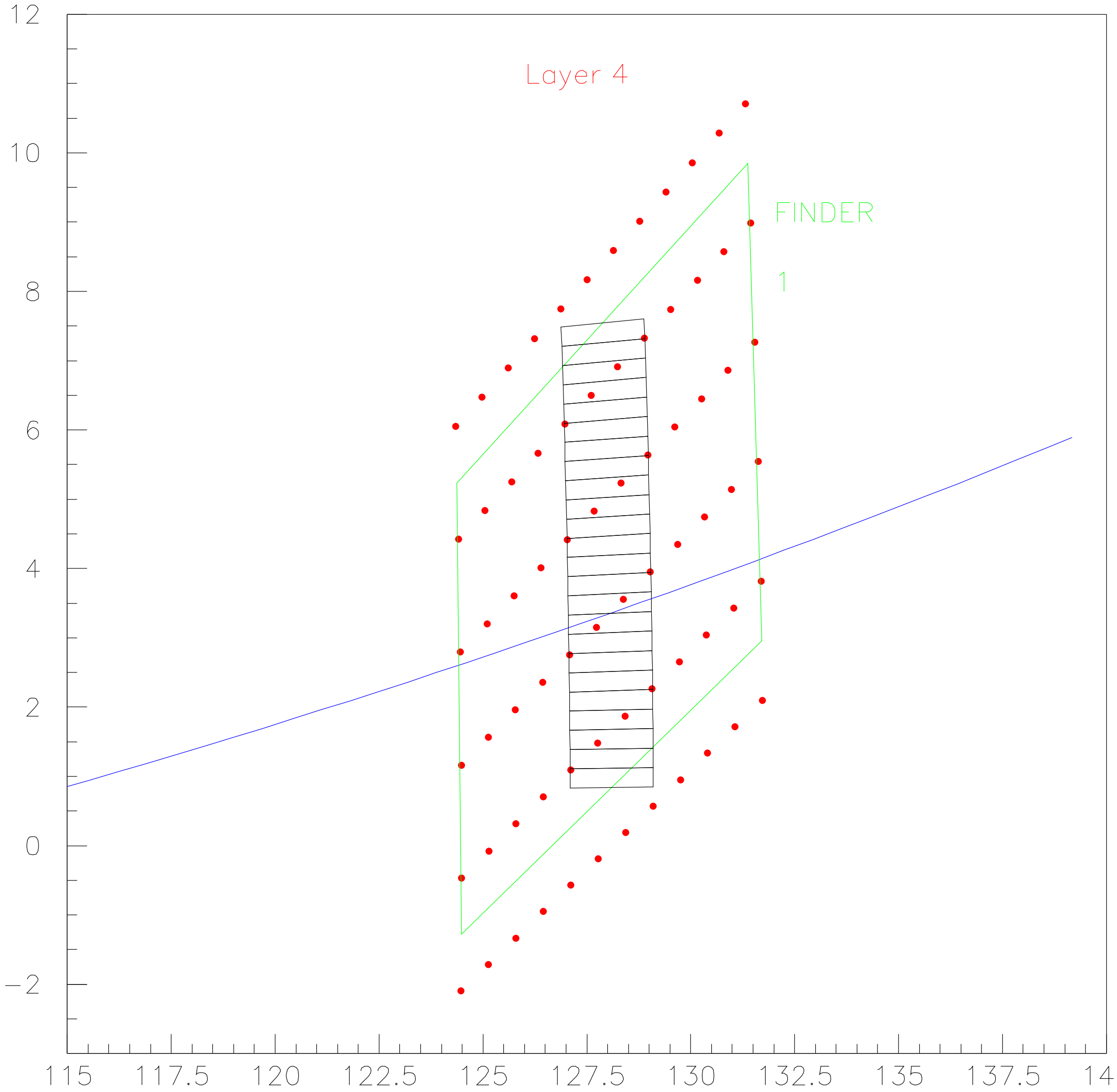
For more information see the XFT Web page and talk by Richard Hughes at July 16th DAQ meeting.

# Introduction

- The eXtremely Fast Tracker (XFT) performs 2-d track reconstruction at Trigger Level 1.
- The inputs are hits on the sense wires of the axial COT layers.
- The XFT identifies tracks with a $P_T > 1.5$ GeV/c.
- The XFT reports a maximum of 1 track every 1.25 degrees. (288 max tracks/event).
- The XFT can be logically divided into two section:
  - Segment Finding (FINDING)
  - Segment Linking (LINKING)

# Segment FINDING

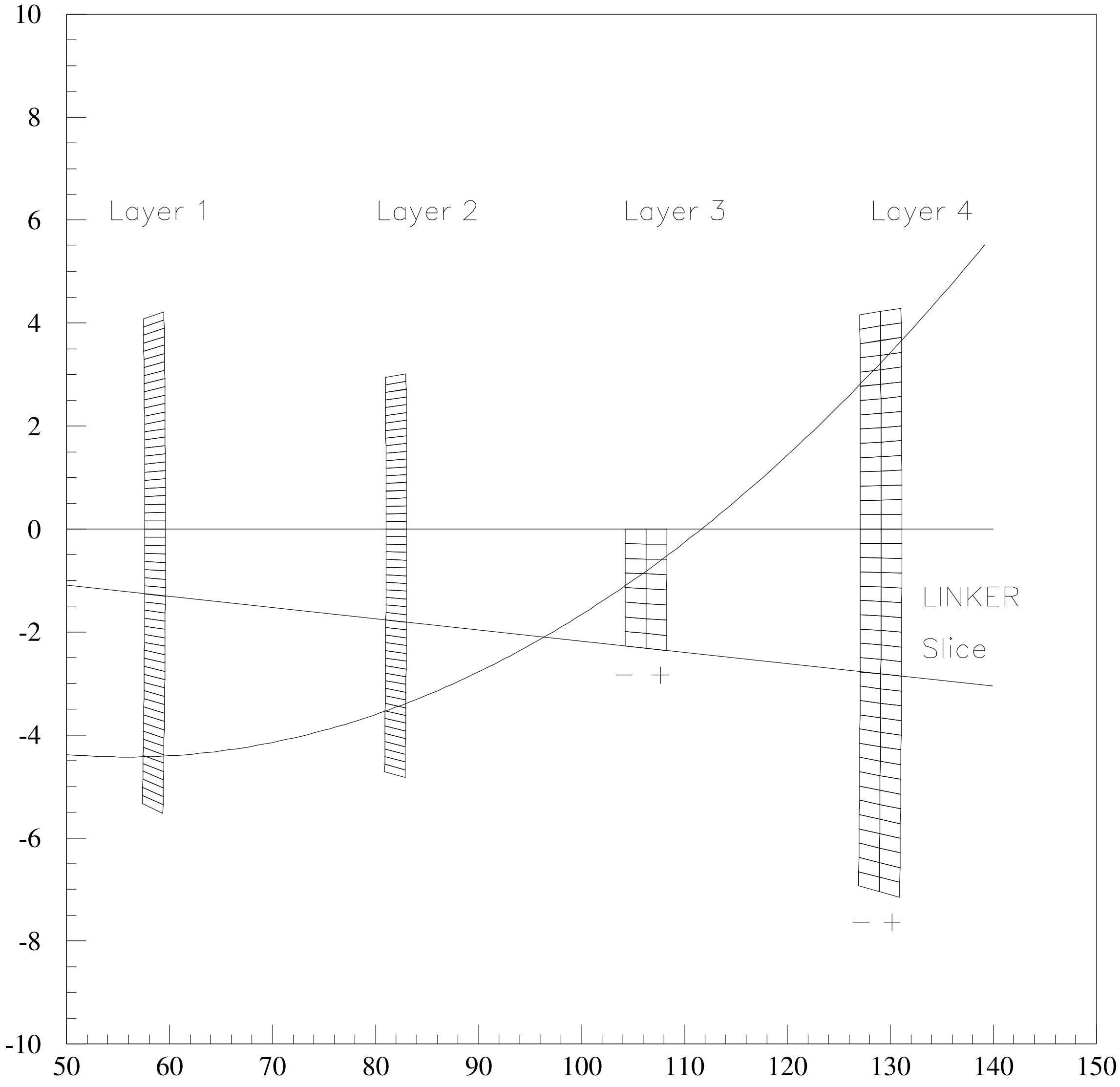
- A mezzanine card on the TDC classifies the hit(s) on a sense wire as PROMPT (near the wire) and/or DELAYED (far from wire).
- Segment finding involves looking for a pattern (MASK) of PROMPT and DELAYED hits on the 12 sense wires in a COT superlayer. The pattern can be spread out over several adjacent COT cells. (see figure)
- Search for *all possible* MASKs (patterns) for tracks with $P_T$ $> 1.5$ GeV/c.
- Due to wire hit inefficiencies, we allow a small number of 'misses' to be present and still 'fire' the MASK. (For wire eff = 99%, 1 miss is allowed, for wire eff = 92% three misses are allowed.)
- For the inner two axial superlayers, each MASK is characterized by a PIXEL which represents the phi position of the track. Each COT cell is divided into 12 of these pixels.
- For the outer two axial superlayers, each MASK is characterized by a PIXEL which represents the phi position *and* the slope (either '+' or '−') of the segment. Each COT cell is divided into 6 phi pixels and two slopes (a total of 12 pixels).
- When a MASK is found the corresponding PIXEL is turned on.



Layer 4
FINDER
1
12
10
8
6
4
2
0
−2
115
117.5
120
122.5
125
127.5
130
132.5
135
137.5
140

## Segment (Pixel) LINKING

- The PIXELS found in each axial superlayer are LINKED together to find valid tracks.
- Linking involves searching for all possible patterns (ROADS) of pixels for tracks with $P_T > 1.5$ GeV/c.
- Primarily, these ROADS are required to have a PIXEL found in each of the four axial superlayers. In a 1.25 deg slice of the COT there are $\approx$ 2500 different ROADS.
- Each ROAD is characterizes by a phi position in the third axial layer (the PIXEL in that layer) and one of 96 $P_T$ bins (48 for '+' charged tracks and 48 for '–' charged tracks).
- When a ROAD is found, the corresponding $P_T$ bin is set.
- All possible ROADS are found within a 1.25 deg slice of the COT. However, only the 'best' road is reported. The 'best' road is the highest $P_T$ track within the slice.


Layer 1
Layer 2
Layer 3
Layer 4
LINKER
Slice
− +
− +
10
8
6
4
2
0
-2
-4
-6
-8
-10
50
60
70
80
90
100
110
120
130
140
150

## Simulation Results

The XFT Algorithm has been implemented into a standalone fortran simulation and into the CDFSIM simulation of the COT. The table below summarizes the results of the simulation.

- Resolutions/fake rates,etc

Also see CDF Notes: XXXX and YYYY for more details.

# XFT Architecture

- PROMPT and DELAYED bits are set for each wire on a mezzanine board on the TDC boards.
- COT Transition card sits in the back of the TDC crates. Ansley cables plug into the card and transfer hit information to three XFT racks on the first floor.
- The top crate in each rack contains FINDER boards used for segment finding.
- Ansley cables plug into a transition cards which receive the information and drive it across the backplane pins to the FINDER cards.
- The results of a FINDER card is output through the front panel and routed to the front panel of the LINKER cards which reside in the lower crate in each XFT rack.
- The output of the LINKER cards is passed through the backplane to a transition card which sends the results onto the XTRP.

- Figure of Data Flow ( XFT_FLOW.PS)

- Figure of Crates (XFT_CRATES2.PS)

## Finder Board

- 48 FINDER boards in the system (Two types):
  - SL1/3 Boards: 2 FINDER Chips from SL1, 4 FINDER chips from SL3.
  - SL2/4 Boards: 3 FINDER Chips from SL2, 5 FINDER chips from SL4.
- There is an input section which aligns the data from different ANSLEY cables.
- The wire data is routed to FINDER chips. Each chips contains the logic to perform segment finding in 4 adjacent COT cells. (More below).
- The output of the Finders is passed to National Channel Links drives which provide the connection between FINDER and LINKER boards.
- The boards also contain a VME Interface, Controls, Clock Control, and Diagnostics.
- The SL1/3 board is designed to handle split wires in the first axial superlayer.

- Finder Block Diagram

## Finder Chip

- The FINDER chip is targeted at an Altera FLEX 10K50 programmable logic device (PLD).
- The chip searches for MASKs in four adjacent COT cells in the same axial superlayer.
- It stores all the possible masks for 1 COT cell of a given superlayer.
- It multiplexes the 4 COT cells through the MASK finding logic.
- It contains a L1/L2 pipelines of input wire and output pixel information.
- Dead wires can be flagged so as not to be counted as a 'miss'.
- The chip is reprogrammable at any time.

- Finder Chip Block Diagram

## Finder Milestones

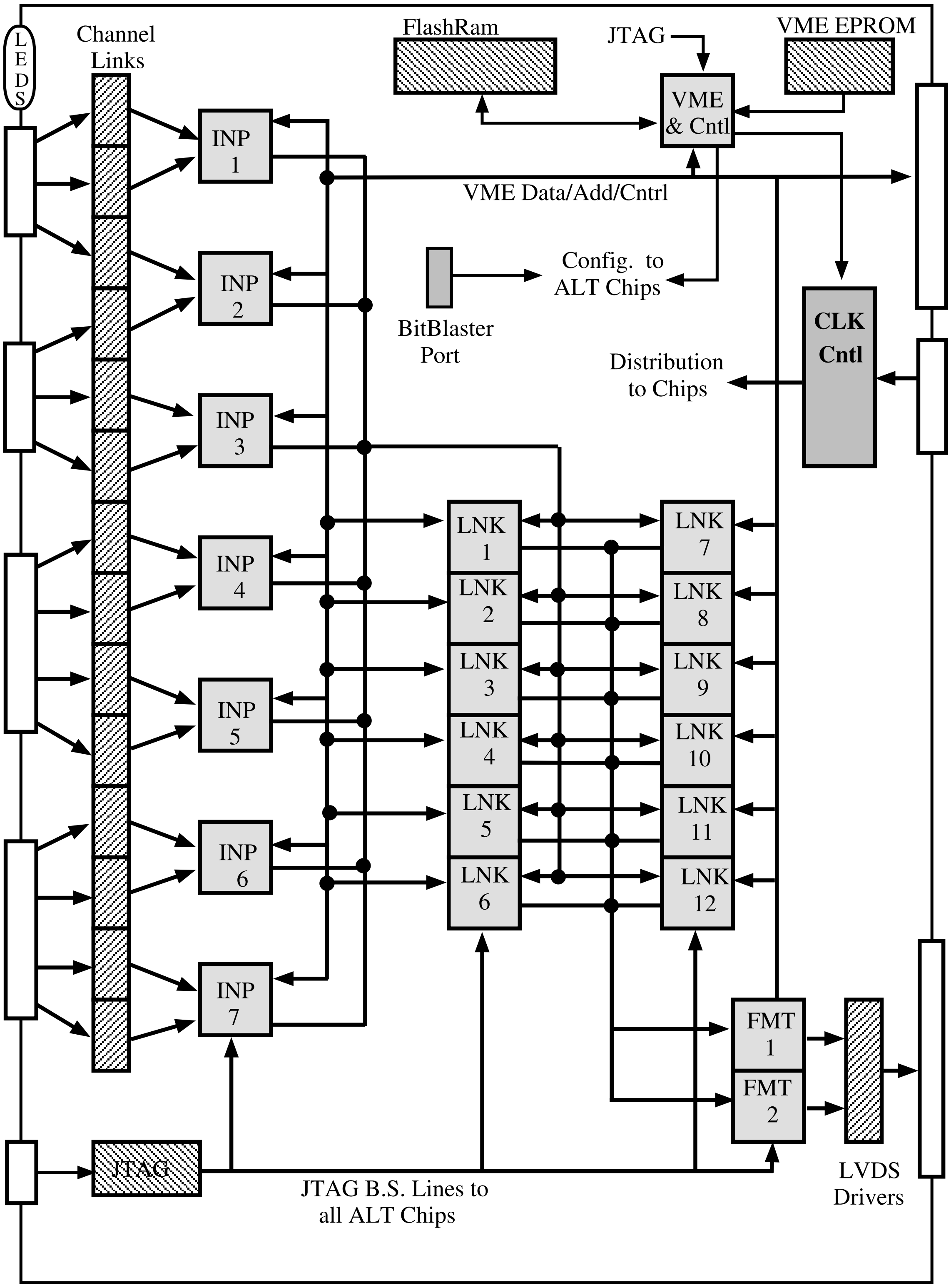
- COT transition card has been designed. Slight modifications pending and waiting for pinouts from COT mezzanine card.
- A prototype Finder transition card has been built and tested. (In need of a mechanical mock-up of XFT rack to examine cooling issues).
- Prototype backplane laid out and built. Electrical testing done..looks good. Redesign for additional neighbor wire sharing done (pending a small simulation study).
- FINDER chip design completed and simulated. (Soon to be tested in actual device...see below)
- Test Board for FINDER to LINKER communication being designed (more below).
- Began schematic for Finder prototype boards.

## Linker Board

- 24 identical LINKER boards in the XFT system each covering 15 degrees of the COT.
- Each LINKER board contains 12 LINKER chips which search for tracks in 1.25 degree slices of the COT.
- Each board accepts input from 4 FINDER boards (2 SL1/3 and 2 SL2/4) boards).
- The inputs are registered and aligned from the channel links by Altera Flex 10K20 PLD's acting as input buffers. These input chips contain the L1 pipeline/L2 buffers for the input pixels.
- The LINKER chips perform the ROAD linking logic (more below).
- The output of the LINKER chips is sent to 1 of 2 FORMATTER chips. These are Altera Flex 10K20 PLD's. The FORMATTER chips:
  - Pt compression
  - Formats the data for the XTRP
  - Removes/Flags duplicate tracks between LINKER chips.
  - Contains L1 pipeline/L2 buffers for LINKER Results.
- The outputs of the FORMATTER chips are sent by LVDS drivers over two 60 conductor flat cables to the XTRP.

# Linker Board Block Diagram

( V 2.0 7/8/97 BLW)

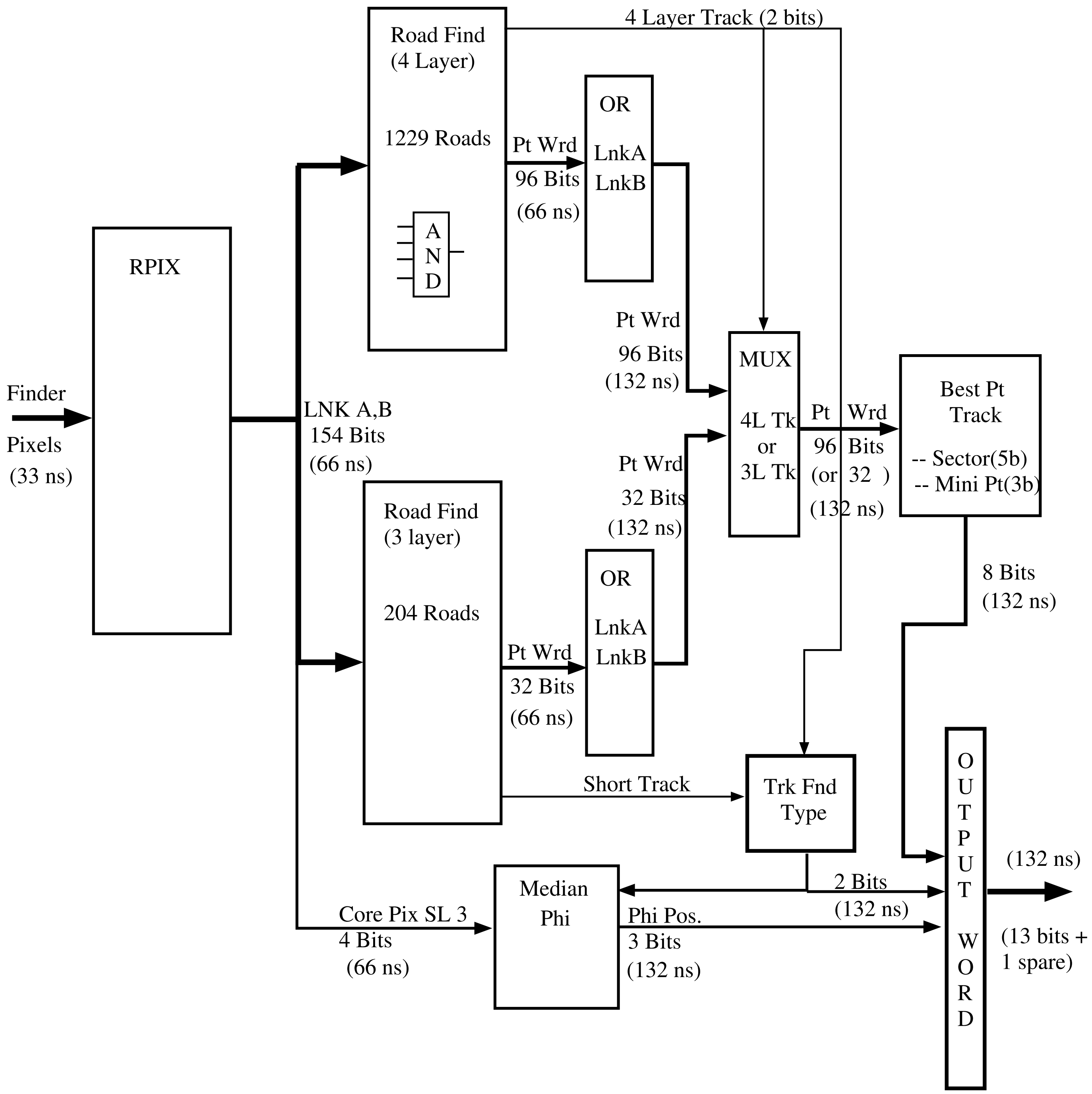


## Linker Chip

- The LINKER chip takes FINDER pixels as input and a searches for valid ROADS (tracks).
- This is implemented in an Altera FLEX 10K70 chip.
- The chip stores ROADS for the 1.25 degree slice that the Linker chip covers.
- The Linker chips searches for both 4 and 3-layer tracks. A 3-layer track is reported only if no 4-layer track is present.
- All valid tracks are found simultaneously.
- The 'best' track is selected from the found tracks. The track information is passed to the FORMATTER chip.
- The algorithm has been fully designed and simulated. (And partially tested in an actual PLD...see below)
- The chip is reprogrammable at anytime.

V2.0 (7/8/97) BLW

# XFT Linker Chip Block Diagram



## Linker Milestones

- Linker Chip Design Completed
- Simulation of Linker Chip in Altera Software:
  - Version of the Linker algorithm which includes only 4 layer tracks.
  - Implemented in a 10K50 (For use on Linker Test Board, see below)
  - Simulated all 2458 Roads at full speed (33ns clk).
  - Cross checked with a hardware simulation of the XFT system.
  - Increased clock speed to 28ns with no failures.
- Formatter Chip:
  - Design Complete
  - Simulated test vectors successfully
- Input Section Chip:
  - Design complete
  - Simulated test vectors successfully
- Began the schematic for Linker Prototype Board.

# Timing

- 1 clock tick = 132nsec
- Finder
  - Input alignment section = 1 clock tick
  - Finder chip = 1 clock tick
    (Note: The 1 clock tick is for the 1st of the 4 cells to be output. The Finder chip takes a total of 2 clock ticks for all 4 cells to be output.)
- Linker
  - Input section 0.5 clock ticks
  - Linker chip = 4 clock ticks
  - Formatter chip 1 clock tick
- Total from output of Ansleys to output of Linker board: 7.5 clock ticks.

*Detailed timing diagrams on web page*

## Prototyping and Testing

A number of Test boards have been and are being developed to test individual pieces of the system prior to full prototype boards.

Test Board I (Sept 96-Nov 96):

- Learn loading of Altera Chips
- Simple algorithmic test
- Comparison of Altera Simulation to chip performance.

Channel Link Test Board:

- Board to test the National channel links which will be used for FINDER to LINKER board communication.
- It will test several different cable configurations.

## Linker Test Board (March 97-Present):

- 3 Altera Chips (10K50's)
  - 1 chip act as input buffer/memory for test vectors
  - 1 chip used for testing (e.g LINKER chip)
  - 1 chip used for output buffer/memory and VME interface.
- Test VME Interface/Controls
- Loading of chips explored (e.g. via a FlashRAM loaded from VME)
- 4-layer track version of the LINKER chip has been successfully tested AT SPEED.
- Will soon extend testing to FINDER chip, Linker FORMATTER, etc.
- Development of JTAG Boundary Scan diagnostics.

## FINDER and LINKER Prototypes:

- The schematics for the prototypes are well underway.
- Expect layout to be finished in Sept.
- Fabrication and check out in Oct.
- System level test in December with 1/24 of XFT (4 FINDER boards, 1 LINKER board)

# Extension of XFT to Stereo Segment Finding

The method developed for segment finding in the axial layers can be extended to the stereo layers. The XFT group has investigated this extension for the outer stereo layer of the COT. For more details see talk by R. Hughes at June 25th, 1997 DAQ meeting.

- Algorithm for a stereo FINDER chip would be exactly the same as axial FINDER, just a different set of MASKs.
- MASKs would assume no stereo angle.
- Divide each cell into 6 phi pixels (no slope)
- Stereo angle causes an apparent phi shift of the segment relative to the 2-d track found with the axial layers.

- The difference between the expected phi position ($\phi_{exp}$) from the 2-d XFT track and the found stereo phi position ($\phi_{fnd}$) gives the Z position of the track in the stereo layer:

$$Z = \tan(\phi_{exp} - \phi_{fnd}) \cdot \frac{1}{Slbr}$$

where $Slbr$ is a constant dependent on the stereo angle.

## Stereo Simulation Results

Performed studies with Standalone Simulation (includes Geom., pulse modeling) with single tracks with a flat distribution in $P_T$ from 1.5 GeV/c – 10 GeV/c. Minimum bias events from Monte Carlo are overlayed on these single tracks to model $\mathcal{L}$ = 2E32 and 1E33.

| Performance | 2E32 | 1E33 |
|---|---|---|
| Efficiency | 99.5% | 98.9% |
| Z Resolution | 5.8cm | 5.9cm |
| Comb. Backg | 3.5% | 12.7% |

- Efficiency is for finding a Stereo segment within a valid window around a found XFT track.
- Resolution for Z position at the center of the stereo superlayer (SL7).
- Comb. Backg is the percentage of the time more than one stereo segment in the valid region around XFT track.

Studies are currently in progress to estimate the impact of Z position information on trigger rates.

## Possible Implementation

Implementation of segment stereo segment finding can be achieve with little extra engineering effort:

- Slight modifications to existing FINDER board design.
- New custom backplane for neighbor sharing of wire information.
- 108 Ansley Cables (or equivalent)
- 1 VME Crate

Note: The Stereo segments must be linked with 2-D XFT tracks. Depending on where is task is performed (L2?) a new board or at least some hardware modification needs to be made. The algorithm for linking is simple (a look-up table) but how and where this is accomplished has not been fully explored.

# XFT Milestones

| | |
|---|---|
| 8/96 | Finish Conceptual design of XFTII for COT. |
| 9/96 | Determine feasibility of FPGA for FINDER/LINKER. |
| 10/96 | Architecture design. |
| 10/96 | Test Board 1 finished.<br>Test JTAG loading/unloading of registers.<br>Test simple portions of FINDER/LINKER design. |
| 3/97 | LINKER Test Board finished.<br>Test full FINDER/LINKER algorithm, at speed.<br>Test planned (multiple) loading of FPGAs.<br>Test JTAG, VME. |
| 9/97 | FINDER/LINKER prototype design/layout finished. |
| 10/97 | FINDER/LINKER prototypes fabricated, checkout begins.<br>New version of prototypes for backplane,<br>Finder transition module<br>First version COT Transition module<br>First version of Linker Transition module |
| 12/97 | XFT 1/24 system level test.<br>(4 FINDER boards, 1 LINKER board) |
| Mid 98 | Start production. |